GaN HEMTs for low-noise amplification — status and challenges

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***Abstract*—GaN electronics combine speed with power handling capabilities and are currently on the path to replace established GaAs electronics in many applications. This paper reviews the advantages that GaN-HEMTs provide in low-noise amplification, and discusses the state of the art and the remaining challenges.**

I. INTRODUCTION

The GaN HEMT technology is currently on its way to replace GaAs technologies in many commercial applications. The rationale behind the significant efforts that were spent by industry and academia was primarily the combination of highest power handling capabilities together with high speed, which promised to enable new applications requiring higher bandwidth and power at higher frequencies — like 5G — and simplified and more compact realization of transceiver components in general.

Although power amplification was the driving force, GaN HEMT technology should also be investigated concerning receiver applications. Besides the fact that it is economically interesting to use the same technology for receive and transmit MMICs, GaN HEMTs proved to have a number of features that are highly interesting for receiver design.

First of all, the lowest RF noise figure is obtained from HEMT devices due to the low thermal noise of the 2DEG channel. GaN competes in this respect with optimized GaAs and InP technologies, and it is observed that the gap in performance gets narrower over the years. On the other hand, traditional low-noise components were not able to handle high input powers well, which is an obstacle in system design. Either the receiver can be subject to an unwanted jamming signal, or it suffers from interference by the transceiver's own power amplifier. In any case, the requirements concerning filtering, switching and overload protection require to be considered. Usually, adding off-chip components like limiters and isolators add cost and complexity. It is highly desirable from a systems point of view to have the freedom of designing single-chip solutions. GaN on SiC, in addition, is a very good heat conducting material which supports the realization of single-chip transceivers.

In the following, we will first compare recently published performance data of GaN low-noise amplifiers (LNAs) and their integration into single-chip transceivers in order to show that this technology is indeed competitive already today. Then, we will address the question how the power handling capabilities of the transistors can be utilized to design for higher linearity or ruggedness, and how the circuits recover from RF stress.

II. PERFORMANCE OF GAN LNAS AND TRANSCEIVERS

Until recently, GaN LNAs generally suffered from rather high noise figure and low gain, so that it was well possible to claim low-noise performance for an amplifier providing a noise figure slightly below 4 dB at Ka-band [1]. But today, the most advanced LNAs provide between 1 and 2 dB at Ka band and compare their performance directly to InP and GaAs technologies [2]. The improvement is not only a result of scaling — from a 120 nm gate length to 20 nm for these two examples — it rather is the result of advancements in technology that led to a significant reduction in contact and access resistances and increased transconductance. However, aggressively scaled technologies pay a prize in terms of breakdown voltage, which is around 10 V for the cited 20-nm technology. Therefore, GaN LNAs up to X band rather rely on more relaxed technologies providing performances like a noise figure of 0.5 dB at 10 GHz, breakdown voltage slightly over 100 V and $f_t \approx 50$ MHz at a gate length of 0.17 µm [3].

Especially for S- and X-bands, transceiver chipsets [4], [5], GaN-based transceiver modules [6], [7], and single-chip solutions [8], [9] were proposed. As an example, [10] presents an X-band chipset consisting of a 27-W, 36% PAE power amplifier chip, a SPDT switch chip and an LNA providing 23 dB of gain together with a noise figure of 1.6 dB. A single-chip transceiver integrating these three building blocks is shown to provide about 40 dBm of output power together with a noise figure between 2.5 and 3 dB in the receive path including switch losses [11].

A single-chip switchless design, taking advantage of the ruggedness of the GaN LNA is also published [12], providing still slightly above 30 dBm in the transmit and a noise figure of 4.5-5 dB an 20 dB gain in the receive path.

III. GAN LNA IN THE PRESENCE OF JAMMING SIGNALS

Jamming signals can be in-band or out of band, they can be received by accident or intentionally, or even be the cross-coupled transmit signal. We need to distinguish two cases: if the jamming signal is of low power levels, an LNA of sufficient linearity will be able to cope with the situation without degrading system performance. High power levels, on the other hand, can be harmful for the receiver electronics. In this case, we wish to protect our receiver. GaN LNAs provide the benefit to be self-protecting up to very high power levels. Since a high-power in-band pulse shadows all other signals anyhow, the question besides of the maximum power rating is: how fast will the the LNA recover and return to normal small-signal low-noise amplification.

2017 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC)
April 20-21, 2017, Graz, Austria
ISBN: 978-1-5090-5861-7

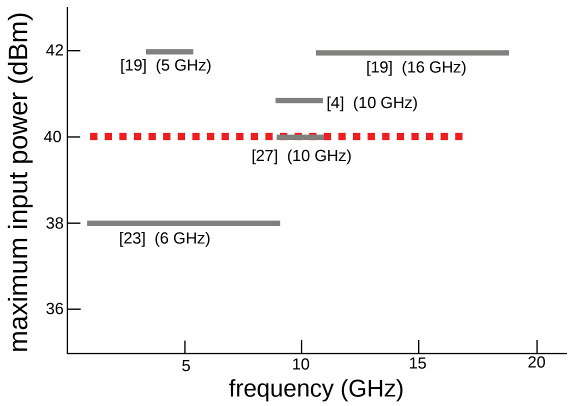

Fig. 1. Overview of highest safe input overdrive powers reported in the literature for (after [27]).

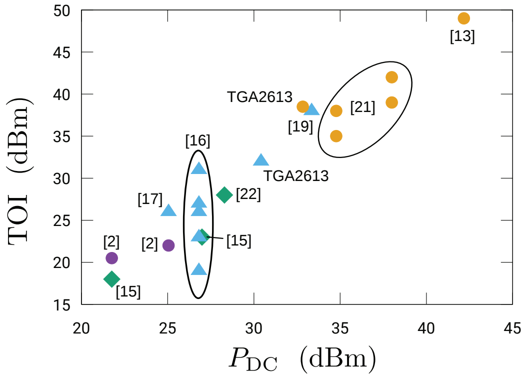

Fig. 2. Dependence of TOI on DC power consumption for LNAs reported in the literature and two commercial LNAs. The LNA operation frequency bands are (purple bullets): Ka-band, (green diamonds): X-band, (blue triangles): S–C-band, (yellow triangles): L-band and below.

A. Linearity

GaN LNAs intrinsically provide high linearity without the requirement for the designer to apply really advanced techniques. As LNAs are class-A amplifiers, high supply voltages and currents potentially boost linearity. This comes at the cost of high dissipated power levels. This might also be the reason why our record in TOI of 49 dBm for a hybrid 2-GHz LNA [13] was outperformed so far only by 1 dB [14]: its power consumption of 16 W might be prohibitive for most real-world applications — and the additional dB in TOI required to spend another 4 W. A number of publications, including [14] present numbers on the trade-off between power consumption and linearity. Schuh and Reber, for example, show that increasing DC power from 100 mW to 500 mW reduces LNA noise figure at X-band from about 1.8 dB to slightly below 1.6 dB while boosting TOI from 18.5 dBm to 23 dBm [15]. The trend is not unusual for GaN devices: As the technology is designed for high operation voltages, best small-signal and noise performance will be obtained at higher supply voltages as for traditional GaAs processes. For the Ka-band, Micovic shows similar noise figures, and increases TOI by 1.5 dB to 22 dBm when DC power is increased from 150 mW to 320 mW [2].

Figure 2 provides an overview on published TOI values as a function of power consumption. The LNAs are designed for different frequency bands in different technologies, ranging from 40 nm gate length [2] to 250 nm (all others). The picture shows that basically, TOI scales with power handling capability of the process and with bias point: scaled technologies provide good RF performance already at low voltages and currents, while high-power L-band transistors demand higher drain voltages but also allow to trade power consumption for linearity.

B. Ruggedness

Ruggedness in GaN is basically achieved by driving the HEMT into a state where it reflects most of the incident power. In a traditional receiver, a protection circuit would shorten the input, but if the first active component in our case is the GaN HEMT, that's clearly not an option as it would damage the gate diode.

But the gate of the HEMT is close to an open circuit anyhow. In the presence of overdrive input powers, the circuit needs to ensure that the stress on the gate diode is low, the power dissipated in the device is under control and that the LNA's output power is not harmful to the subsequent electronics. This can be achieved by changing the bias towards a deep class-C operation point.

A circuit topology enabling the LNA to change its bias dynamically at high input power levels requires only to feed the gate voltage through a high-ohmic resistor R. With increasing input powers, the gate voltage swing increases as well, eventually driving the gate diode into conduction at the positive peak voltage. As a result, a positive DC gate current I_g is observed, lowering the gate voltage V_g by $R \cdot I_g$. Figure 3(a) shows the schematic, (b) the voltage at the gate as a function of input power measured for a single $4 \times 50\,\mu\mathrm{m}$ GaN HEMT at 2 GHz, and (c) presents the measured gate current-voltage waveforms for the lowest and highest input power [17]. Following this scheme, the GaN LNA is protected by keeping possibly harmful gate DC currents I_g low by selecting a high DC feed resistor R. As the HEMT is effectively operated in deep class-C, output power saturates, and self-heating stays under control. The LNA can thereby survive hours of overdrive input power easily, and the destruction power level is defined by gate breakdown voltage. As seen in Figure 3(c), GaN LNAs provide gate breakdown voltages similar to their drain breakdown voltages, which allows for maximum CW input powers up to about 40 dBm.

Virtually all rugged GaN LNAs rely on this mechanism. But even if the LNA itself is save, it might still provide output powers that are harmful to subsequent stages. Additional measures might be required to limit the LNA saturated output power, e.g. limiting drain current [18] or including a limiting circuit on the GaN LNA chip [15].

The maximum save input power reported for this topology is 15 W [19], it is limited by gate breakdown provided proper choice of DC feed resistor and matching circuit. In order to push this limit further, a stacked topology was proposed that applies the input voltage to a series connection of gates, thus adding the breakdown voltages [20]. In a first test, destruction powers exceeding 20 W were measured.

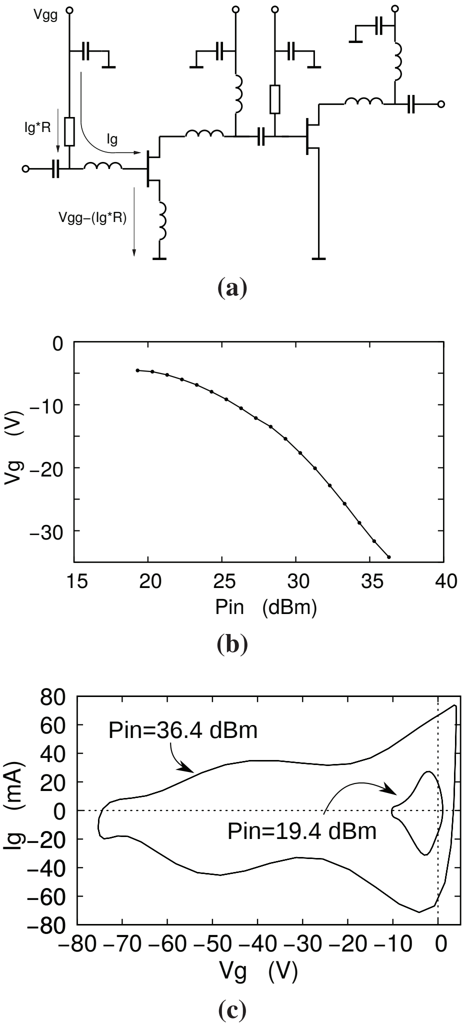

Fig. 3. (a) Typical circuit topology of a two-stage GaN LNA. (b) Measured gate voltage DC V_g of a $4 \times 50\,\mu$m GaN HEMT as a function of input power at 2 GHz. (c) Measured gate current-voltage waveforms for the lowest and highest input power [17].

C. Recovery Time

It is an important issue how fast an LNA recovers from an overdrive pulse. It is of prime importance that the LNA survives without damage, as discussed in the previous section, but long times required to return to normal operation after the blocking signal disappeared would be prohibitive e.g. in pulse radar applications.

Although this issue is relevant and is investigated by a number of groups, only few results get published. To begin summarizing the results, it is not easily possible to measure recovery of the noise figure directly. Instead, recovery towards the original bias point or towards the original S_{21} is measured assuming that the noise performance follows these indicators.

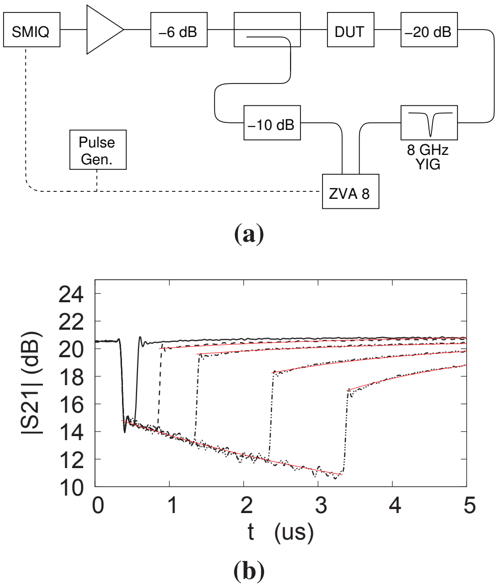

Fig. 4. Measuring recovery time of S_{21} at 8 GHz after a blocker pulse of 39 dBm at 2 GHz (a) measurement setup (b) time-dependent S_{21} measured for different pulse durations. The red lines indicate expected impact of self-heating and cooling down [24].

Figure 4a shows our initial measurement setup allowing to measure small-signal S_{21} at 8 GHz as a function of time through a Rohde & Schwarz ZVA, while applying pulses of 39 dBm at 2 GHz to the device. Measurement results are given in (b) for different pulse length together with red lines approximating the impact of self-heating and cooling down [24]. From this work we concluded that the device can heat up during the pulse, which leads to the known reduction in gain and an increase in noise. To avoid the effect, one would have to limit the power dissipation by an optimized design or an external limiter, e.g. as proposed in [15]. The only other effect observed in small-signal gain recovery was the RC time constant involved in discharging the capacitances at the LNA input, as the bias point returns from around -40 V to the normal bias around -2 V.

However, we learned that this is only part of the story. The LNA under test was designed to test for linearity and ruggedness, and the HEMT was operated at high currents instead of the 10% I_{DSS} that would be chosen as a rule of thumb for minimum noise performance.

A comparison of recovery times of two commercial GaN LNAs and a device from the Chalmers foundry revealed that LNAs featuring a Fe-doped buffer suffer from significant delay in recovery compared to instant recovery of the Chalmers device without buffer doping [25]. They used a vector signal generator and an amplifier providing up to 33 dBm pulses of 1 to 100 µs at 3 GHz. After the pulse, the generator signal jumps back to -20 dBm. A vector signal analyzer is employed to measure the transmission, and also variation in drain supply current is monitored. In this measurement, it was observed that the two LNAs from different commercial technologies needed in the range of 10 ms until the difference in gain reduces to less than 3 dB after a 10 µs, 33 dBm pulse. The DC drain currents followed this trend, and even the device that did not suffer from gain degradation showed a post-pulse reduction in current. It seems that this behavior is caused by memory effects that still play a dominant role in GaN transistors, since the time constant is too long to be explained by thermal or capacitance discharging effects and because it is only observed if the HEMTs buffer layer is Fe-doped.

The study also shows that the gain drop depends on input signal power, which can be explained by the higher voltage swings that activate more traps. For one of the devices, gain

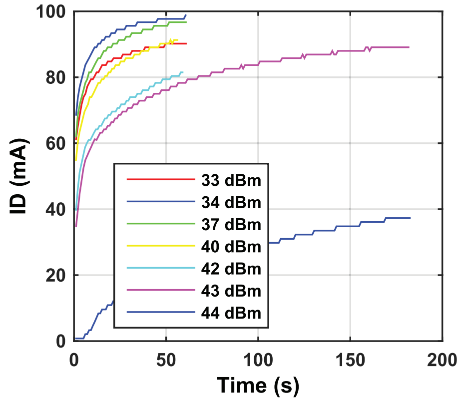

Fig. 5. Recovery of the DC drain current of a stacked GaN LNA MMIC after a CW stress measurement at 5 GHz. The overdrive input power presented to the LNA is given in the inset [26].

even stayed below 0 dB for almost 0.5 ms. This means that the LNA is effectively switched off by the pulse for a significant amount of time.

Investigation of DC current recovery of our own LNAs [26] showed even longer recovery times in the range of minutes, see Figure 5. However, with the results of [24], [25], we do not expect any significant negative impact of DC bias point variations on the small-signal performance.

Regarding the recovery of GaN LNAs after high-current pulses, one needs to consider self-heating due to the much higher powers the LNA survives. Even more challenging is the impact of traps leading to very long time constants concerning the return to the original bias point. Depending on the type of traps involved, small-signal gain can be affected as well.

IV. CONCLUSIONS

GaN LNAs provide interesting features that are not available in other technologies. Depending on technology and circuit design, high ruggedness, high linearity and competitive noise and small-signal performance can be achieved. Although recovery after overload by blocking signals remains to be a challenge, first devices become commercially available and research is underway that exploits the unique features of GaN to integrate full transceiver front-ends on single chips, e.g. for X-band radar applications.

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