Direct Model Predictive Control of Noninverting Buck-boost DC-DC Converter

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***Abstract*—In this paper, direct model predictive control (DMPC) of the noninverting buck-boost DC-DC converter with magnetic coupling between input and output is proposed. Unlike most of the other converters, the subject converter has the advantage of exhibiting minimum phase behavior in the boost mode. However, a major issue that arises in the classical control of the converter is the dead zone near the transition of the buck and boost mode. The reason for the dead zone is practically unrealizable duty cycles, which are close to zero or unity, of pulse width modulation (PWM) near the transition region. To overcome this issue, we propose to use DMPC. In DMPC, the switches are manipulated directly by the controller without the need of PWM. Thereby, avoiding the dead zone altogether. DMPC also offers several other advantages over classical techniques that include optimality and explicit current constraints. Simulations of the proposed DMPC technique on the converter show that the dead zone has been successfully avoided. Moreover, simulations show that the DMPC technique results in a significantly improved performance as compared to the classical control techniques in terms of response time, reference tracking, and overshoot.**

***Index Terms*— Noninverting buck-boost DC-DC converter, Direct model predictive control, Dead zone avoidance.**

I. Introduction

In numerous applications, like battery charging/discharging, fuel-cell regulation systems, power factor correction, and MPPT of solar panels, a dc-dc converter is used to obtain a controlled output from a varying input source [1]-[3]. A non-inverting buck-boost converter is preferred in applications requiring buck-boost properties and having low current/voltage ripples [4]. Their beneficial aspects incorporate high power transfer efficiency, small voltage ripples, and small stresses on active and passive components [5], [6].

Majority of the converters that operate in boost mode exhibit right half plane (RHP) zeros in continuous-conduction-mode. The existence of these RHP zeros, which makes the system non-minimum phase, has the tendency to make the controller design difficult, limit the loop bandwidth, penalize output capacitor size, and make the converter susceptible to oscillations[1], [7]. The combination of magnetic coupling between input and output inductors [8] and a series resistor-capacitor network [9] depicted in Fig. 1, has successfully eliminated RHP zeros. Thus, the system can easily achieve wide control bandwidth. Other advantages include the prospect of regulating input/output currents or voltages [10] with quick and response [11].

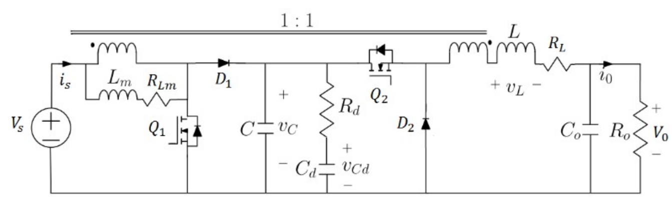

Fig. 1. Circuit diagram of noninverting Buck-Boost converter.

However, the topology in Fig. 1 also possesses an extensive downside. The switching pulses generated near the vicinity of transition between buck and the boost mode are so short that a practical circuit cannot catch it. As a result, a so-called dead zone appears close to the transition region. The appeared dead zone denotes the discontinuity in the converter conversion ratio (1) defined in a single duty ratio control variable *u* which takes values between 0 and 2 [2] as shown in Fig. 2. The dead zone causes excessive ripples in the output voltage and potential disorder of the converter [12]. The vanishing of dead zone is of great importance because we want soft transition between buck and the boost mode in several applications [13]-[15].

$$M(u)=\frac{\min(1,u)}{1-\max(0,u-1)} \tag{1}$$

$$\begin{cases} s_1=\max(0,u-1) \\ s_2=\min(1,u) \end{cases} \tag{2}$$

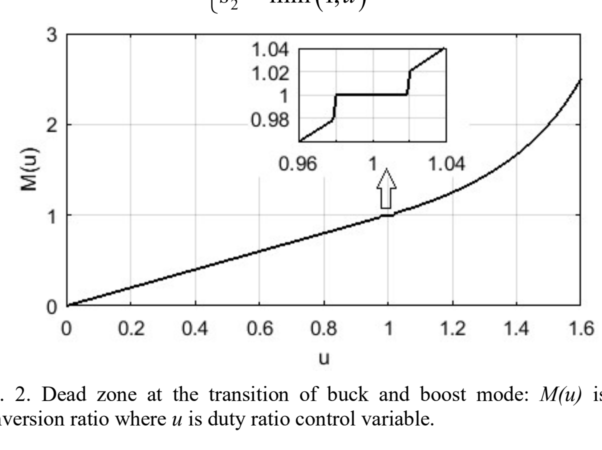

Fig. 2. Dead zone at the transition of buck and boost mode: *M(u)* is the conversion ratio where *u* is duty ratio control variable.

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Numerous dead zone minimization methods have been used in the literature [5], [16]-[21]. A well-known technique is focused on the overlap of buck and the boost operation modes at the buck-boost transitions [2], [17], [18]. Its principle disadvantages are: ripples in output voltage are poorly minimized, there are substantial subharmonics and the switching losses are almost twice [2]. In [12] much better results were obtained regarding dead-zone minimization, in which the overlapping of buck and boost mode is merged and fixed with the duty cycle of buck mode to its optimum attainable value. But the main drawback of this technique is that the ripples are improved at the cost of efficiency in the boost mode [12]. Another strategy was proposed in [22]. The principle concept of this technique is the addition of the dead zone avoidance and minimization (DZAM) machine in the control loop that will vanish the dead zone. Unfortunately, this technique is difficult to actualize in analog control systems.

In the literature, some other methods are used for attaining soft transitions, which can't be readily employed to the converter topology examined in this paper. They either rely on sliding mode control [23], [24] or adjust each duty cycle to exactly half [15].

The main contribution of this paper is to use direct model predictive control (DMPC) for the aforementioned topology that can completely avoid the dead zone. DMPC is one of the emerging control techniques for power electronics converters [25]-[36]. Key advantages of DMPC are: it can deal with plant nonlinearities, multiple inputs, multiple control objectives, and any constraints on inputs/states while ensuring optimal control [37]. Another advantage of DMPC is that unlike PWM control, the switch can be directly controlled without a demodulator. Avoiding demodulator allows to use an accurate model of the converter that incorporates switching nonlinearities as compared to an averaged model. The use of accurate model along with optimal control allows DMPC to exhibit superior performance for some power converters as compared to most other control techniques [25], [28], [34]. In DMPC switch transitions are only done at a fixed sampling time, thus limiting the minimum width of the switching pulses. This completely wipes out the dead zone to attain smooth transitions between buck and boost mode. A disadvantage of DMPC is its high computational complexity. However, it has been mitigated by some efficient techniques and the availability of fast speed microprocessors [28], [38]. Another key point is that the converter in Fig. 1 is minimum phase. Therefore, we can have a small value of prediction horizon to reduce the computational complexity.

The paper is organized as follows. Section II presents the state space mathematical model of the converter. The proposed control scheme is presented in Section III. In Section IV the simulation results are shown. Finally, the conclusion is stated in Section V.

II. State Space Modeling of the Converter

The buck-boost converter depicted in Fig. 1 contains two controllable transistors Q_1 and Q_2; and two power diodes D_1 and D_2. The inductors L and L_m with the internal resistances R_L and R_{Lm} , respectively, and capacitors C and C_0 are used for storing and delivering energy according to the operating mode of the converter. The converter has two controllable inputs S_1 and S_2, which represent the gate signals of transistors Q_1 and Q_2, respectively.

TABLE I
Switching States

S_1	S_2	Status
0	0	Used in Buck Mode
0	1	Used in Buck, Boost Mode
1	0	Used in Boost Mode
1	1	Not Used

In the PWM based control an averaged model is used. However, we will utilize the model for all switching combinations. All the possible combinations of controllable inputs are shown in Table I, where 1 denote ON state and 0 denotes OFF state of the transistor. Assuming continuous-conduction-mode (CCM), three different linear models are related with the switch positions. The continuous-time model of the converter is as follows:

$$\dot{x}(t)=\begin{cases} A_1x(t)+Bv_s(t) & s_1=0,s_2=0 \\ A_2x(t)+Bv_s(t) & s_1=0,s_2=1 \\ A_3x(t)+Bv_s(t) & s_1=1,s_2=1 \end{cases} \tag{3}$$

where

$$x(t)=\left[i_{Lm}(t),i_L(t),v_c(t),v_o(t)\right]^T$$

is the state vector comprising of inductors currents and capacitors voltages,

$$A_1=\begin{bmatrix} -R_m/L_m & 0 & -1/L_m & 0 \\ -R_m/L & -R_L/L & -1/L & -1/L \\ 1/C & 1/C & 0 & 0 \\ 0 & 1/C_0 & 0 & -1/R_0C_0 \end{bmatrix}$$

$$A_2=\begin{bmatrix} -R_m/L_m & 0 & -1/L_m & 0 \\ -R_m/L & -R_L/L & 0 & -1/L \\ 1/C & 0 & 0 & 0 \\ 0 & 1/C_0 & 0 & -1/R_0C_0 \end{bmatrix}$$

$$A_3=\begin{bmatrix} -R_m/L_m & 0 & 0 & 0 \\ -R_m/L & -R_L/L & 1/L & -1/L \\ 0 & -1/C & 0 & 0 \\ 0 & 1/C_0 & 0 & -1/R_0C_0 \end{bmatrix}$$

and

$$B=\left[1/L_m,\quad 1/L,\quad 0\quad 0\right]^{\mathrm{T}}$$

The continuous-time model in Equation (3) can be discretized by using Euler approximation to obtain the following:

$$x[n+1]=\begin{cases} G_1x[n]+Hv_s[n], & s_1=0,s_2=0 \\ G_2x[n]+Hv_s[n], & s_1=0,s_2=1 \\ G_3x[n]+Hv_s[n], & s_1=1,s_2=1 \end{cases} \tag{4}$$

where

$$x[n]=\left[i_{Lm}[n],\quad i_L[n],\quad v_c[n],\quad v_0[n]\right]^{\mathrm{T}}$$

is the state vector, $G_i=I+A_iTs$ for $i=1,2,3, H=BTs, I$ denotes the identity matrix and T_S is the sampling time.

III. Proposed Control Scheme

The control technique used in this paper is direct model predictive control (DMPC). In DMPC the control law is based on an optimization problem. The optimization problem minimizes an objective function, which penalizes deviation from the control goals. The optimization problem finds the optimal switching sequence for the next N time samples, where N is the prediction horizon. In DMPC only the first switch positions in the optimal switching sequence are applied to the circuit and the optimization problem is solved again at the next time sample to incorporate feedback [39]. In DMPC the control mechanism is carried out by the direct manipulation of switch states for the complete sampling interval. Consequently, this technique never demands a modulator [40].

In our case we have two control goals. The first is to regulate the output voltage and the second is to improve efficiency by limiting excessive switching transitions. The objective function is designed such that it calculates the sum of output voltage error and the difference between two successive switching states over the finite prediction horizon N. The latter term is designed to reduce the switching frequency and avoid unnecessary switching. The objective function at time instant k is as follows:

$$J_n = \sum_{l=1}^{N}\left(\left|v_{0err}\left[n+l\right]\right| + \lambda\left(\left|\Delta s_1\left[n+l\right] + \Delta s_2\left[n+l\right]\right|\right)\right) \tag{5}$$

where $v_{0err}\left[n+l\right]:=v_{ref} - v_0\left[n+l\right]$ is the error in output voltage, v_{ref} is the reference output voltage, $\Delta s_1\left[n+l\right]:=s_1\left[n+l\right] - s_1\left[n+l-1\right]$ denotes a change in the position of s_1, and $\Delta s_2\left[n+l\right]:=s_2\left[n+l\right] - s_2\left[n+l-1\right]$ denotes a change in the position of s_2, and λ is the weighting factor.

The optimization problem in MPC is the minimization of the objective function Equation (5) to find optimal values of s_1 and s_2 over the prediction horizon. The optimization problem is stated below:

$$\left[S_{1,n}^*, S_{2,n}^*\right] = \underset{S_{1,n},S_{2,n}}{min} J_n \tag{6a}$$

$$\text{s.t.} \left(s_1\left[n+l\right], s_2\left[n+l\right]\right)\epsilon\mathbb{S}\ l = 0,\ldots,N-1 \tag{6b}$$

where $S_{1,n}:=\left[s_1\left[n\right], s_1\left[n+1\right],\ldots,s_1\left[n+N-1\right]\right]$ and are the sequences of switching states over the horizon $S_{2,n}:=\left[s_2\left[n\right], s_2\left[n+1\right],\ldots,s_2\left[n+N-1\right]\right]$ are the sequences of switching states over the horizon $N;\mathbb{S}:=\left\{(0,0),(0,1),(1,1)\right\}$ and $S_{1,n}^*$ and $S_{2,n}^*$ are the optimal sequences that minimize the cost J_n.

The constraint Equation (6b) ensures that only the feasible input combination shown in Table I are allowed. Solving the optimization problem results in optimal inputs for time instant n and future inputs for the remainder of prediction horizon. In DMPC, only the first element of the computed optimal sequences is applied to the system. At the next time sample, the state are measured or estimated and the optimization problem is solved again. This mechanism allows feedback in DMPC.

The optimization problem Equation (6) has an exponential computational complexity with the prediction horizon. Since there are three members in the set $\mathbb{S}$, there is a possibility of 3^N distinct sequence. In enumeration based techniques of DMPC the objective function Equation (5) has to be evaluated for each possible sequence [28]. Moreover, based on the model the future states also have to be predicted for each possible sequence. These calculations lead to increase in the total computational complexity. However, in our case we can keep a short horizon since the converter is minimum phase.

An advantage of DMPC is that the control inputs s_1 and s_1 can only be changed after the sampling interval. Therefore, unlike PWM, the transistor gate pulses are never smaller the sampling time, which may have issues in realizing practically. Moreover, in DMPC the converter doesn't exclusively operate in either the buck mode or boost mode. DMPC chooses the best feasible inputs in $\mathbb{U}$ that could meet the control goals. Another advantage of DMPC is that we can put other constraints in the optimization problem Equation (6). For example, a constraint on the maximum inductor currents can be used to avoid a current control loop used in classical control techniques.

The concept of proposed DMPC is summarized in algorithm 1, in which function f represents the state space model in Equation (4). Flow chart is abridged in Fig. 3. Initially the best known optimal cost J^* is initialized by a big number and all the possible 3^N sequences of inputs are generated. For each sequence the states and output are predicted that are used to

Algorithm 1 DMPC algorithm

Function $s_1^*(n),,\ s_2^*(n)=$**DMPC**$\left(\hat{x}(n), s_1(n-1)\right), s_2(n-2)$
    $J^*(n)=\infty; s_1^*(n)=\phi; s_2^*=\phi$
For all **S_1,** S_2 *over N* **do**
    J=0
  For n=1 to N **do**
    If $s_1(n)=1$ & $s_2(n)=1$ **then**
      $x(n+1)=f_1\left(x(n), s_1(n), s_2(n)\right)$
    else if $s_1(n)=0$ & $s_2(n)=1$ **then**
      $x(n+1)=f_2\left(x(n), s_1(n), s_2(n)\right)$
    else
      $x(n+1)=f_3\left(x(n), s_1(n), s_2(n)\right)$
    end if
    $v_{0err}\left[n+1\right]=v_{ref}-v_0\left[n+1\right]$
    $\Delta s_1\left[n\right]:=s_1\left[n\right]-s_1\left[n-1\right]$
    $\Delta s_2\left[n\right]:=s_2\left[n\right]-s_2\left[n-1\right]$
    $J=J+\left|v_{0err}\left[n+1\right]\right|+\lambda\left|\Delta s_1\left[n\right]+\Delta s_2\left[n\right]\right|$
  end for
  if $J<J^*(n)$ **then**
    $J^*(n)=\text{J}, s_1^*(n)=S_1(1), s_2^*(n)=S_2(1)$

end function

evaluate the objective function. If the objective function is smaller than J^*, then the best known cost J^* and best known input sequence is updated. The block diagram of the converter along with proposed controller is depicted in Fig. 4.

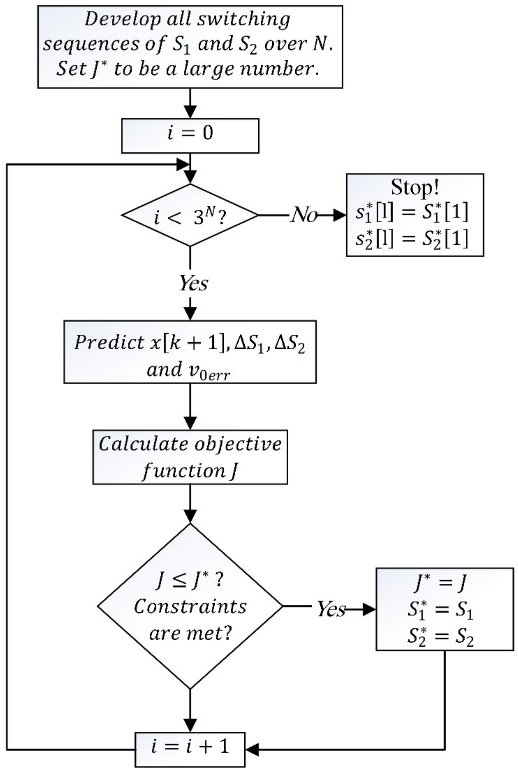


Fig. 3. Flowchart of the DMPC algorithm.

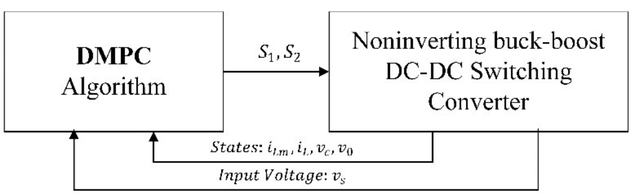
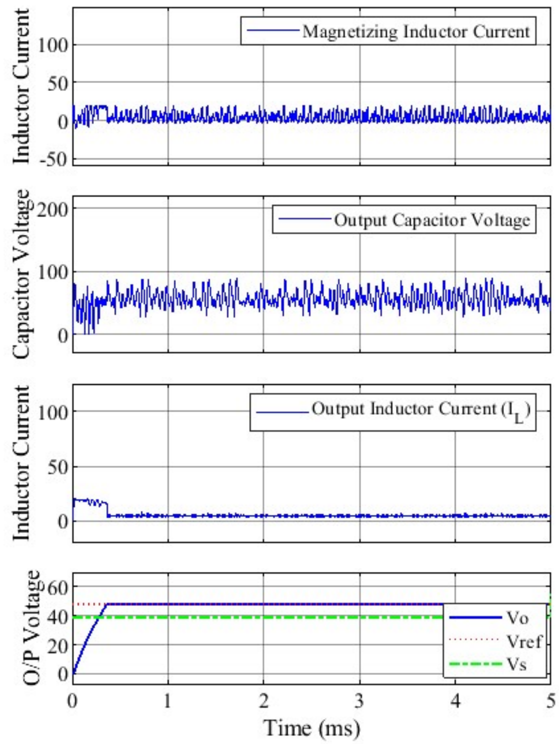


Fig. 4. Block diagram of DMPC algorithm.

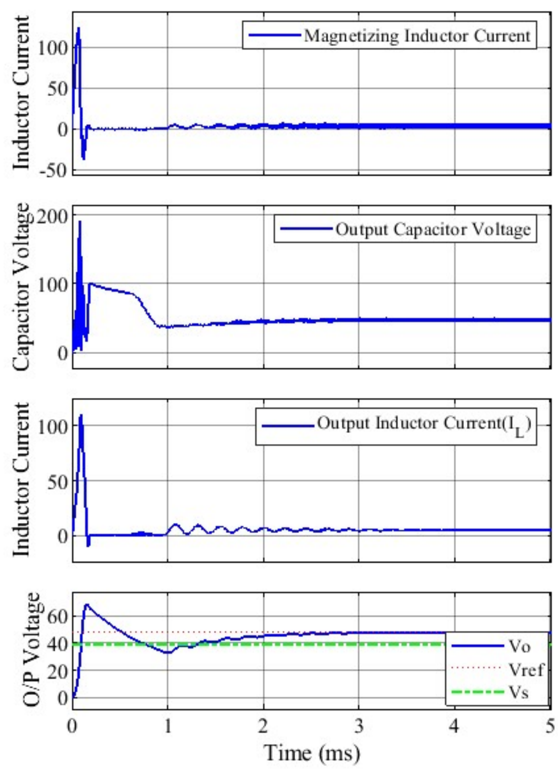
IV. Simulation Results and Comparison

The converter depicted in Fig. 1 is simulated with the proposed control and the obtained results are presented here. Five different cases are considered. In case 1 the converter start-up is observed. In case 2, step up and step down variation are made in reference voltage. In case 3 step up/down variation are made in the input voltage and the dynamic response of the converter is examined. In case 4, step down change is made in load resistor and response of controllers is observed. In case 5 ramp change in input is made to examine the controller's response close to buck/boost transition region.

The values of the parameters used are: $L_m = 14\mu H$, $R_{Lm} = 0.5\Omega$, $L = 30\mu H, R_L = 0.3\Omega, C = 2.6\mu F, R_d = 1.5\Omega$, $C_d = 22\mu F, C_0 = 110\mu F$ and $R_0 = 9.6\Omega$. Input voltage V_s varies in the range of 39V to 55V The control goal is to regulate the output voltage V_0 to 48V. The weighting factor λ is kept 0.1, while the prediction horizon N is taken as 6. The sampling time $T_s = 1\mu s$ and sampling frequency $F_s = 1MHz$. We have been able to use such a small N because the system is minimum phase. A small value of N helps to reduce the computational complexity of the algorithm. The results of the proposed DMPC are compared with PI controller. The PI controller has a proportional gain of 1/25 and integral gain of 100.



(a)



(b)

Fig. 5. Converter start up (a) Controlled through proposed DMPC (b) Controlled through PI.

A. Case 1: Start up with Constraints on Inductor Currents

The start-up of the converter with a constant input voltage of 39V is simulated with both PI controller and the proposed DMPC. In DMPC the currents $i_L[n]$ and $i_{Lm}[n]$ are constrained to be less than 20A each. The results are shown in Fig. 5. The inductor currents rise sharply to a peak of more than 100A in PI. On the other hand, the inductor currents in DMPC stay within the specified constraint of 20A . The settling time of DMPC is approximately $0.3ms$ as compared to approximately $2.5ms$ for PI control. Moreover, the DMPC has no overshoot as compared to an overshoot of nearly 42% for PI control. The ripple in the output voltage for both control schemes is 0.2%. The comparison shows that the proposed DMPC has a much improved performance as compared to PI control.

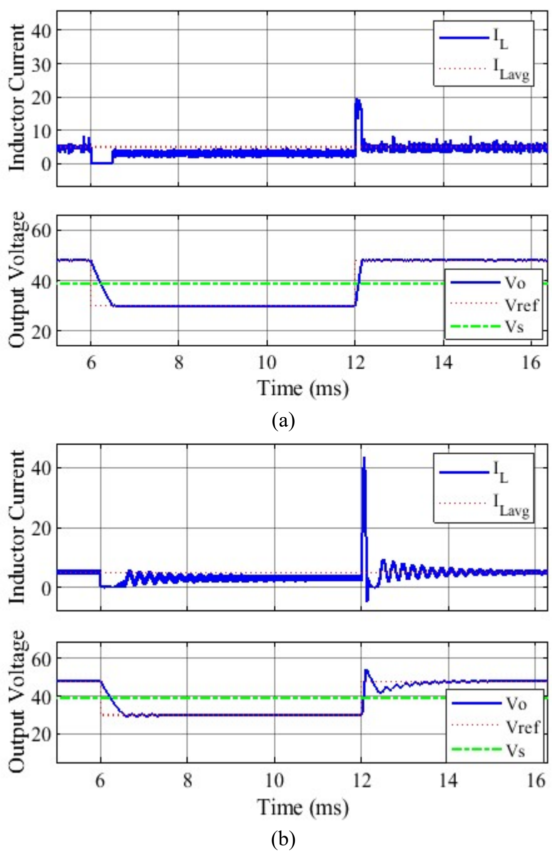


Fig. 6. Step changes in output voltage reference (a) Controlled through proposed DMPC (b) Controlled through PI

B. Case 2: Step Down/up Change in Output Reference Voltage

The reference voltage was stepped down from 48V to 30V and stepped up back to 48V at t=6ms and t=12ms , respectively. It can be seen in Fig. 6, that DMPC tracks the new reference quickly without any undershoot or overshoot as compared to the PI controller.

C. Case 3: Step Down/up Change in Input Voltage

In this case the input voltage was first stepped up from 39V to 55V at t=6ms and then stepped down from 55V to 39V at t=12ms . Response of both the DMPC and PI controller is depicted in Fig. 7. At the changes in input voltage, the DMPC controller keeps the converter output at the required reference without any significant deviation. Whereas the PI controller has an undershoot/overshoot and slow to track the reference.

Besides the advantages stated earlier, in this particular case the inherent feed forward control in DMPC contributes to the improved performance. The formulation of DMPC involves the value of input voltage in the model of the plant, which has a feed forward effect.

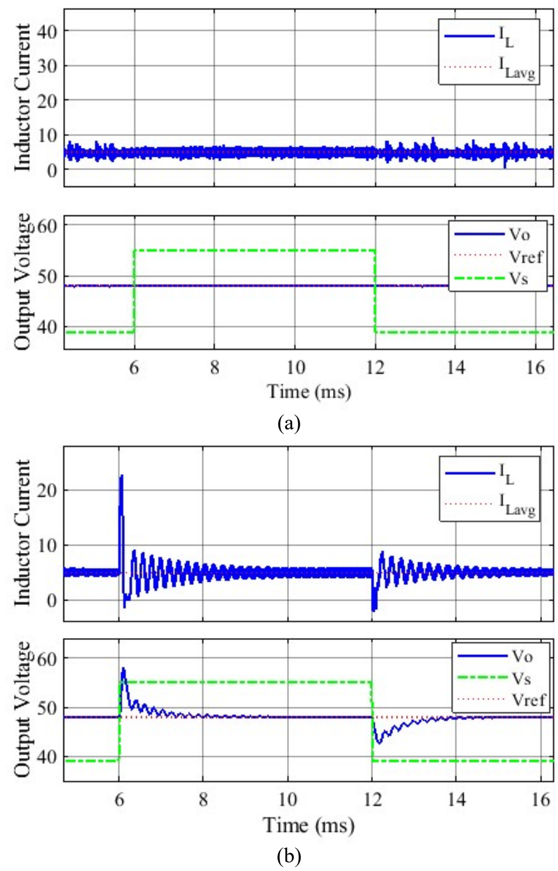


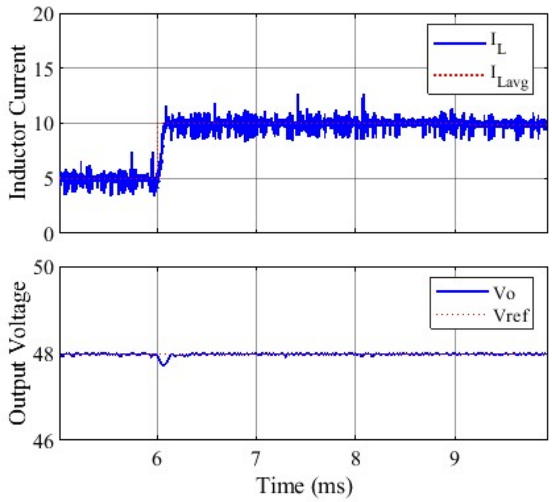
Fig. 7. Step changes in input voltage (a) Controlled through proposed DMPC (b) Controlled through PI.

D. Case 4: Step Down Change in Load Resistor

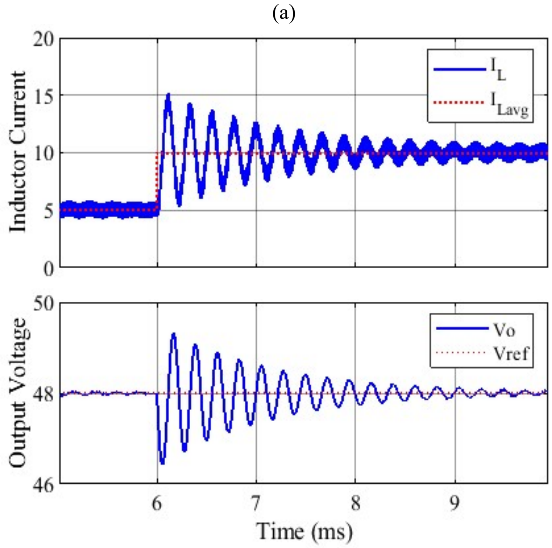
Usually, the load changes in an obscure way, which leads to a mismatch in model, and steady-state error in output voltage. In order to solve this problem, an additional external loop is needed to be designed, to provide state estimates and adjust the reference current to remove the steady state error. Although the PI-based loop may be sufficient to meet the above two goals, here a discrete-time Kalman filter is used in combination with DMPC and the performance is compared with PI. Due to the integral characteristic of the Kalman filter, it can accurately track the reference voltage. Here the load resistance drops to exactly half from $R_0 = 9.6\Omega$ to $R_0 = 4.8\Omega$ at $6msec$, shown in Fig. 8. The converter is simulated in boost mode with input voltage of 39V and reference voltage is kept 48V.

E. Case 5: Ramp Change in Input Voltage

In this case a linearly varying source is applied as an input voltage to the converter operating at steady state operating conditions with output voltage reference of 48V . Response of both DMPC and PI controllers is depicted in Fig. 9. Zoomed



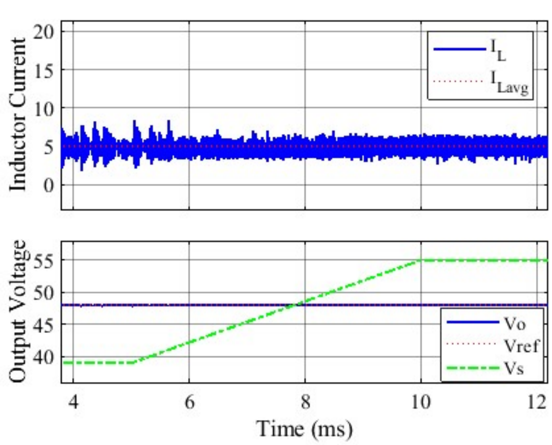
(a)



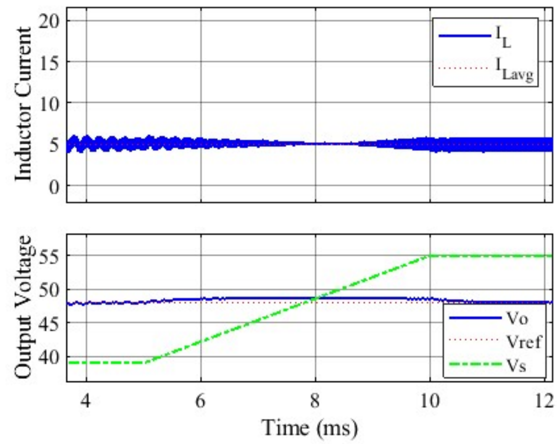
(b)

Fig. 8. Step down change in the load resistor (a) Controlled through proposed DMPC (b) Controlled through PI.

view of output voltage and respective duty cycles of transition region around 48V is given in Fig. 10. Fig. 10(a) clearly shows that in DMPC the smallest width of switching signals is $1\mu s$, which is easy to realize practically. Whereas in Fig. 10(b) for PI control, the width of switching waveforms can become too small for practical realization, which leads to dead zone.

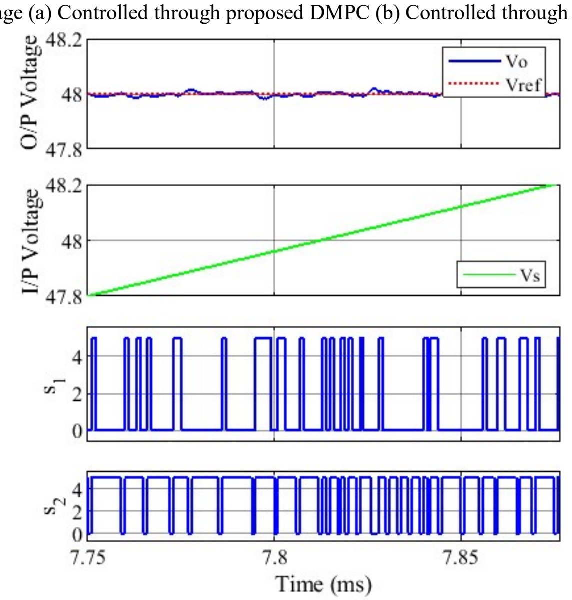


(a)

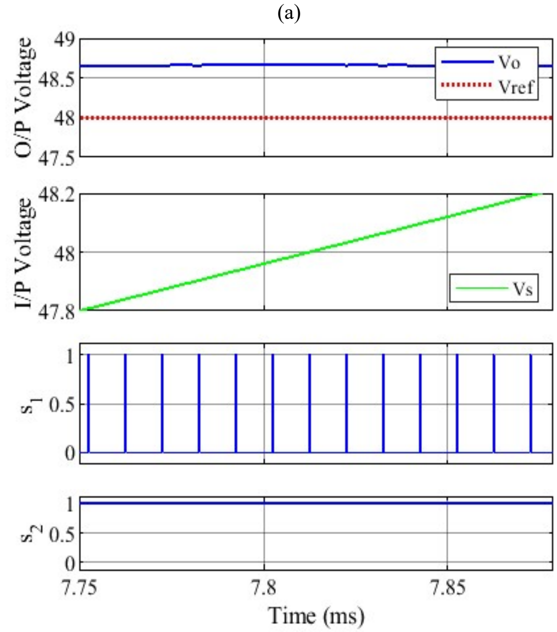


(b)

Fig. 9. Output voltage of the converter with respect to ramp change in input voltage (a) Controlled through proposed DMPC (b) Controlled through PI



(a)



(b)

Fig. 10. Zoomed view of output voltage and respective duty cycles round transition region (a) Controlled through proposed DMPC (b) Controlled through PI.

V. Conclusion

In this paper we proposed direct model predictive control of non-inverting buck-boost DC-DC converter. A key advantage of DMPC is that it directly manipulates the switches without the need of any modulator. Thereby, eliminating the dead zone in transition between buck and boost mode, which is of major concern in control of the subject converter. Another advantage of DMPC include inclusion of current constraints that avoids the use of an extra current loop. Other beneficial aspects of the proposed DPMC is lesser overshoot/undershoot, quicker response time, and inherent feed forward. A usual drawback of DMPC is its computational complexity. However, the converter is minimum phase which makes it possible to use a small value of prediction horizon that reduces the computational complexity.

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