A Modified Neutral-point Voltage Control Strategy for Three-level Inverters Based on Decomposition of Space Vector Diagram

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***Abstract*—Capacitor voltage imbalance is a significant problem for three-level inverters. Due to the mid-point modulation of these inverter topologies, the neutral point potential moves up or down depending on the neutral point current direction creating imbalanced voltages among the two capacitors. This imbalanced capacitor voltage causes imbalanced voltage stress among the semiconductor devices and causes increase output voltage and current harmonics. This paper introduces a modified voltage balancing strategy using two-level space vector modulation. By decomposing the three-level space vector diagram into two-level space vector diagram and redistributing the dwell times of the two-level zero space vectors, the modified voltage balancing method ensures minimal NP voltage ripple. Compared to the commonly used NP voltage control method (using 3L SVM [9]), the proposed modified NP voltage control method offers a slightly higher neutral-point voltage ripple and output voltage harmonics but, it has much lower switching loss, code size and execution time.**

***Index Terms*—Three-level inverter, Neutral-point voltage control, Execution time.**

I. Introduction

FOR high power energy conversion applications nowadays, three-level inverter topologies are very attractive in comparison to two-level inverter topologies. Some of the advantages of these inverter topologies are lower semiconductor devices blocking voltage requirement hence lower switching loss, lower EMI (dv/dt) and reduced output filter requirement (lower converter footprint or higher power density) [1], [2]. But three-level inverter topologies have significant drawback: they suffer from dc-link capacitor voltage unbalance due to the mid-point modulation of the two series connected dc-link capacitors [3], [4]. This voltage imbalance between the upper and lower dc-link capacitors results in higher dc-link capacitor voltage ripple, higher output current harmonics and uneven semiconductor device voltage stress (reliability issue). Therefore, the NP voltage oscillation should be eliminated to have balanced voltage among the lower and upper capacitors and improve the performances of three-level inverter topologies.

Many dc-link capacitor voltage balancing strategies have been proposed in literatures for three-level inverter topologies. In [5] and [6], carrier based dc-link capacitor voltage balancing is proposed by adding offset voltage signal to the sinusoidal reference signals. The required offset voltage signal is determined using either feedback control or analytical calculation using the sensed neutral point potential oscillation and neutral point current direction. But this method has good effectiveness only for low modulation indices [7]. It has poor effectiveness for higher modulation index values due to the low frequency harmonics in the neutral point potential. There will be low-frequency ripple in the dc-link capacitor voltages and in the line-to-line output voltages for high modulation indices. Because of this Space Vector Modulation (SVM) based capacitor voltage balancing strategies are mostly preferred for three-level inverter topologies.

The Nearest Three Vectors space vector modulation [8] –[10] is the widely chosen SVM strategy for 3L inverters. In this SVM strategy, the location of the reference voltage vector is first identified and then three closest vectors are selected. The effective duty ratio of the three phase legs are then calculated using volt-second balance principle from the reference voltage vector and the three-nearest space vectors. One small space vector is used in each switching sequence and the dwell time of the negative and positive small vector is adjusted based on the NP current direction and the NP potential deviation to achieve capacitor voltage balancing. But this modulation strategy is very complex resulting in larger code size and execution time.

Control code execution time is critical for feedback control performance in grid-connected inverters. To achieve synchronization between grid current sampling and PWM pulses, the grid current sampling frequency is usually made to be equal to the switching frequency of the inverter [11], [12]. In padé approximation of delays [13], the modulator delay is equal to half of the switching period, therefore the delay due to ADC sampling, feedback control and space vector modulation code execution has to be less than half of the switching period to achieve synchronization. Therefore, for high switching frequency applications, the control code execution delay must be very small to fulfill this synchronization requirement.

In [14]-[17] improved SVM methods using decomposition of space vector diagrams are introduced to minimize the mathematical burden of 3L SVMs. These modulation strategies

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transform the 3L SVD into 6 smaller 2L SVDs and the two-level SVM strategy is then used. Therefore, the need for subsector (region) identification is eliminated. In addition, the vector dwell time computation for two-level inverters is much simpler than that of three-level SVM strategies. Therefore, these space vector modulation strategies result in significant code execution time reduction compared to the widely used 3L SVM strategy. However, neutral-point voltage control (avoiding voltage imbalance for the dc capacitors) is a difficulty for those modulation algorithms. The traditional voltage balancing technique using 3L SVM (using small vector dwell time redistribution) cannot be directly used. The 3L redundant small vectors are not available in 2L SVD. Due to this, capacitor voltage imbalance remained a significant problem for 3L SVM strategies using two-level SVM method.

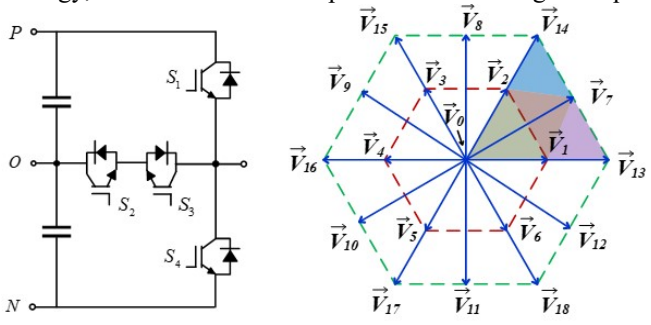
This paper introduces a modified neutral-point voltage control (voltage balancing strategy) for three-level inverters using space vector diagram decomposition and dwell time redistribution of the two-level zero space vectors. Based on the neutral point current direction and the deviation of the neutral-point (NP) potential, it readjusts the dwell times of the zero space vectors in 2L SVD to equalize the discharging and charging times of the two capacitors. It has a slightly higher neutral-point voltage ripple and output voltage harmonics compared to the commonly used 3L SVM capacitor voltage balancing strategy discussed in [9] but, it achieves much lower switching loss, code size and execution time.

II. Review of 3L SVM Strategies

A. Conventional SVM Strategy

Three-level VSI contain three switching states [P], [O], and [N] as shown in Fig. 1 (a) that yield 27 different combinations of switching states accounting all the three phases. These switching states provide 19 distinct space vectors distributed across two concentric hexagons as shown in Fig. 1 (b). These two hexagons make the space vector diagram of three level inverters. The space vectors are classified into four types: zero vectors located at the center of the hexagons, small vectors located at the inner hexagon vertices, medium vectors located half way between the vertices of the outer hexagon and large vectors located at the vertices of the outer hexagon. Table I shows the list of space vectors for three-level inverters [18]-[20].

In the Nearest Three Vectors (NTV) space vector modulation strategy, the 3L SVD is decomposed into six triangular equal sectors and 24 subsectors (regions). According to the information of where the reference vector is located, three space vectors that are closest to each other are picked, and their corresponding dwell times are calculated using the principle of volt-second balance, (1).



(a) (b)

Fig. 1. Topology and space vector diagram of three-level T-type inverter.(a) topology structure, (b) space vector diagram.

$$\begin{cases} \vec{V}_1 T_1 + \vec{V}_2 T_2 + \vec{V}_0 T_0 = \vec{V}_{ref} T_S \\ T_1 + T_2 + T_0 = T_S \end{cases} \quad (1)$$

Fig. 2 shows the space vectors and their corresponding dwell times for region 1 of sector 1 as an example. By individually considering the imaginary part and the real part of (1), the three space vectors dwell times are determined. Table II gives the vector dwell time expressions for sector one. The same expression can be used for other sectors too but the reference voltage angle (θ) must be converted to the range[0, π/3].

After the dwell times of the three nearest space vectors are calculated, appropriate switching sequence based on the specific control objective is used to determine the switching-on and switching-off times of each inverter phases. Fig. 3 shows an example of a seven-segment switching sequence and its corresponding phase output voltages. In this SVM strategy, voltage regulation for the dc link capacitors is realized by redistributing the dwell times of the redundant small vectors.

TABLE I
LIST OF THREE-LEVEL SPACE VECTORS

Space Vector		Switching State	Magnitude
$\vec{V}_0$		PPP, OOO, NNN	0
$\vec{V}_1$	$\vec{V}_{1P}$	POO	$\frac{1}{3}V_{dc}$
	$\vec{V}_{1N}$	ONN	
$\vec{V}_2$	$\vec{V}_{2P}$	PPO	
	$\vec{V}_{2N}$	OON	
$\vec{V}_3$	$\vec{V}_{3P}$	OPO	
	$\vec{V}_{3N}$	NON	
$\vec{V}_4$	$\vec{V}_{4P}$	OPP	
	$\vec{V}_{4N}$	NOO	
$\vec{V}_5$	$\vec{V}_{5P}$	OOP	
	$\vec{V}_{5N}$	NNO	
$\vec{V}_6$	$\vec{V}_{6P}$	POP	
	$\vec{V}_{6N}$	ONO	
$\vec{V}_7$		PON	$\frac{\sqrt{3}}{3}V_{dc}$
$\vec{V}_8$		OPN	
$\vec{V}_9$		NPO	
$\vec{V}_{10}$		NOP	
$\vec{V}_{11}$		ONP	
$\vec{V}_{12}$		PNO	
$\vec{V}_{13}$		PNN	$\frac{2}{3}V_{dc}$
$\vec{V}_{14}$		PPN	
$\vec{V}_{15}$		NPN	
$\vec{V}_{16}$		NPP	
$\vec{V}_{17}$		NNP	

TABLE II
THREE LEVEL SPACE VECTORS DWELL TIME CALCULATION FOR SECTOR ONE [19].

Region	T_1		T_2		T_0	
1	$\overrightarrow{V_1}$	$T_S\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$	$\overrightarrow{V_2}$	$T_S\left[2m_a\sin\theta\right]$	$\overrightarrow{V_0}$	$T_S\left[1-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$
2	$\overrightarrow{V_1}$	$T_S\left[1-2m_a\sin\theta\right]$	$\overrightarrow{V_2}$	$T_S\left[1-2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$	$\overrightarrow{V_7}$	$T_S\left[2m_a\sin\left(\frac{\pi}{3}+\theta\right)-1\right]$
3	$\overrightarrow{V_1}$	$T_S\left[2-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$\overrightarrow{V_{13}}$	$T_S\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)-1\right]$	$\overrightarrow{V_7}$	$T_S\left[2m_a\sin\theta\right]$
4	$\overrightarrow{V_{14}}$	$T_S\left[2m_a\sin\theta-1\right]$	$\overrightarrow{V_2}$	$T_S\left[2-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$\overrightarrow{V_7}$	$T_S\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$

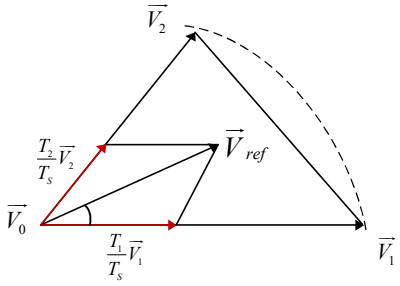


Fig. 2. Voltage vectors and their corresponding dwell times.

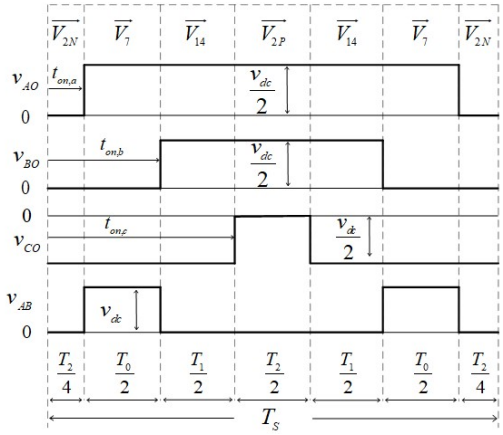


Fig. 3. seven-segment switching sequence for V_{ref} in sectorl-4

As can be seen from the figure, the dwell time of the small vector (V_2) is allocated equally between the two small vectors (V_{2P}) and (V_{2N}) to realize capacitor voltage regulation.

B. 3L SVM Based on SVD Decomposition

In these modulation strategies, the 3L SVD is transformed into 6 small 2L SVDs as depicted in Fig. 4. One small hexagon is chosen depending on the polarities of the input sinusoidal voltages as shown in Fig. 5. It is then shifted to the origin of the outermost hexagon. After this, transformation of the space vector diagram is done by subtracting $V_{dc}/3$ from the reference voltage vector (V_{ref}).

$$V'_{ref} = V_{ref} - \frac{V_{dc}}{3}\angle(n-1)\frac{\pi}{3} \tag{2}$$

where, V'_{ref} is in two-level SVD, V_{ref} is in three-level SVD, and n is the sector number.

After one small hexagon is selected and the reference vector is transformed, the conventional 2L SVM strategy is applied in order to calculate the effective duty ratios of the inverter phase legs. Based on the transformed reference vector location, three-nearest two-level space vectors are used to produce the transformed reference vector. The complete list of the two-level space vectors is shown in Table III. The two-level vectors dwell times are similarly determined using the principle of volt second equivalency (balance) shown in (3).

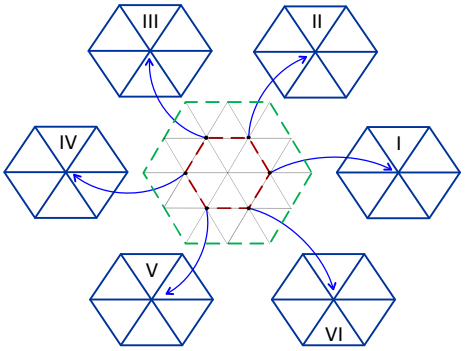


Fig. 4. Decomposition of 3L SVD into equivalent 2L SVDs.

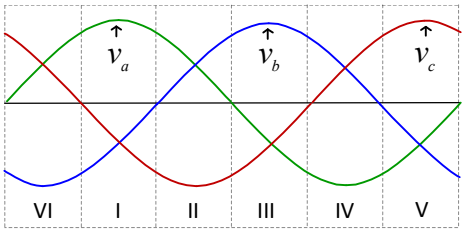


Fig. 5. Method for identification of sector for hexagon selection.

TABLE III
LIST OF TWO-LEVEL SPACE VECTORS.

Space Vector		Switching State	Definition
Zero Vector	$\vec{V}_0$	PPP OOO	$\vec{V}_0 = 0$
Active Vector	$\vec{V}_1$	POO	$\vec{V}_1 = \frac{2}{3}V_d e^{j0}$
	$\vec{V}_2$	PPO	$\vec{V}_2 = \frac{2}{3}V_d e^{j\frac{\pi}{3}}$
	$\vec{V}_3$	OPO	$\vec{V}_3 = \frac{2}{3}V_d e^{j\frac{2\pi}{3}}$
	$\vec{V}_4$	OPP	$\vec{V}_4 = \frac{2}{3}V_d e^{j\pi}$
	$\vec{V}_5$	OOP	$\vec{V}_5 = \frac{2}{3}V_d e^{j\frac{4\pi}{3}}$
	$\vec{V}_6$	POP	$\vec{V}_6 = \frac{2}{3}V_d e^{j\frac{5\pi}{3}}$

$$\begin{cases} T_1 = \dfrac{2\sqrt{3}T_S V_{ref}^{'}}{V_{dc}} \sin\left(\dfrac{\pi}{3} - \theta\right) \\ T_2 = \dfrac{2\sqrt{3}T_S V_{ref}^{'}}{V_{dc}} \sin\theta \\ T_0 = T_S - T_1 - T_2 \end{cases} \quad \text{for } 0 \le \theta < \pi/3 \qquad (3)$$

Compared to the three-level space vector dwell time calculation procedure, the two-level space vector dwell time calculation is very simple hence it helps to reduce the computational burden of these SVM strategies.

III. Proposed Capacitor Voltage Balancing Strategy

Three-level inverters can be considered as a composition of two two-level inverters evident from Fig. 6. Looking at the figure, the three-level [P] state is equivalent to the upper two-level [P] switching state; the three-level [O] switching state is equivalent to the upper two-level [O] switching state and the lower two-level [P] switching state and the three-level [N] switching state is equivalent to the lower two-level [O] switching state. During the positive half cycle of the three-level reference voltage, the switches (S_1 and S_3) modulate the upper dc-link capacitor. Therefore, the upper two-level inverter is used when the three-level reference voltage is positive. On the other hand, when the three-level reference voltage is negative, the switches (S_2 and S_4) modulate the lower dc-link capacitor. Hence the lower two-level inverter is used when the polarity of the three-level reference voltage is negative. The polarity of the three level sinusoidal reference voltages determines the sector number of the 3L SVD as shown in Fig. 5. Therefore, the information that which of the two-level inverters must be used can be determined from the three-level sector number. Table IV shows the relationship between the two-level inverters and the three-level sector numbers.

The 3L space vectors can be converted into smaller 2L space vectors using the relationship between the three-level switching states [P, O, N], the two-level switching states [P, O] and three-level sector number. When one small hexagon is selected and moved to the center of the inner/outer hexagon, the space vectors located at the center of the small hexagon will be transformed into the space vectors located at the center of the inner/outer hexagon, and the space vectors located at the vertices of the small hexagon will be transformed into the space vectors located at the vertices of the inner hexagon. Fig. 7(a)

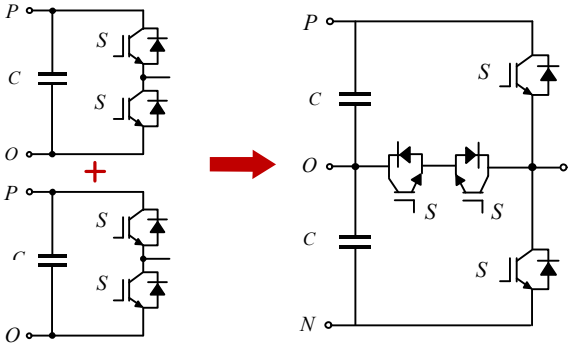


Fig. 6. Derivation of three-level T-type inverter from two half-bridge inverter cells.

TABLE IV
RELATIONSHIP BETWEEN MAIN SECTOR NUMBER AND THE TWO-LEVEL INVERTERS.

Sector	Inverter Phase		
	Phase A	Phase B	Phase C
1	Upper	Lower	Lower
2	Upper	Upper	Lower
3	Lower	Upper	Lower
4	Lower	Upper	Upper
5	Lower	Lower	Upper
6	Upper	Lower	Upper

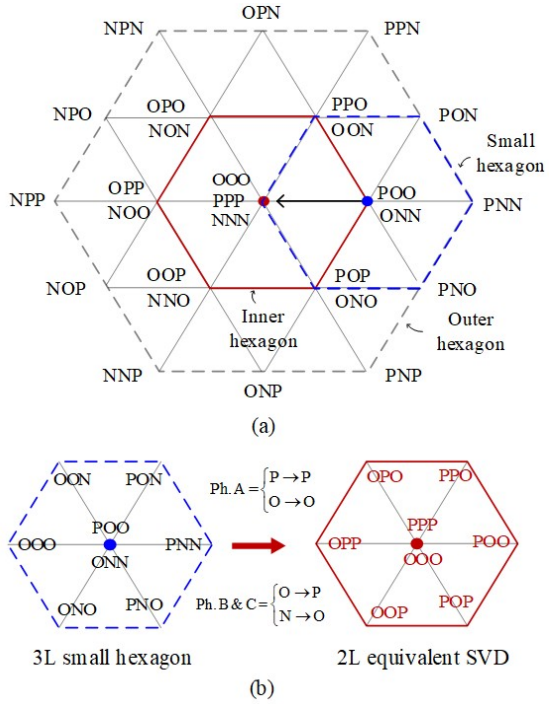


Fig. 7. (a) small hexagon selection, (b) space vector diagram transformation for sector 1.

illustrates the space vector diagram transformation process for sector 1. In this sector, Phase A uses the upper two-level inverter while the other two phases (Phase B and Phase C) use the lower two-level inverter. Therefore, the three-level [P] switching state translates to the two-level [P] switching state and the three-level [O] switching state translates to the two-level [O] switching state for Phase A. For the other two phases, the three-level [O] switching state translates to the two-level [P] switching state and the three-level [N] switching state translates to the two-level [O] switching state.

Even though there are redundant space vectors at some vertices of the small hexagons, only one of these redundant space vectors is valid for space vector diagram transformation. The three level space vector that is needed for the space vector diagram transformation is selected from the redundant space vectors based on the three-level sector number. For sector 1 for example, the polarity of the phase A reference voltage is positive and the polarity of the other two reference voltages is negative. The switching states of Phase A can be either [P] or [O] but the switching states of the other two states should be either [O] or [N]. Therefore, the three-level space vectors

satisfying this combination should be used. Fig. 7 (b) shows the valid three-level space vectors for the three-level small hexagon and the corresponding equivalent two-level space vectors for sector 1. The three-level space vectors for the other sectors can be similarly converted into the smaller two level space vectors using the same procedure. The resulting two-level space vectors will be the same; only the position of the transformed reference vector will be different for the other sectors. After, the 3L SVD is transformed into the equivalent 2L SVD, the commonly used 2L SVM strategy is applied. Table V shows the switching sequences of the conventional two-level SVM strategy [27].

TABLE V
SWITCHING SEQUENCE OF THE 2L SVM STRATEGY[27]

Sector	Switching sequence
1	OOO→POO→PPO→PPP→PPO→POO→OOO
2	OOO→OPO→PPO→PPP→PPO→OPO→OOO
3	OOO→OPO→OPP→PPP→OPP→OPO→OOO
4	OOO→OOP→OPP→PPP→OPP→OOP→OOO
5	OOO→OOP→POP→PPP→POP→OOP→OOO
6	OOO→POO→POP→PPP→POP→POO→OOO

When the 3L SVD is decomposed into the equivalent 2L SVDs, the 3L small vectors are converted to the 2L zero space vectors ([PPP] and [OOO]) since the magnitude of the 3L small vectors is $V_{dc}/3$. Therefore, voltage balancing for the dc-link capacitors can be achieved by utilizing the 2L zero space vectors. Table VI shows the relationship between the 2L zero space vectors and the three-level redundant small vectors for different sectors. It can be seen from the table that the two-level zero space vector [OOO] is equivalent to the three-level negative small vectors and the two-level zero space vector [PPP] is equivalent to the three-level positive space vectors.

Fig. 8 shows a three-level inverter equivalent circuit when [PPP] and [OOO] are used. When [PPP] is applied to the inverter as shown in Fig. 8 (a), the upper dc-link capacitor is connected to the inverter terminals. When the neutral point current flows into the neutral point (i_{NP} is negative), the upper dc-link capacitor voltage decreases while the lower dc-link capacitor voltage increases. On the other hand, when the neutral point current flows out of the neutral point (i_{NP} is positive), the upper capacitor voltage increases and the lower capacitor voltage decreases. When [OOO] is used to the inverter as shown in Fig. 8 (b), the lower dc-link capacitor is clamped to the inverter terminals. The opposite result occurs for the dc-link capacitor voltages when this switching state is used.

In this paper, the local two-level zero space vectors' dwell time distribution is rearranged (as shown in Fig. 9) according to (4) – (7) to achieve voltage balancing for the dc-link capacitors. When the upper capacitor voltage is greater than the lower capacitor voltage, the neutral point voltage error (Δu) will be positive. The time allocated to the [PPP] zero space vector is reduced if the neutral point current is positive (the neutral point current is flowing out of the neutral point), and the time allocated to the [PPP] zero space vector is increased if the neutral point current is negative (the neutral point current is flowing into the neutral point). On the other hand, when the upper dc-link capacitor voltage is less than the lower dc-link capacitor voltage, the neutral point voltage error will be negative. In this case, the time allocated to the [PPP] zero space vector is increased for positive neutral point current and the time allocated to the [PPP] zero space vector is decreased for negative neutral point current.

TABLE VI
RELATIONSHIP BETWEEN THE TWO-LEVEL ZERO SPACE VECTORS AND THE THREE-LEVEL SMALL SPACE VECTORS

Zero space vectors	Three-level small vector for sectors					
	1	2	3	4	5	6
OOO	ONN	OON	NON	NOO	NNO	ONO
PPP	POO	PPO	OPO	OPP	OOP	POP

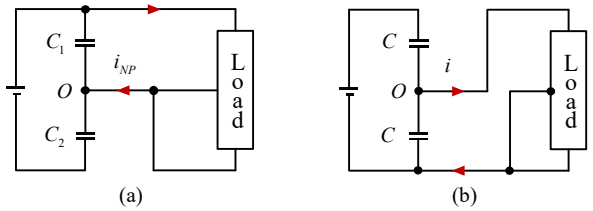


Fig. 8. Equivalent circuits of two-level zero space vectors: (a) when [PPP] is used, (b) when [OOO] is used.

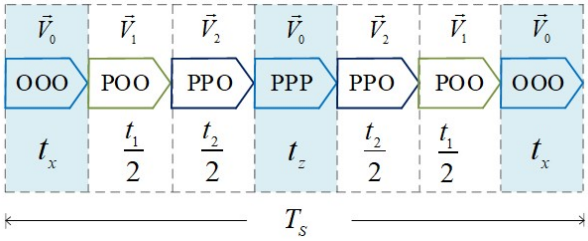


Fig. 9. The proposed capacitor voltage balancing strategy using zero-space vector dwell time redistribution.

$$t_x = \frac{(1-\Gamma\Delta u)}{4} T_0 \tag{4}$$

$$t_z = \frac{(1+\Gamma\Delta u)}{2} T_0 \tag{5}$$

$$\Delta u = \frac{v_{c1} - v_{c2}}{2} \tag{6}$$

$$\Gamma = \begin{cases} 1, & i_{NP} < 0 \\ -1, & i_{NP} > 0 \end{cases} \tag{7}$$

where v_{c1}, v_{c2} are the lower and upper capacitor voltages respectively, Δu is the neutral-point potential error, and Γ is the neutral point current polarity indicator.

The polarity of the neutral point current (i_{NP}) is determined from its average value for one switching cycle as shown in (8).

$$i_{NP} = d_{ao} i_a + d_{bo} i_b + d_{co} i_c \tag{8}$$

where d_{ao}, d_{bo} and d_{co} represent the average duty cycles of the [O] switching states for the three inverter phases given by (9).

$$d_{xo} = \begin{cases} 1-u_x & u_x \geq 0 \\ 1+u_x & u_x < 0 \end{cases} \quad x \in \{a,b,c\} \tag{9}$$

where u_a, u_b and u_c are the transformed three phase reference

voltage signals in two-level space vector diagram.

In summary the main contributions of this paper are:

- Detailed analysis and description of the relationship between the three-level space vectors and the local two-level space vectors for 3L SVM strategies based on SVD decomposition.
- Illustration of the 2L zero space vectors effects on the neutral-point potential of three-level inverters.
- A new voltage balancing strategy for dc-link capacitors for three-level inverters using space vector diagram decomposition.

IV. Performance Comparison

The proposed voltage balancing strategy performance is studied in simulation in MATLAB and comparison is carried out with the performance indexes of the widely used 3L SVM based NP voltage control technique presented in [9]. The space vector modulation strategy in [9] is taken as a standard strategy for comparing performance due to its lower switching losses and lower voltage ripple of the neutral point compared to other three level SVM strategies such as [21] – [23]. There are some techniques proposed for neutral-point voltage ripple reduction such as [24], [25] but they produce high switching loss.

The system specifications for this investigation are: $V_{dc} = 800$ V, $P_{rated} = 20$ kW, $V_{out} = 480$ V (rms) and $C_{dc} = 200$ μF. For studying the output current ripple for grid applications, an LCL filter with inverter side inductance of 200 μH, grid side inductance of 50 μH, filter capacitance of 10 μF, and damping resistance of 0.3 Ω is used. These parameters are determined according to the design guideline presented in [26].

A. Neutral-point (NP) Voltage Ripple

The traditional 3L SVM based NP voltage control technique uses the dual small vectors (positive and negative) to minimize the NP voltage deviation. The small space vectors are used at the beginning, middle and end of the switching sequence as shown in Fig. 10. The small space vectors dwell times are redistributed depending on the magnitude of the neutral point potential deviation and the direction of the neutral point current to minimize the voltage imbalance between the two capacitors. The voltage balancing strategy proposed in this paper also uses a similar approach to suppress the neutral point voltage deviations. But it rather uses the two-level zero space vectors (which are equivalent to the three-level small vectors) at the beginning, middle and end of the switching sequence as shown in Fig. 9. Similar to the traditional 3L SVM capacitor voltage balancing method, it also uses active dwell time distribution method for the two zero space vectors.

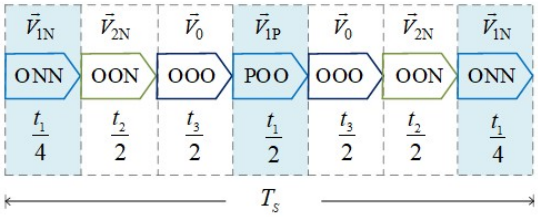


Fig.10. The conventional 3L SVM strategy switching sequence in sector 1 and region 1.

The dwell time distribution between the two-level [OOO] and [PPP] zero space vectors depend on the neutral point voltage deviation and the NP current direction as shown in (4) – (7). However, the voltage balancing method proposed in this paper has slightly higher NP potential ripple in comparison with the commonly used 3L SVM based NP voltage control technique in [9]. This is because the traditional 3L SVM capacitor voltage balancing method has better neutral point voltage regulation when the reference vector is in region one and two due to the availability of two redundant small space vectors in these regions. In the capacitor voltage balancing strategy proposed in this paper, both three-level small space vectors transform to a single two-level zero space vector pairs hence the space vector redundancy disappears.

Fig. 11 shows the magnitude of the estimated (estimated using Matlab/Simulink simulation) NP potential ripple for the commonly used 3L SVM capacitor voltage balancing strategy and the capacitor voltage balancing strategy proposed in this paper for different operating conditions. The figure shows that the modified voltage balancing method has slightly higher NP voltage ripple in comparison to the traditional 3L SVM method for capacitor voltage balancing.

B. Output Voltage Harmonics

In the traditional 3L SVM strategy when the reference voltage vector is in region 1 or 2, two of the three nearest space vectors are small space vectors. These redundant small vectors are used to remove the even-order harmonics from the output inverter voltages in addition to dc-link capacitor voltage balancing. To accomplish this objective, regions one and two are further divided into two sections (Fig. 12) and the small vector closer to the reference voltage vector is used for neutral point voltage control in each section. For example, when the reference voltage vector is in region 1a, $\vec{V}_1$ is used for balancing capacitor voltage as shown in Fig. 13 (a) and $\vec{V}_2$ is used for balancing capacitor voltages when the reference voltage vector is in region 1b as shown in Fig. 13 (b).

In the proposed dc-link capacitor voltage balancing strategy when one small hexagon is selected and transformed into an equivalent two-level space vector diagram, the three-level small vector located at the center of the small hexagon is transformed into the two-level zero space vectors. Therefore, only one type of small vector is technically used for dc-link capacitor voltage balancing in this neutral point voltage control technique. Because of this, the modified neutral point voltage control technique proposed in this paper lacks the even order harmonic elimination capability that the conventional 3L SVM voltage balancing technique has. Hence it has slightly higher output voltage harmonic content. Fig. 14 shows the output voltage harmonic spectrum for the conventional 3L SVM capacitor voltage balancing method and the proposed capacitor voltage balancing method. The figure shows that voltage balancing method proposed in this paper has slightly higher output voltage harmonics compared the traditional 3L SVM voltage balancing strategy.

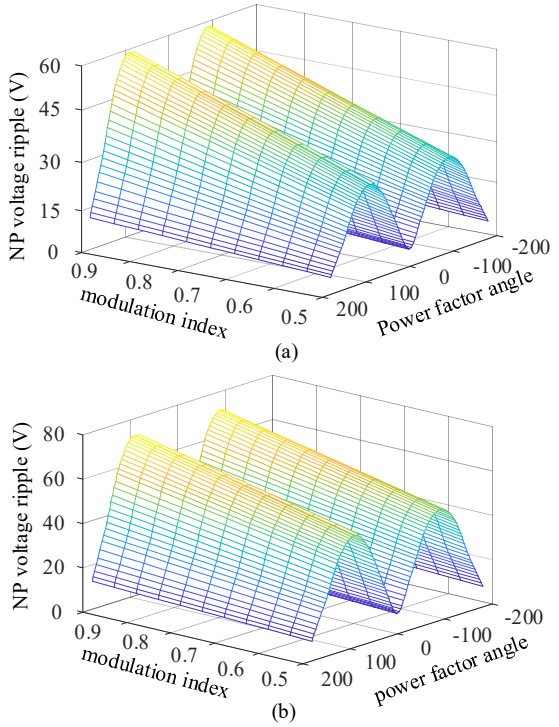


Fig. 11. Peak-to-peak NP potential ripple: (a) commonly used 3L SVM voltage balancing technique in [9], (b) proposed capacitor voltage balancing method.

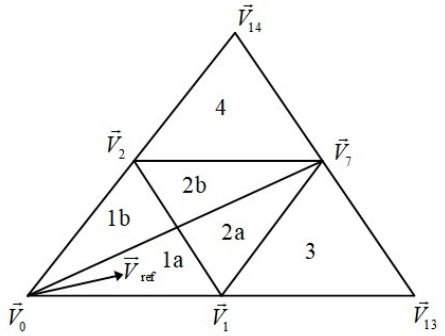


Fig. 12. Sector division (Sector 1) for minimization of even-order harmonics.

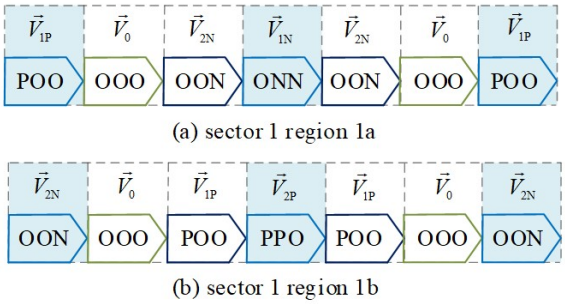


Fig. 13. Switching sequence of the conventional capacitor voltage balancing method in sector 1 and region 1.

C. Switching Loss

The modified voltage balancing method introduced in this paper uses a symmetrical switching sequence with only two switchings per switching cycle. The commonly used 3L SVM voltage balancing technique also has two switchings per switching cycle. But it has higher number of switchings per fundamental line cycle compared to the capacitor voltage balancing technique proposed in this paper because of the extra switchings in region one and region two for even-order harmonic elimination. This capacitor voltage balancing technique alternatively uses the two available small vectors in region one and two to eliminate the even-order harmonics besides to the capacitor voltage regulation thereby involving additional switching actions. Therefore, the capacitor voltage balancing technique proposed in this paper has lower switching loss in comparison with the traditional 3L SVM based NP voltage control technique.

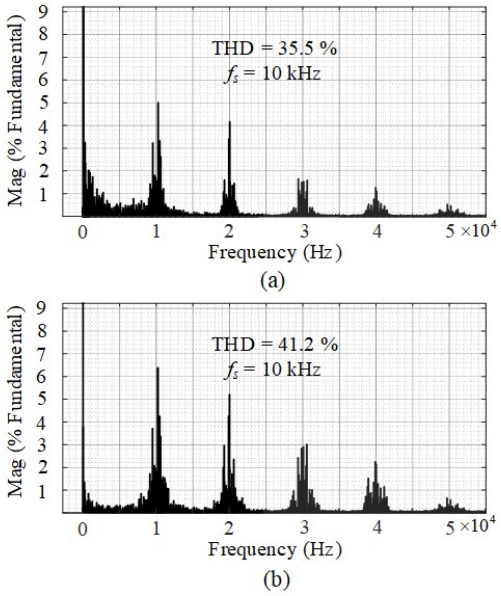


Fig. 14. Harmonic spectrum of the output voltage for different voltage balancing methods: (a) conventional 3L SVM based balancing (b) Modified voltage balancing introduced in this paper.

The switching losses of the semiconductor devices for the traditional SVM capacitor voltage balancing method and the capacitor voltage balancing technique proposed in this paper are estimated for different operating conditions using PLECS electrothermal simulation. An Infineon 1200 V, 25 A Si IGBT (IGW25N120H3) is used for the switches. Fig. 15 shows the estimated semiconductor device switching losses of the two

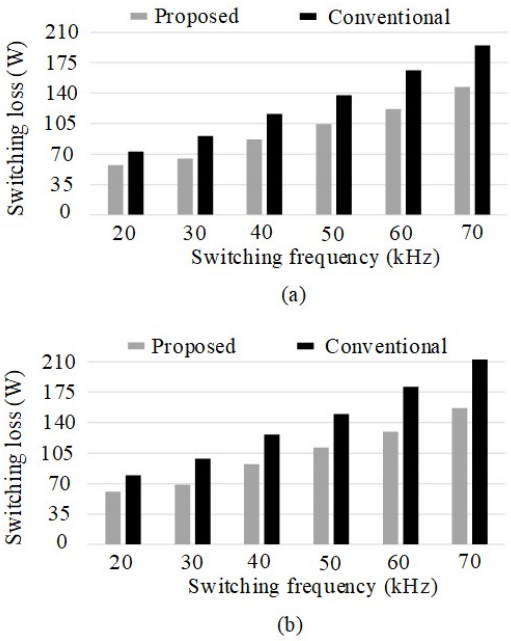


Fig. 15. Estimated switching loss: (a) pf = 1, (b) pf = 0.8 (lag).

voltage balancing techniques for different load operating conditions. The figure shows that the capacitor voltage balancing technique proposed in this paper has lower switching loss than the traditional 3L SVM capacitor voltage balancing technique.

D. Code execution time

Both the traditional 3L SVM neutral point voltage control technique and the modified neutral point voltage control technique proposed in this paper are implemented in TI Delfino DSP (TMS320F28335). Their code computation time is measured using the Code Composer Studio (CCS) execution time profiling tool. Fig. 16 shows the measured code execution time for the commonly used 3L SVM based neutral point voltage control method and the proposed dc-link capacitor voltage balancing method. The proposed dc-link capacitor voltage balancing method has lower code size and execution time because of its simplicity in the overall algorithm and space vector dwell time calculation. This offers two benefits: reducing the control hardware requirement and providing better stability for control of grid-connected inverters.

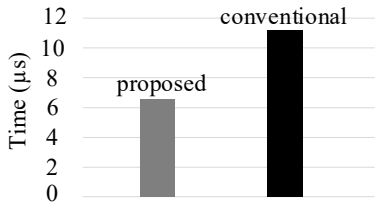


Fig. 16. Measured execution time for the voltage balancing method proposed in this paper and the commonly used 3L SVM voltage balancing method.

E. Dynamic Performance

The dynamic performance of the capacitor voltage balancing technique proposed in this paper is studied using Matlab simulation for step change in modulation index. The simulation investigation is carried out using a three-level T-type inverter with the specifications: rated power (P_{rated}) = 20 kW, dc bus voltage (V_{dc}) = 800 V, output voltage (V_{out}) = 480 V, dc-link capacitor (C_{dc}) = 200 μF. Fig. 17 shows the load currents, load voltages, and dc-link capacitor voltages for the proposed dc-link capacitor voltage balancing strategy for a step change in modulation index from 1.0 to 0.6. When the modulation index decreases, the reference voltage vector magnitude also decreases. Therefore, the magnitude of the output voltage and output current as well as the neutral point voltage ripple will also reduce. The capacitor voltage balancing technique proposed in this paper has a very good dynamic performance – the output voltage and output current magnitude quickly changes when the modulation index changes without introducing transient disturbance.

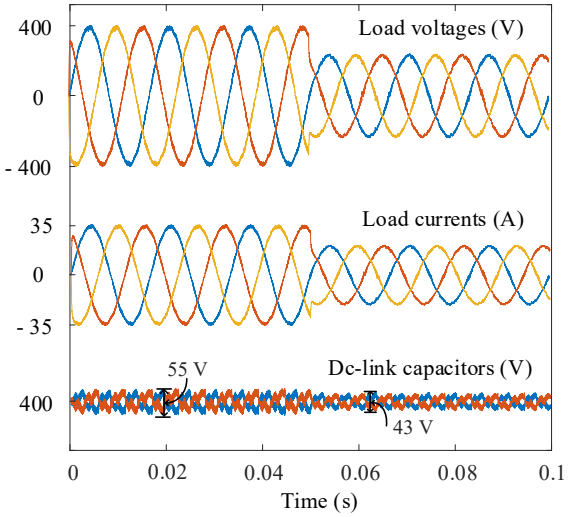


Fig. 17. Transient response of the proposed dc-link capacitor voltage balancing method to step change in modulation index from 1.0 to 0.6.

V. Experimental Results

The capacitor voltage balancing technique proposed in this paper is validated by experimental test of a 10 kW, 480 V inverter. Fig. 18 shows the experimental test setup. A modulation index of 0.9 is used for the experimental test. Texas Instruments Delfino microcontroller (TMS320F28335) is used to implement the control. The performance of the modified neutral point voltage control strategy introduced in this paper is compared with the performances of the commonly used 3L SVM voltage balancing method described in [9] and the natural sinusoidal pulse width modulation method without any dc-link capacitor voltage balancing technique. Fig. 19 presents the inverter output voltage and output current. The figure shows that the SVM method achieves the intended three level output waveforms. The dc-link capacitor voltages along with the inverter phase output voltage and output currents are shown in Fig. 20 for the traditional 3L SVM based NP voltage control technique, in Fig. 21 for the modified voltage balancing method, and in Fig. 22 for sinusoidal pulse width modulation method.

The figure shows that the capacitor voltage balancing technique proposed in this paper has slightly higher NP voltage

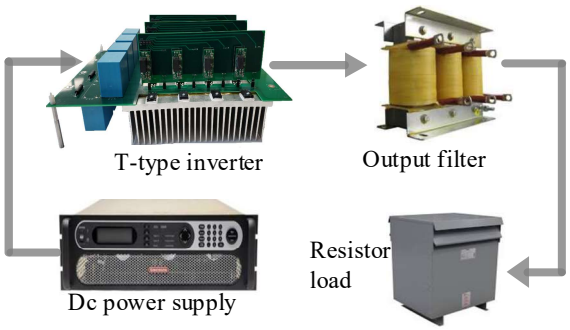


Fig. 18. Experimental test setup.

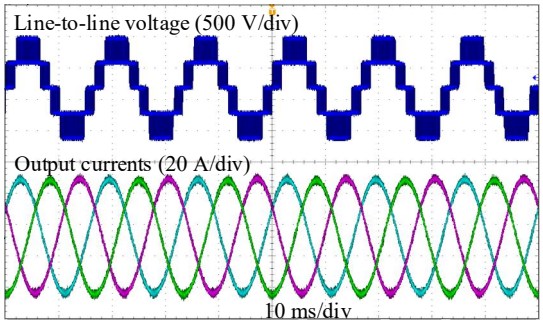


Fig. 19. Line to line voltage and three-phase line currents for the proposed capacitor voltage balancing method.

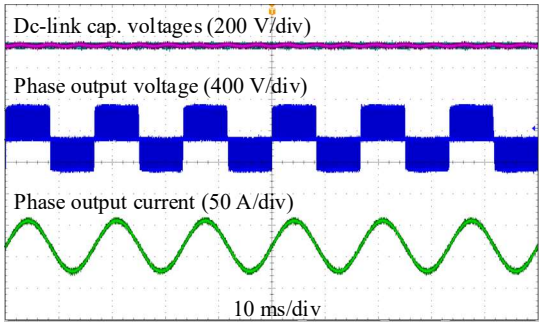


Fig. 20. Capacitor voltages and output waveforms for the commonly used SVM capacitor voltage balancing technique.

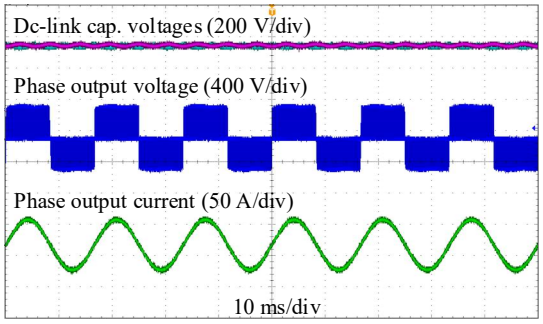


Fig. 21. Capacitor voltages and output waveforms for the capacitor voltage balancing technique proposed in this paper.

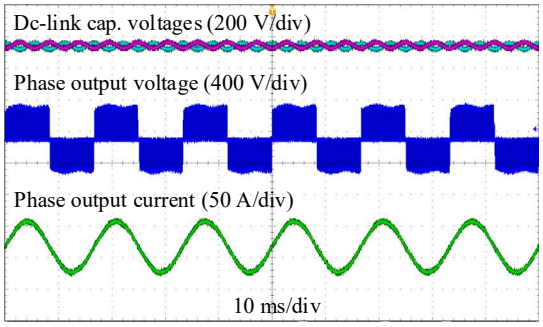


Fig. 22. Capacitor voltages and output waveforms for sinusoidal pulse width modulation (without balancing).

ripple in comparison with the commonly used 3L SVM based NP voltage control technique in [9] but the difference is not very large. But compared to the sinusoidal pulse width modulation method, it offers significantly smaller NP voltage ripple.

The transient performance of the proposed dc-link capacitor voltage balancing strategy is also verified by experiment as shown in Fig. 23. As can be seen from the figure, the proposed dc-link capacitor voltage balancing method has a very good transient performance. The performance of the proposed dc-link capacitor voltage balancing strategy to a change in the inverter operating condition is also experimentally verified. Fig. 24 shows the dynamic performance of the proposed dc-link capacitor voltage balancing method to a step change in modulation index from 1.0 to 0.6. The efficiency and THD performance of the proposed dc-link capacitor voltage balancing strategy is also verified by experiment. Fig. 25 shows comparison of the measured inverter efficiency values for different load conditions for the proposed and the conventional dc-link capacitor voltage balancing strategies. Fig. 26 shows comparison of the measured THD values of the output

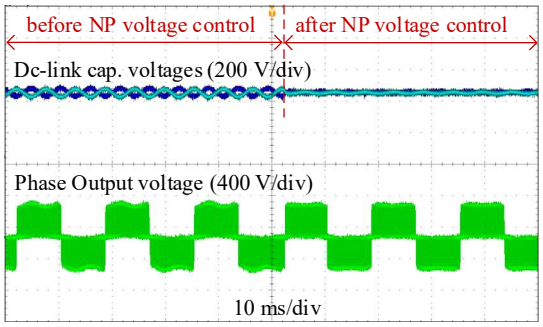


Fig. 23. Transient performance of the proposed dc-link capacitor voltage balancing method.

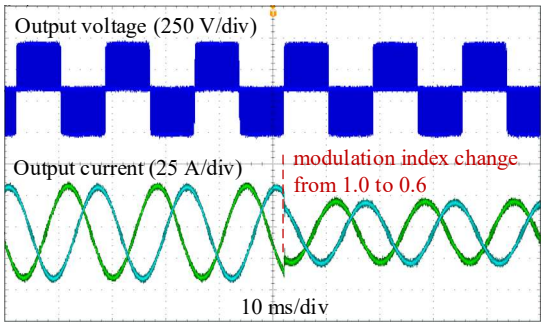


Fig. 24. Dynamic response of the proposed dc-link capacitor voltage balancing strategy to a step change in modulation index.

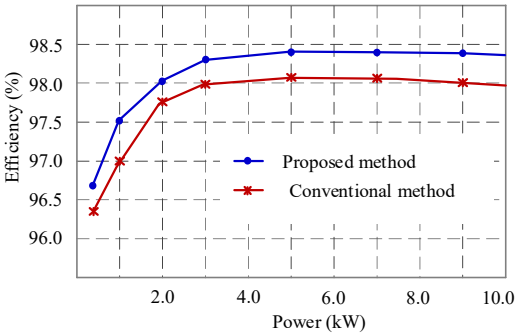


Fig. 25. Comparison of measured efficiency values for the proposed and the conventional dc-link capacitor voltage balancing strategies.

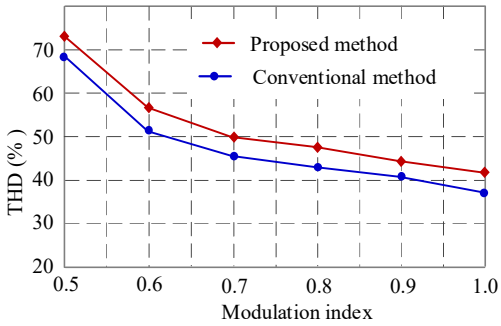


Fig. 26. Comparison of measured total harmonic distortion (THD) values for the proposed and the conventional dc-link capacitor voltage balancing strategies.

line-to-line voltage for the proposed and the conventional dc-link capacitor voltage balancing strategies.

In addition to its slightly higher neutral-point voltage ripple and output voltage harmonics, the proposed dc-link capacitor voltage balancing method has some limitations. One such limitation is the output voltage linearity. The linear operation range of this capacitor voltage balancing method is for modulation index values of ($m \in [0, 1]$). For higher modulation

index values, the output voltage gain will be nonlinear hence the output voltage THD will increase dramatically as shown in Fig. 27.

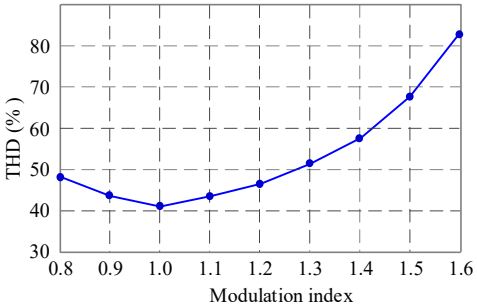


Fig. 27. Output voltage THD of the proposed capacitor voltage balancing method for higher modulation indices.

VI. CONCLUSION

This paper introduces a modified voltage balancing strategy for three level inverters using decomposition (transformation) of space vector diagrams. The modified voltage balancing method redistributes the dwell times of the 2L zero space vectors in accordance with the direction of the neutral-point current and the magnitude of the NP potential oscillation to eliminate the NP voltage oscillation (capacitor voltage imbalance). In comparison with the conventional 3L SVM based neutral point voltage control technique in [9] (the commonly used voltage balancing method), the modified voltage balancing method has slightly higher NP voltage ripple and output voltage harmonics. But, it has much lower switching loss compared to the traditional 3L SVM dc-link capacitor voltage balancing method due to its lower number of switching actions per fundamental cycle. Besides, it has also lower execution time and code size compared to the commonly used 3L SVM capacitor voltage balancing technique.

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