MMC-MTDC Transmission System with Partially Hybrid Branches

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Abstract—**This paper proposes a hybrid submodule modular multilevel converter (MMC) topology which is suitable for multi terminal direct current (MTDC) transmission systems. Each arm of the proposed MMC topology consists of a half-bridge submodule (HBSM) branch and two parallel full-bridge submodule (FBSM) branches. Comparing with the conventional MTDC transmission system, the proposed topology can selectively block the DC fault current and isolate the corresponding fault line without expensive DC circuit breakers (DCCBs). Thus, the influence range of the DC fault can be reduced and the reliability of the power supply can be improved as well. The corresponding modulation and voltage balancing strategies are developed for the proposed hybrid MMC topology. The feasibility of the proposed topology and control strategy is verified in the MATLAB/ Simulink simulation.**

Index Terms—**Hybrid modular multilevel converter, multi terminal networks, high voltage dc (HVDC) transmission.**

I. INTRODUCTION

NOWADAYS, HVDC transmission systems are widely adopted in the island-grid power connection, the non-synchronous grids interconnection, and distributed energy generation systems [1][2]. The growing demand for large-scale renewable energy delivery expands the transmission capacity and distance of MMC-MTDC systems [3][4].

At present, cables and overhead lines are two options for DC transmission lines in MTDC projects[5]. The cost of the DC transmission cable is higher and the cables are difficult to lay in some scenes [6]. Compared with cables, the failure rate of overhead lines is higher [7]. Thus, the DC fault detection and protection scheme of MMC-MTDC systems is of concern [8][9]. The DC fault detection methods are widely studied such as impedance calculations, rate of change of voltages and currents[10], overcurrent detection[11].

The DC fault blocking capability is necessary for the MTDC system to protect converters [12]. Many topologies and methods are dealing with the DC fault protection capabilities of the MTDC system, such as the HBSM-MMC with DCCBs [13][14], FBSM-MMC [3][15], and the hybrid MMC with HBSM and FBSM [2][16].

Setting a DCCB at each terminal of the MTDC system is one of the most common and effective DC grid protection strategies [14]. The fault current can be quickly isolated by DCCBs. However, this is at the expense of high economic investment and additional operational losses [17]. These obstacles limit its application to MTDC systems. Another DC fault blocking method is to equip submodules with fault clearance capabilities, such as FBSM, clamp-double submodule (CDSM), and so on [18]. As shown in Fig. 1, the fault current path of HBSM is different from that of FBSM, the fault current still flows through the diode after the HBSM is blocked. However, the current flows through the FBSM capacitor and charge it so that the diode is subjected to reverse voltage to cut off the fault current. Although the FBSM has the capability of dc fault clearance, it also increases module cost and switching losses [19]. Therefore, the hybrid MMC with HBSM and FBSM is proposed.

The hybrid MMC consists of FBSM and HBSM. By appropriately designing the ratio of FBSM and HBSM, the hybrid MMC maintains the DC fault blocking capacity while reducing the cost and power loss[20]. Since the hybrid MMC has the above advantages, there is much research on the hybrid MMC, such as the voltage balancing control[20][22], the fault ride-through process[21], and the reliability analysis[18].

However, the above researches focus on the hybrid MMC itself and did not pay attention to its application in the MTDC system. In the MTDC system, the main drawback of the hybrid MMC is that it cannot isolate the fault line, which often expands the impact range of the DC fault. In [23], a continuous operation strategy under DC fault was mentioned. However,
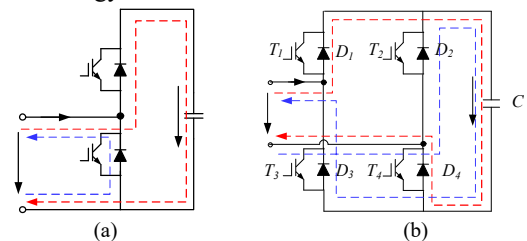
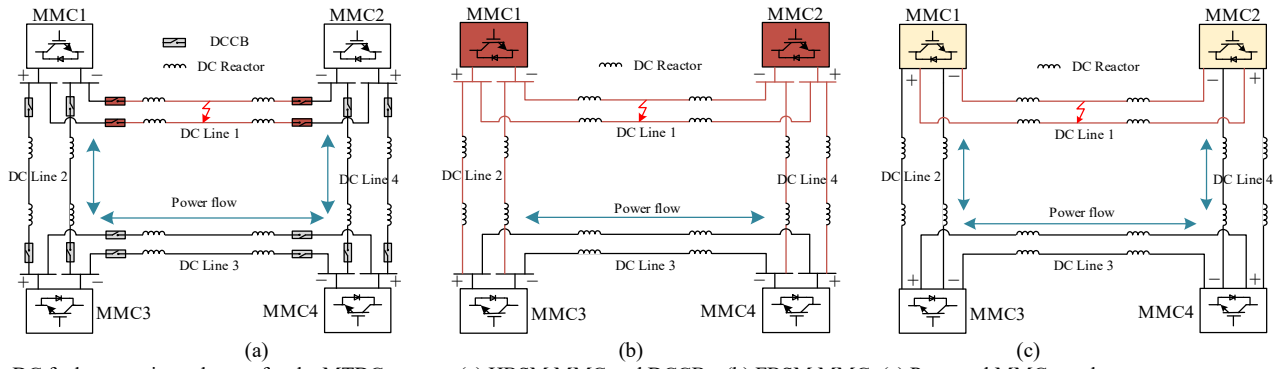Fig. 1. SM fault current path after blocking. (a) HBSM. (b) FBSM

Fig. 2. DC fault protection schemes for the MTDC system. (a) HBSM MMC and DCCBs; (b) FBSM MMC; (c) Proposed MMC topology.

this strategy still relies on DCCBs and the circuit breakers at the nodes present a challenge for protection control.

In order to overcome the above obstacles, this paper proposes a hybrid MMC topology that can reduce the influence range of line faults and improve the power supply reliability of MTDC transmission systems. As shown in Fig.2, if a pole-to-pole fault occurs on the DC line, the MTDC system will feed current to the fault point. When the overcurrent is detected, the fault protection of the MTDC system is activated. As shown in Fig. 2(a), for the MTDC system equipped with DCCBs, the fault current is blocked by DCCBs and the fault line is also isolated by DCCBs. Because of the aforementioned drawbacks of DCCBs, the MMC topology with fault blocking capability is also an alternative in the MTDC system. As shown in Fig. 2(b), the DC fault current can be interrupted after the FBSM-MMCs are blocked. Because MMC 1 and MMC 2 are blocked, the DC line 2 and DC line 4 cannot transmit power and the influence range of the DC line fault is expanded. With the proposed MMC topology, the fault on the DC line 1 can be blocked and isolated selectively. Comparing Fig. 2(b) and Fig. 2(c), we can see that the influence range of the DC fault can be reduced and the reliability of the power supply can be improved with the proposed MMC topology.

The rest of this paper is organized as follows: Section II presents the MMC topology with partially hybrid branches. In section III, the corresponding MMC station control strategy for the proposed hybrid MMC is presented. In Section IV, the

proposed topology and control strategies are validated by simulation results. Section V presents the topology comparison result of different MTDC protection schemes. Finally, the concluding remarks are provided in Section VI.

II. PROPOSED HYBRID MMC TOPOLOGY

The proposed hybrid MMC topology is shown in Fig. 3. The parallel FBSM branches are connected to the DC line 1 and the DC line 2. The components of the FBSM branch 1 are indicated by subscript 1 and the components of the FBSM branch 2 are indicated by subscript 2. The parameters and variables of the proposed MMC topology are shown in Table I. The resistance of the arm is not considered in the analysis and the arm inductance is recorded as L_0. v_{pj} is the sum of the inserted HBSM voltages on the upper arm of phase j and v_{nj} is the sum of the inserted HBSM voltages on the lower arm of phase j, where j denotes the AC phase and $j \in \{a, b, c\}$. The voltage of the FBSM branch 1 is expressed as v_{pj1} or v_{nj1} and the voltage of the FBSM branch 2 is expressed as v_{pj2} or v_{nj2}. The current flowing through each branch is similarly marked.

As shown in Fig. 3, the relationship of the FBSM branch 1 variables can be derived as follows.

TABLE I

THE PROPOSED HYBRID MMC PARAMETERS

Parameters	Symbols
AC rated voltage amplitude	V_g
DC line rated voltage	V_{dc1}, V_{dc2}
Rated active power of DC lines	P_{ref1}, P_{ref2}
Rated reactive power of DC lines	Q_{ref1}, Q_{ref2}
SM number of a HB branch	N_H
SM number of FB branches	N_{F1}, N_{F2}
HBSM capacitance	C_{smh}
FBSM capacitance	C_{smf1}, C_{smf2}
HBSM rated voltage	U_{smh}
FBSM rated voltage	U_{smf1}, U_{smf2}
Arm inductance	L_0
DC line reactor	L_d
Capacitor voltage ripple rate	ξ

Fig. 3. The MMC topology with partially hybrid branches.

$$L_0 \frac{di_{pj}}{dt} + L_0 \frac{di_{pj1}}{dt} = \frac{1}{2} v_{dc1} - v_{gj} - v_{pj} - v_{pj1} \tag{1}$$

$$L_0 \frac{di_{nj}}{dt} + L_0 \frac{di_{nj1}}{dt} = \frac{1}{2} v_{dc1} + v_{gj} - v_{nj} - v_{nj1} \tag{2}$$

The equations of the FBSM branch 2 can be obtained similarly. The AC current is composed of the current flowing through the FBSM branch 1 and the current flowing through the FBSM branch 2.

$$i_{gj} = i_{gj1} + i_{gj2} \tag{3}$$

Where,

$$i_{gj1} = i_{nj1} - i_{pj1} \tag{4}$$

$$i_{gj2} = i_{nj2} - i_{pj2} \tag{5}$$

The rated capacitor voltage of the FBSM branch 1 and that of the FBSM branch 2 are U_{smf1} and U_{smf2} respectively. The SM number of the FBSM branch 1 and that of the FBSM branch 2 are N_{F1} and N_{F2} respectively.

Under normal operating conditions, the rated voltages of the DC lines 1 and DC line 2 can be expressed as follows.

$$V_{dc1} = N_H U_{smh} + N_{F1} U_{smf1} \tag{6}$$

$$V_{dc2} = N_H U_{smh} + N_{F2} U_{smf2} \tag{7}$$

For each phase, the sum of the inserted HBSM is always N_H and the sum of the inserted FBSM is N_{F1} and N_{F2} respectively. In the normal operation condition, the SM capacitor voltage should be equal. If the rated voltages of HBSM and FBSM are all equal, the number of SMs invested in each branch has the following relationship.

$$\frac{N_{F1} + N_H}{N_{F2} + N_H} = \frac{V_{dc1}}{V_{dc2}} \tag{8}$$

When a pole to pole short-circuit fault occurs on the DC line 1, FBSMs connected to the DC line 1 are blocked. The HBSM and the parallel FBSM branches to which the DC line 2 is connected remain in operation. Due to the fault current blocking effect of FBSMs, the AC system cannot feed current to the fault point and the fault current on DC line1 is quickly blocked. Meantime, as the parallel FBSM branches are still working, the power transmission of DC line 2 is not affected.

According to [24], for a hybrid MMC with DC fault riding

through ability, the FBSM proportion should satisfy the following inequality.

$$\{N_{F1}, N_{F2}\} \geq N_H \tag{9}$$

The DC voltage level of the MTDC system is always uniform, the FBSM number N_{F1} and N_{F2} should also be the same. If the rated voltages of the DC line 1 and that of the DC line 2 are different, the FBSM number N_{F1} and N_{F2} can be calculated according to (8) and (9). Unless otherwise stated, the number of SMs in a FBSM branch is always equal to the number of SMs in a HBSM branch in the following analysis.

The sub-module capacitance is designed to limit the ripple of the capacitor voltage. According to [25], the capacitance of the FBSM branch 1 can be calculated as follows.

$$C_{smf1} = \frac{P_{ref1}}{3\xi U_{smf} V_{dc1} \omega m} \left[1 - \left(\frac{m \cos \varphi}{2} \right)^2 \right]^{1.5} \tag{10}$$

where, ω is the angular velocity corresponding to the grid frequency, $\cos\varphi$ is the power factor, and m is the MMC modulation ratio.

In this paper, the grid frequency is 50Hz. The modulation ratio m and the power factor $\cos\varphi$ are both set to 1. In (10), if the other parameters are all set, the sub-module capacitance is linear with the rated power. The capacitance of the FBSM branch 2 can be similarly designed according to the rated power of DC line 2. Furthermore, the power flowing through the HBSM branch is the sum of the two FBSM branches, and the HBSM capacitance is designed as follows.

$$C_{smh} = C_{smf1} + C_{smf2} \tag{11}$$

The topology shown in Fig. 3 can handle the case where the single-terminal grid supplies power to the other two terminals. Furthermore, the proposed topology can be extended to N-terminals DC grids with N parallel FBSM branches.

III. CONTROL STRATEGIES

As for the MTDC system in Fig. 2 (c), MMC 1 is connected to two MMCs (MMC 2 and MMC 3) via the DC line 1and DC line 2. The parameters of the two DC lines and the MMC stations are usually different and the control modes of the two

Fig. 4. The proposed MMC station control strategy.

DC outputs may be different. The conventional MMC control strategies are no longer applicable in the proposed MMC topology. Therefore, this paper proposes a corresponding MMC station control strategy for the proposed hybrid MMC topology.

The proposed MMC station control strategy includes: branch voltage controller, circulating current suppression controller (CCSC), and nearest level modulation (NLM). The proposed MMC station control strategy is shown as Fig. 4 and the design of each controller is described in detail in this section.

A. Branch Voltage Controller

In order to realize the function of the proposed topology, the corresponding branch voltage controller is designed according to the circuit relationship.

First, the AC output voltage of each branch can be defined as follows.

$$v_{hj} = \frac{v_{nj} - v_{pj}}{2} \tag{12}$$

$$v_{fj1} = \frac{v_{nj1} - v_{pj1}}{2} \tag{13}$$

$$v_{fj2} = \frac{v_{nj2} - v_{pj2}}{2} \tag{14}$$

According to (1) and (2), the relationship of the AC output voltages in the three-phase coordinate system is as follows.

$$L_0 \frac{di_{gj}}{dt} + L_0 \frac{di_{gj1}}{dt} = 2v_{gj} - 2v_{hj} - 2v_{fj1} \tag{15}$$

$$L_0 \frac{di_{gj}}{dt} + L_0 \frac{di_{gj2}}{dt} = 2v_{gj} - 2v_{hj} - 2v_{fj2} \tag{16}$$

In the synchronous rotating coordinate system, (15) and (16) can be rewritten as follows.

$$v_{hd} + v_{fd1} = v_{gd} - \frac{L_0}{2} \frac{d(i_{gd} + i_{gd1})}{dt} - \frac{\omega L_0}{2}(i_{gq} + i_{gq1}) \tag{17}$$

$$v_{hq} + v_{fq1} = v_{gq} - \frac{L_0}{2} \frac{d(i_{gq} + i_{gq1})}{dt} + \frac{\omega L_0}{2}(i_{gd} + i_{gd1}) \tag{18}$$

According to (17) and (18), the double loop controller of the FBSM branch 1 can been designed and the output voltage reference of the double loop controller is denoted as $v_{j1,ref}$. The double loop controller of the FBSM branch 2 can been designed in a similar way, and the output voltage reference of this controller is denoted as $v_{j2,ref}$. The double loop controllers are shown in Fig. 4.

The AC output voltage of the HBSM branch is defined as v_{hj} and the AC output voltages of the two FBSM branches are defined as v_{fj1} and v_{fj2} respectively. The double loop controller voltage reference is composed of the voltage of the HBSM branch and that of the FBSM branch.

$$v_{j1,ref} = v_{hj} + v_{fj1} \tag{19}$$

$$v_{j2,ref} = v_{hj} + v_{fj2} \tag{20}$$

According to (6) and (7), the branch reference voltages in (19) and (20) have a certain ratio. The results of the branch reference voltage can be calculated as follows.

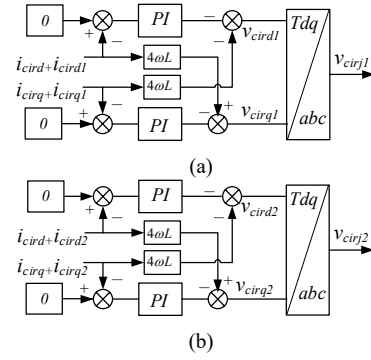$$v_{hj} = \frac{N_H v_{j1,ref} + N_H v_{j2,ref}}{2N_H + N_{F1} + N_{F2}} \tag{21}$$

(a)

(b)

Fig. 5. Circulating Current Suppressing Controller. (a) CCSC1; (b) CCSC2.

$$v_{fj1} = \frac{(N_H + N_{F1} + N_{F2})v_{j1,ref} - N_H v_{j2,ref}}{2N_H + N_{F1} + N_{F2}} \tag{22}$$

$$v_{fj2} = \frac{(N_H + N_{F1} + N_{F2})v_{j2,ref} - N_H v_{j1,ref}}{2N_H + N_{F1} + N_{F2}} \tag{23}$$

If CCSC is not considered, the output of the branch voltage controller can be directly used for NLM. Thus, the branch reference voltage of the upper and lower arms of each phase can be calculated according to (12) (13) and (14).

B. Circulating Current Suppressing Controller

As for the proposed hybrid MMC topology, the circulating current is also different from the conventional MMC. So the CCSC should be redesigned. The circulating current of the conventional MMC is defined as follows.

$$i_{cirj} = \frac{1}{2}(i_{nj} + i_{pj}) \tag{24}$$

Similarly, the FBSM branch circulating currents of the proposed hybrid MMC topology can be defined as follows.

$$i_{cirj1} = \frac{1}{2}(i_{nj1} + i_{pj1}) \tag{25}$$

$$i_{cirj1} = \frac{1}{2}(i_{nj1} + i_{pj1}) \tag{26}$$

According to (1) and (2), the circulating currents of the proposed hybrid MMC topology have the following relationship.

$$L_0 \frac{di_{cirj}}{dt} + L_0 \frac{di_{cirj1}}{dt} = \frac{1}{2}v_{dc1} - \frac{1}{2}(v_{pj} + v_{nj}) - \frac{1}{2}(v_{pj1} + v_{nj1}) \tag{27}$$

$$L_0 \frac{di_{cirj}}{dt} + L_0 \frac{di_{cirj2}}{dt} = \frac{1}{2}v_{dc2} - \frac{1}{2}(v_{pj} + v_{nj}) - \frac{1}{2}(v_{pj2} + v_{nj2}) \tag{28}$$

It can be seen from (27) and (28) that the circulating current of the FBSM branch 1 and that of the FBSM branch 2 do not affect each other. The circulating currents can be controlled separately. In the double frequency negative sequence rotating coordinate system, the structure of the CCSC are shown in Fig. 5.

C. Nearest Level Modulation

The equalization and stability of SM voltage is the basis for stable operation of MMC. For the NLM Strategy, the SM capacitor voltage balancing is affected by the modulation reference, the current direction and the SM capacitor voltage sorting result. The proposed hybrid MMC topology contains two parallel FBSM branches and a HBSM branch each arm. Because the current flowing through each branch is inconsistent and the power loss of the FBSM is not the same as
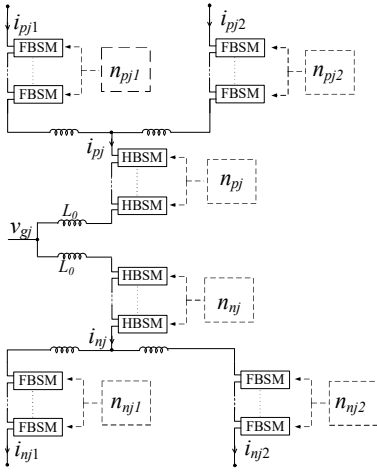
Fig. 6. The modulation outputs of each branch.

the HBSM, it is difficult for the SM capacitor voltages of different branches to maintain a balance.

Therefore, in the control process, the reference voltages of different branches are separated. As long as the SM capacitor voltage in each branch is balanced and each branch follows the branch reference voltage, the proposed topology can operate stably. The modulation output results corresponding to each branch are shown in Fig. 6. On the basis of branch modulation, the SM capacitor voltage balance control of each branch can be realized

Taking the HBSM branch as an example, the SM capacitor voltage balancing control strategy is shown in Fig. 7. The input voltage of the NLM is v_{hj} and the number of inserting SMs n_{pj} of the HBSM branch can be obtained. When the current flowing through the HBSM branch is positive, n_{pj} submodules with the lower capacitor voltage are inserted. When the current flowing through the HBSM branch is negative, n_{pj} submodules with the higher capacitor voltage are inserted.

Through the above modulation and voltage balancing strategy, the SM capacitor voltages of each branch can be balanced. The sum of the inserting SM capacitor voltages follows its voltage reference. Thus, the SM capacitor voltages of the entire arm can achieve balancing.

IV.   VERIFICATION

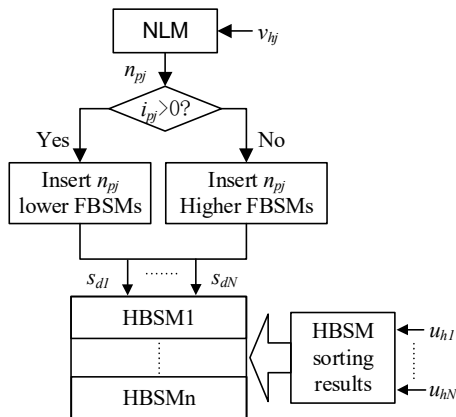In MATLAB/Simulink, the simulation model is constructed to verify the feasibility of the proposed MMC topology and

Fig. 7. Voltage balancing control strategy of the HBSM branch.

TABLE II
CONTROL CASE

Symbol	Value	Symbol	Value
V_g	23 kV	V_{dc1}, V_{dc2}	50 kV
Q_{ref1}, Q_{ref2}	0 Mvar	P_{ref1}	50 MW
P_{2ef2}	62.5 MW	N_H	10
N_{F1}, N_{F2}	10	C_{smh}	13.2 mF
C_{smf1}, C_{smf2}	6.6 mF	U_{smh}	2.5 kV
U_{smf1}, U_{smf2}	2.5kV	L_0	9 mH
L_d	120 mH	ξ	± 10 %

control strategies. The HVDC transmission system adopts bipolar transmission mode, and MMC 1 adopts the proposed hybrid MMC topology shown in Fig. 3. The preset fault is a bipolar short circuit fault on the DC line 1. The system parameters of the simulation model are shown in Table II. The DC voltage level of the MTDC system is uniform and the transmission power of each line is often different. In this case, the DC line 1 and DC line 2 have the same parameters except for active power, and the circuit parameters of FBSM branch 1 are consistent with that of FBSM branch 2. Both FBSM branch 1 and FBSM branch 2 adopt DC voltage and reactive power control modes.

In the case, the DC line 1 has a DC bipolar short-circuit, and the FBSM branches connected to the DC line 1 are completely blocked after 5 milliseconds. The control loop 1 fails at the same time and the reference value of the control loop 1 $v_{j1,ref}$ is consistent with $v_{j2,ref}$. The HBSM branch and the FBSM branch 2 connected to the DC line 2 remain in normal operation and the DC line 2 still maintains power transmission. The results in this section are the internal variables of MMC1 or the system connected to MMC1.

Fig. 8 (a) shows the current of the DC line 1 and that of the DC line 2. Before the fault occurs, the current of the DC line 1 is stable at 1 kA and that of the DC line 2 is 1.25 kA. After the fault occurs, the DC current rises rapidly until the FBSM branches connected to the DC line 1 are blocked. Due to the presence of the DC limiting inductor, the current of the DC line 1 i_{dc1} will be limited in a secure range. As the DC bipolar short-circuit fault occurs, the current of the DC line 2 i_{dc2} has a
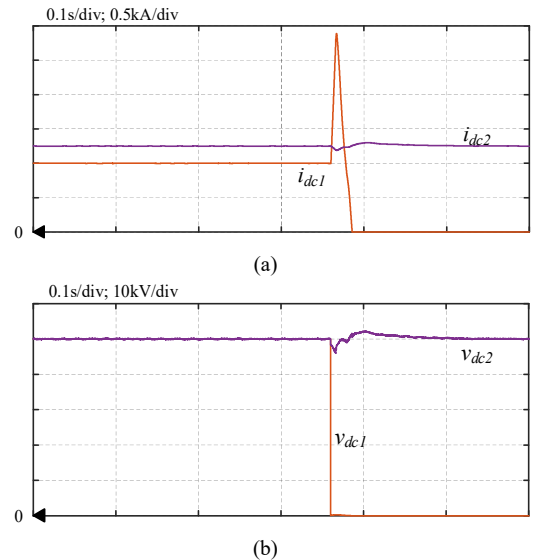

Fig. 8. The operation of the DC line. (a) DC current; (b) DC voltage.
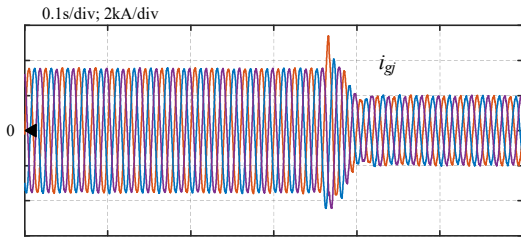
0.1s/div; 2kA/div

i_{gj}

Fig. 9. The AC grid current of MMC 1.

small fluctuation and quickly returns to its normal value.

Fig. 8 (b) shows the voltage of the DC line 1 and that of the DC line 2. Before the fault occurs, the two DC lines both operate in the normal condition and the rated voltage is 50 kV. The voltage of the DC line 1 v_{dc1} decreases as soon as the fault occurs. This is due to DC fault and FBSM blocking will make the DC voltage drop to 0. Similar to the current, the voltage of the DC line 2 quickly returns to stability after a short period of fluctuation. After applying the proposed topology, the DC fault of the DC line 1 has little effect on the DC line 2 and the DC fault is isolated. The above simulation results illustrate the effectiveness of the proposed topology and control strategies.

Fig. 9 shows the AC grid current of MMC 1. It can be seen that the grid current will rise before the fault current is blocked. After the FBSMs connected to the DC line 1 are blocked, the transmission power of the AC grid falls from (P_1+P_2) to P_2 and the peak of the grid current also falls. With the proposed hybrid MMC topology, the DC fault line is isolated and the AC grid can continue to transmit power to the fault-free DC lines.

Fig. 10(a) shows the upper arm currents which flow through the three-phase HBSM branches. Similar to the grid current, the currents flowing through the HBSM branches also rise before
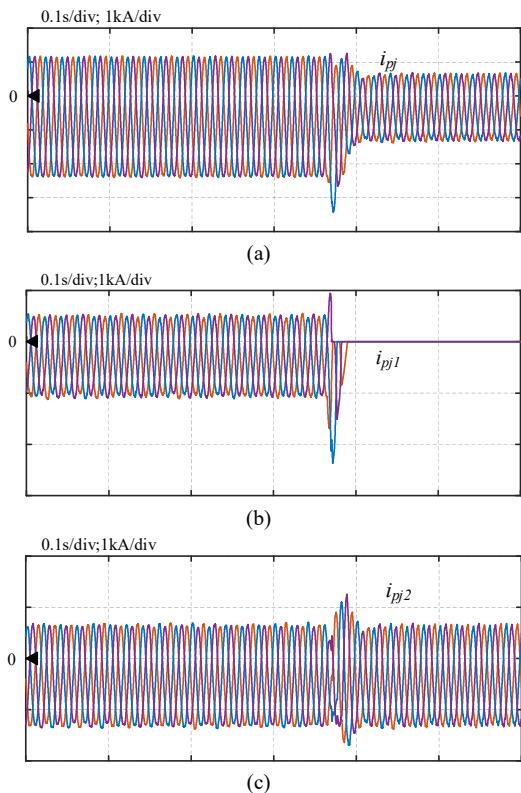
the fault current is blocked. The currents flowing through the FBSM branches are shown in Fig. 10(b) and Fig 10(c). As the FBSMs connected to the DC line 1 are blocked, the currents flowing through those branches decrease to 0. And the currents flowing through the remained FBSMs can return to normal operation after a period of fluctuation. It can be seen from Fig. 10 that the DC bipolar fault will have an impact on the system. However, by blocking the corresponding FBSMs, the fault current can be blocked, and the fault-free line can still operate normally.

Take the upper arm of phase A as an example, the simulation results of the SM capacitor voltages are shown in Fig. 11. The SM capacitance was designed according to (10) and (11). After the fault occurs, the capacitor voltages of the HBSM branch are still at the rated value. However, the current flowing through the HBSM branch is reduced, so its capacitor voltage ripple will also decrease as shown in Fig. 11 (a). It can be seen from Fig. 11 (b) that the SM capacitor voltages of the FBSM branch 1 will rise as the FBSMs are blocked. This is because the fault current will charge the FBSM capacitor until the fault current is completely blocked. As shown in Fig. 11 (c), the capacitor voltages of the FBSM branch 2 can return to the rated voltage after a small increase.

As long as the fault is cleared, the MTDC system can return to normal operation. For permanent faults, the entire MMC can be restarted after the fault is cleared. In this case, the energy stored in capacitors will be consumed by the bypass resistors. For

The simulation results show that the proposed topology and control strategies can quickly block the fault current and isolate

0.1s/div; 1kA/div

i_{pj}

0

(a)

0.1s/div;1kA/div

0

i_{pj1}

(b)

0.1s/div;1kA/div

i_{pj2}

0

(c)

Fig. 10. The upper arm current of each phase. (a) HBSM branch; (b) FBSM branch 1; (c) FBSM branch 2.

0.1s/div; 0.2kV/div

u_{smh}

2.0

(a)

0.1s/div; 0.2kV/div

u_{smf1}

2.0

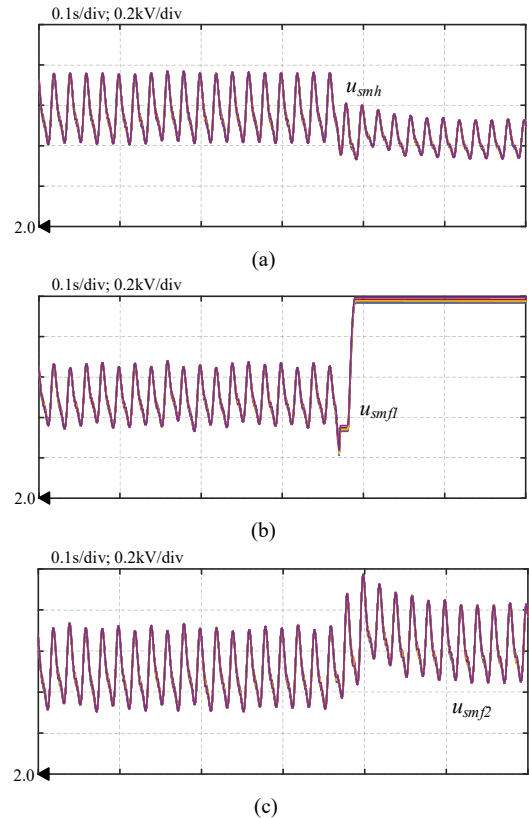(b)

0.1s/div; 0.2kV/div

u_{smf2}

2.0

(c)

Fig. 11. The SM capacitor voltages of phase A upper arm. (a) HBSM branch; (b) FBSM branch 1; (c) FBSM branch 2.

temporary faults, the corresponding controller is initialized first, and then the blocked FBSMs are restored. In this case, the energy stored in capacitors will be transmitted to the load. The fault line under the DC bipolar short-circuit fault. The feasibility and effectiveness of the proposed topology have been verified.

V. TOPOLOGY COMPARISON

The DC fault protection schemes of the MMC-MTDC system are shown in Fig. 2. First, the HBSM-MMC cannot interrupt the DC fault current and DCCBs are necessary to protect the converter under DC short-circuit faults. Secondly, the hybrid MMC can use FBSMs to block DC fault current. Finally, the proposed MMC topology can block the DC fault current and isolate the fault line as shown in Fig. 2 (c). The device number and power loss of different topologies are listed in Table III.

According to (9), the number of FBSMs in the hybrid MMC cannot be less than the number of HBSMs. For the hybrid MMC in Table 3, the number of FBSMs is equal to the number of HBSMs. If the ratio of FBSM increases, the cost and loss of the hybrid MMC will further increase. A simplified MMC loss model is adopted to calculate the power loss of the topologies [26]. The parameters used in the power loss calculation are derived from the datasheet of the Infineon insulated gate bipolar transistor (IGBT) module FZI500R33HL3.

As shown in Table III, the HBSM-MMC has the lowest power loss and the least number of semiconductor devices. However, DCCBs are expensive and bulky [27][28]. Compared with the proposed MMC topology, the hybrid MMC requires fewer semiconductor devices, but its loss is higher and there is no fault isolation capability. Although the proposed MMC topology requires the most semiconductor devices, the current flowing through the FBSM branch is only half of the HBSM current. The smaller current stress can reduce the devices' cost and power loss. The proposed MMC topology has two FBSM branches, which increases the system complexity and cost, but it also has the aforementioned advantages compared to other topologies. It is a beneficial choice for the MTDC system.

TABLE III
TOPOLOGY COMPARISON

Item	Proposed topology	Hybrid MMC (N_H= N/2)	HB MMC + DC breaker
MMC rated power	110MW	110MW	110MW
DC voltage	50kV	50kV	50kV
No. of HBSMs per arm	10	10	20
No. of FBSMs per arm	2×10	10	0
SM capacitor voltage	2.5kV	2.5kV	2.5kV
Power capacity per HBSM	1.83 MW	1.83 MW	1.83 MW
Power capacity per FBSM	0.92 MW	1.83 MW	0
No. of IGBTs per arm	100	60	40
No. of DC breakers	0	0	16
Conduction Loss	881.29kW	1307.90kW	880.29kW
Switching Loss	168.45kW	96.99kW	64.78kW
Total Loss	1049.74kW	1404.89kW	945.07kW
Total loss ratio	0.95%	1.28%	0.86%
DC fault blocking	yes	yes	yes
DC fault isolation	yes	no	yes

VI. CONCLUSION

In this paper, a MMC topology with partially hybrid branches is proposed. The proposed MMC topology is suitable for the MTDC system, as it can reduce the influence range of the DC fault and improve the reliability of the power supply. In order to selectively block the fault current and isolate the fault line, corresponding control strategies are also proposed. With the branch reference calculation and group voltage balancing method, the parallel FBSM branches can operate in different conditions. The power flow of the proposed topology can be flexibly controlled, which improves the availability of the proposed topology. The proposed topology and control strategies are verified by simulation results.

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