On-Line Fault Diagnosis and Fault-Tolerant Operation of Modular Multilevel Converters –A Comprehensive Review

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***Abstract*—Modular multilevel converters (MMCs) have been one of the most broadly used multilevel converter topologies in industrial applications, particularly in medium-voltage motor drives and high-voltage dc power conversion systems. However, due to the utilization of large amount of semiconductor devices, the reliability of MMCs becomes one of the severe challenges constraining their further development and applications. In this paper, common electrical faults of the MMC have been summarized and analyzed, including open-circuit switching faults, short-circuit switching faults, dc-bus short-circuit faults, and single line-to-ground faults on the ac side. A thorough and comprehensive review of the existing online fault diagnostic methods has been conducted. In addition, fault-tolerant operation strategies for such various fault scenarios in MMCs have been presented. All the fault diagnosis and fault-tolerant operation strategies are comparatively evaluated, which aims to provide a state-of-the-art reference on the MMC reliability for future research and industrial applications.**

***Index Terms*—Modular multilevel converters, switching open-circuit fault, line-to-ground fault, diagnosis, fault tolerance.**

I. Introduction

MODULAR multilevel converter (MMC) has been one of the most attractive converter topologies for medium-voltage motor-drive systems and high-voltage direct-current (HVDC) transmission systems. The main advantages of MMC include: modularity and scalability to different voltage and power levels, high efficiency, low harmonic distortions in the output voltages, and the absence of additional bulky capacitors on the dc bus [1][2].

As is shown in Fig. 1, the most general topology of an MMC consists of two arms per phase leg, in which each arm comprises *n* series-connected identical *L*. Each SM contains a half-bridge converter circuit and a dc capacitor *C*. The output voltage of each SM equals its capacitor voltage (V_c) when the SM is activated, or zero when it is deactivated. The voltage

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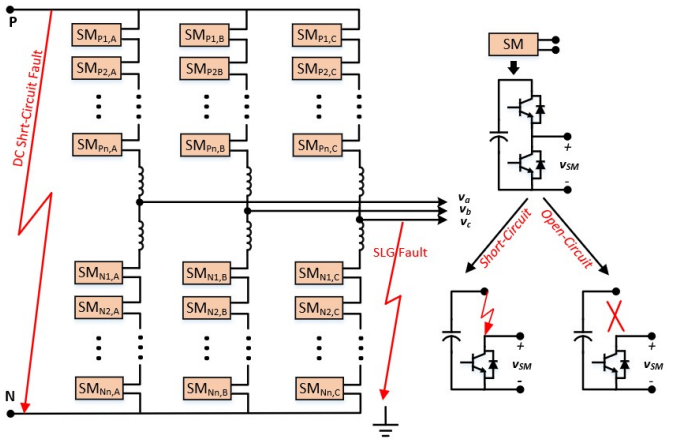


Fig. 1. Common electrical faults in a half-bridge MMC.

waveforms at the ac side of the MMC can be synthesized by using multiple options of modulation techniques [1]. Most of these modulation methods are based on defining the number of SMs to be activated in each of the arms, and the particular SMs activated are determined by a voltage balancing algorithm [3].

Reliability has been one of the most severe challenges for the further development of MMCs, since there are typically a great many of semiconductor switching devices utilized in the circuit topologies which decrease the converter hardware reliability. The more SMs are employed, the higher the failure rate of the MMC has. Any electrical faults, such as switching open-circuit (OC) faults, short-circuit (SC) faults, dc-bus short-circuit fault, or single line-to-ground (SLG) fault, as illustrated in Fig. 1, may cause a malfunction of the whole MMC or even catastrophic system failures if an effective fault diagnosis and fault-tolerant solution is unavailable. Therefore, it is of paramount necessity to review and compare the existing fault diagnosis and fault-tolerant approaches to these common faults that could occur to MMCs.

The remaining content of this paper is organized as follows. In Section II, the common electrical faults that could occur in MMCs and their impact on the converter performance will be analyzed in different categories. These faults include the switching OC faults, switching SC faults, SC faults on the dc side, and SLG fault on the ac side. In Section III, existing fault diagnosis methods in the literature will be reviewed and evaluated. In Section IV, fault-tolerant operation approaches in the literature for the aforementioned electric faults in MMCs will be comparatively discussed. Finally, conclusions and recommendations are given in Section V.

II. Common Electrical Faults in MMCs

Common electrical faults in MMCs can be classified into four categories, namely, switching OC faults, switching SC faults, SC fault on the dc side, and SLG fault on the ac side. Each type of these faults will be analyzed in detail as follows.

A. Open-Circuit (OC) Switching Fault

During operation of an MMC, degradations such as bond wire lift-off or soldering cracking due to thermal-mechanical induced stress and significant junction temperature swings can cause an OC fault in the solid-state switching devices [4]. Other common causes for an OC fault include gate driver malfunction, electrical disconnection, and the like. Such a fault may lead to a significant increase of the capacitor voltages in the faulty SM due to the absence of discharge circuit path, which could result in cascaded damage to the MMC systems. Additionally, an OC switching fault can cause dramatic distortion of the output voltages and currents, because of the loss of the access to some output voltage levels, leading to further reliability degradations in the load. For instance, if the load is a medium-voltage electric motor, the distortion in the output current of an MMC may induce considerable vibration and acoustic noise as well as torque pulsation of the motor. Thus, it is of great necessity to detect and identify such OC faults in MMCs, so a fault-tolerant or fault isolation strategy can be triggered in time.

B. Short-Circuit (SC) Switching Fault

Switching SC fault is also destructive to an MMC system. SC faults can occur due to parasitic turn-on (e.g., cross-talk), gate driver malfunction, overcurrent, overvoltage, overheat, and other reasons. Detecting short-circuit switching faults typically relies on hardware circuits integrated in the gate drivers due to the requirement of fast response, because the short-circuit withstanding time of semiconductor devices is typically less than 10 μs [5]. The recently emerging wide bandgap devices require faster detection speed (i.e.,<5μs) for SC fault, due to smaller die size and reduced thermal capacitance [6]. Currently, most of the commercial gate drivers have been integrated with short-circuit detection/protection, and one broadly adopted solution is named desaturation protection, in which the on-state voltage of the switching devices will be sensed and compared to a predetermined threshold value to determine a SC fault [7]. When such a SC fault is detected, the driver will softly turn off the switching devices in MMCs, which finally results in a switching OC fault in the MMCs.

C. Short-Circuit (SC) Fault on DC Side

Like all other voltage source converters (VSCs), half-bridge based MMCs (HB-MMC) is not immune to dc short-circuit fault (i.e., pole-to-pole fault). Once such a fault occurs, the capacitors in the SMs will discharge, and the fault current in the converter arms and dc bus will mainly derive from the discharging of SM capacitors. Once the fault is detected, the semiconductor switches will be typically turned off and the MMC will enter into the blocking mode, in which the ac source will feed the fault on the dc-side through the anti-parallel diodes of the half-bridge cells, as illustrated in Fig. 2. In such an uncontrolled operation scenario, the converter has to withstand pronounced fault current from the ac network until the dc fault is interrupted, which most likely will damage the converter due to the limited current capability in the semiconductor devices or other power components. In a medium-voltage motor drive system, the high back electromotive force (EMF) of the machine can also generate large current due to the dc fault through an uncontrolled generator mode, damaging the converter components. In the applications that are vulnerable to temporary dc faults such as weak ac grid, a fast fault detection and fault ride-through (FRT) capability with the MMCs is highly required. Challenges on how to promptly detect a dc SC fault based on monitoring the fault signatures contained in the converter voltage or current signals, and how to tolerate such a fault in a timely manner during post-fault operation, will be of great significance to be addressed.

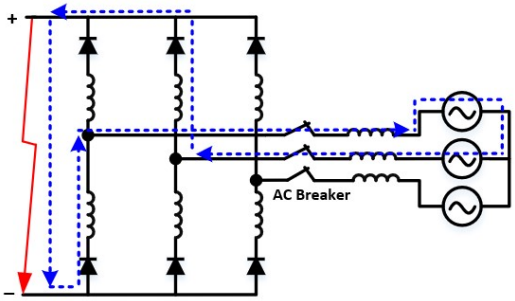


Fig. 2. Equivalent circuit of HB-MMC during a dc short-circuit fault at blocking mode.

D. Single Line-to-Ground Fault on AC Side

In a point-to-point MMC-HVDC transmission system, an SLG fault could occur between any of the ac lines to the ground, as shown in Fig. 1. Depending on the fault location, there are three possible SLG fault scenarios: fault in the primary side of a Y-Δ transformer based system, fault in the secondary side of a Y-Δ transformer based system, and fault in a transformerless system. For instance, insulation failures of transformer wall bushings may cause an SLG fault between the MMC and the transformer. Once an SLG fault happens, there could be ac voltage sags and instantaneous power reduction of the MMCs. Also, a twice line frequency oscillation could be imposed in the dc-bus voltage. The twice line frequency oscillation would not only be transferred to the other converter station leading to additional voltage stress to the power devices of the MMC, but also probably cause malfunction of the protection system [8]. If an SLG fault occurs at the power dispatcher converter station side while it is operated at an inverter mode to deliver active power to the coupled grid, the average SM capacitor voltage of the MMC would increase immediately causing temporary dc bus overvoltage [9]. This is due to the fact that the average SM capacitor voltage is imposed simultaneously on the dc bus voltage.

The simulation waveforms of a grid-connected MMC system (with interface Y-Δ transformer) in a SLG fault process are shown in Fig. 3 to illustrate the consequence of a SLG fault. From the top to the bottom in Fig. 3, these waveforms include

ground current of the grid, grid currents, ground current of the Y-side (i.e., grid-side) of the transformer, terminal line-to-line voltage of the MMC, *dq*-component of the output current of the MMC, active and reactive power at the ac terminal of the MMC, and average capacitor voltage of the upper arm of phase *a* in the MMC. As it can be seen, once the SLG fault occurs at the instant of t=0.7 seconds, significant ground current, unbalanced three-phase line-to-line voltages, excessive fluctuation of the active and reactive power, and average capacitor overvoltage of the upper arm, will appear all together, which may trip or damage the MMC system. Therefore, it is of great significance to detect and provide a fault-tolerant solution to such SLG faults.

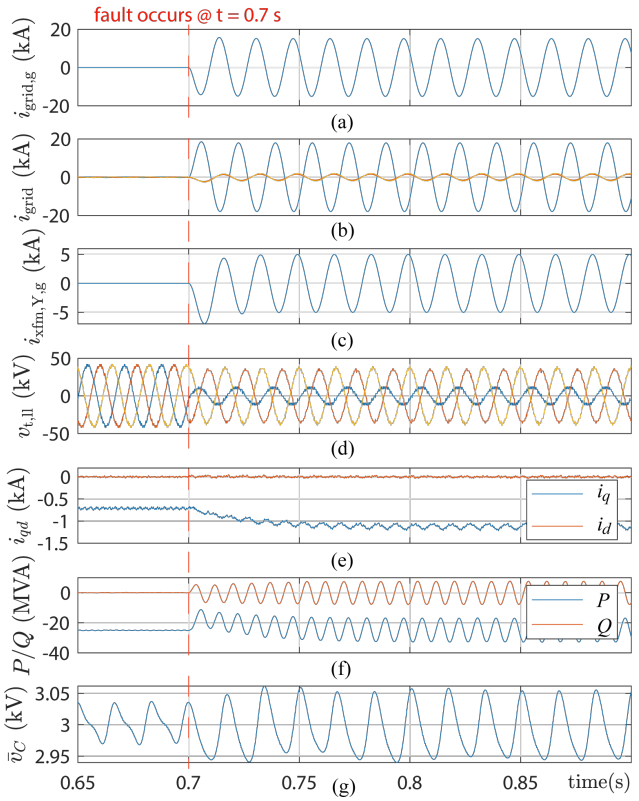


Fig. 3: Simulation waveforms of a grid-connected MMC system (with interface Y-Δ transformer) in a SLG fault process: (a) ground current of the grid, (b) grid currents, (c) ground current of the Y-side (grid-side) of transformer, (d) terminal line-to-line voltage of the MMC, (e) *dq*-component of output current of the MMC, (f) active and reactive power at ac terminal of the MMC, and (g) average capacitor voltage of the upper arm of phase *a* in the MMC.

III. On-Line Fault Diagnosis of MMCs

As is known, there are typically two steps for online diagnosis, namely, fault detection and fault identification. These two steps sometimes can be achieved online simultaneously. In practical implementation, criteria for evaluating an online diagnostic method generally include: high accuracy, easy implementation, fast diagnostic speed, low cost, noninvasive diagnosis, and high robustness. These criteria will be employed during the following review of the existing diagnostic methods in the literature for the aforementioned four types of electrical faults in MMCs.

A. Diagnosis of OC Switching Fault

Two typical OC switching faults in SM are illustrated in Fig. 4. Unlike the diagnosis of SC switching fault, the online diagnosis of OC switching faults mostly relies on nonintrusive software algorithm integrated into the system controller. This is mainly due to the fact that OC switching faults allow longer time to be detected than that for SC faults, and most of the software-based detection methods typically possess lower implementation cost. Such software-based methods detect and identify the fault by monitoring the variations of the fault signatures contained in the critical converter operation variables. The software-based diagnostic methods include two categories: model-based methods and signal-processing based methods. For these model-based diagnostic methods [10-13], the OC switching fault occurrences can be diagnosed by comparing the measured fault indicator variables to the estimated values which are computed from the developed mathematical models. In the signal processing-based methods [14-17], the variables under monitoring are processed in either time domain or frequency domain, and then compared to predetermined threshold values.

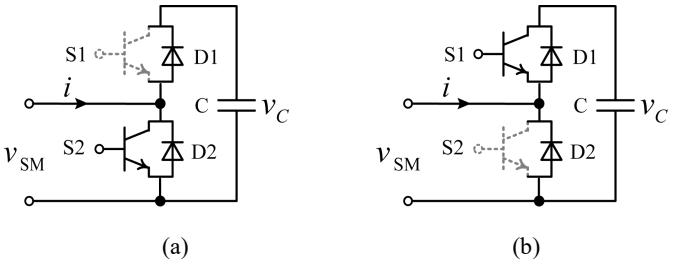


Fig. 4: Two typical OC fault in a SM: (a) OC fault at the upper switch, (b) OC fault at the lower switch.

Relations among the variables of the MMC can be summarized as follows:

$$v_{t,j} = \frac{V_{dc}}{2} - \sum_{i=1}^{N} S_{j,u,i} v_{C,j,u,i} - L_{arm} \frac{di_{j,u}}{dt} - R_{arm} i_{j,u}, \quad (1)$$

$$v_{t,j} = -\frac{V_{dc}}{2} + \sum_{i=1}^{N} S_{j,l,i} v_{C,j,l,i} + L_{arm} \frac{di_{j,l}}{dt} + R_{arm} i_{j,l} \quad (2)$$

$$C \frac{dv_{C,j,u,i}}{dt} = S_{j,u,i} i_{j,u} \quad (3)$$

$$C \frac{dv_{C,j,l,i}}{dt} = S_{j,l,i} i_{j,l} \quad (4)$$

where $v_{t,j}$ is the terminal voltage of phase j, V_{dc} is the dc-link voltage, $S_{j,u,i}$ ($S_{j,l,i}$) is the gating signal of the upper switch of the i-th SM in the upper (lower) arm of phase j, $v_{C,j,u,i}$ ($v_{C,j,l,i}$) is the capacitor voltage of the i-th SM in the upper (lower) arm of phase j, $i_{j,u}$ ($i_{j,l}$) is the current through the upper (lower) arm of phase j, L_{arm} is the inductance of arm inductor, R_{arm} is the equivalent resistance of the arm, and C is the capacitance of SM capacitor. Based on (1) and (2), dynamics of the circulating current of phase j, i.e., $i_{j,cir}$, can be expressed as:

$$L_{arm} \frac{di_{j,cir}}{dt} = \frac{V_{dc}}{2} - \frac{1}{2}\sum_{i=1}^{N} S_{j,l,i} v_{C,j,l,i} - \frac{1}{2}\sum_{i=1}^{N} S_{j,u,i} v_{C,j,u,i} - R_{arm} i_{j,cir} \quad (5)$$

where $i_{j,cir}$ is defined as $(i_{j,u} + i_{j,l})/2$. Since the OC faults will

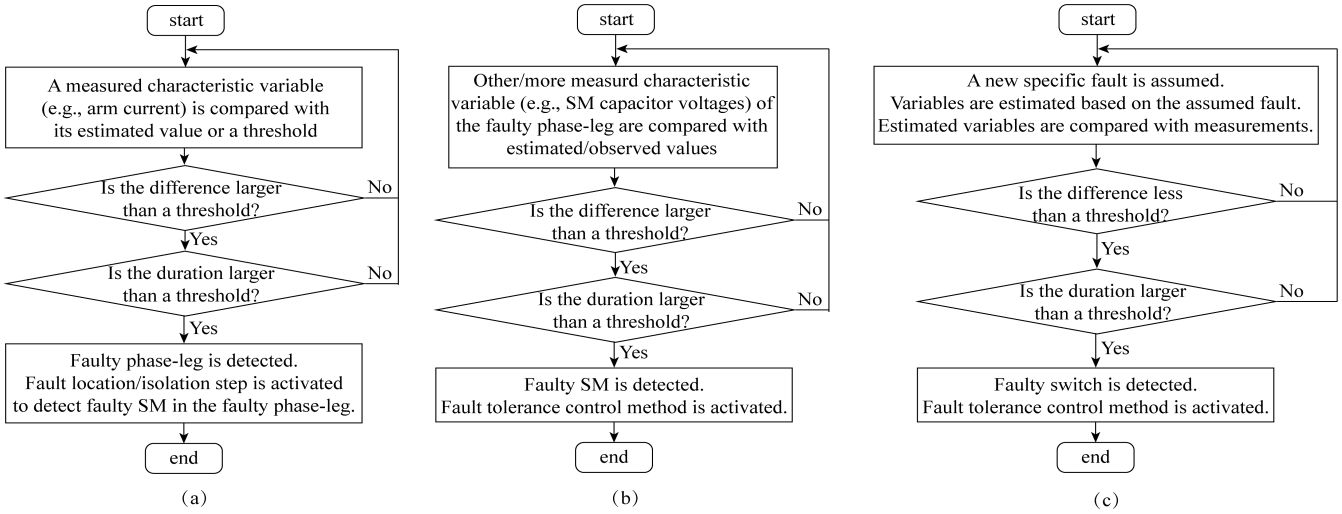


Fig. 5. Two-step framework to detect a switching OC fault in MMCs: (a) the fault detection step, (b) the fault location step based on signal processing-based method, (c) the fault location step based on model-based trial-and-error method.

cause the output voltage of the SM and the current path in the SM differ from their expected/commanded ones, as detailed in Table I, waveform distortion of the internal currents, i.e., $i_{j,u}$ and $i_{j,l}$, and SM capacitor voltages, i.e., $v_{C,j,u,i}$ and $v_{C,j,l,i}$ will appear after the faults. Besides, since the gating signal is generated based on the control loop and the sampled currents and voltages, the gating signal will be distorted as well subsequent to the occurrence of the OC switching fault. Therefore, $i_{j,u}$, $i_{j,l}$, $v_{C,j,u,i}$, $v_{C,j,l,i}$, $S_{j,u,i}$, $S_{j,l,i}$, and the relevant derivative variables, e.g., $i_{j,cir}$ can be used as fault indicators of the system.

TABLE I
Impact of the OC faults on the SM output.

Normal SM				
i	>0		<0	
S_1	1	0	1	0
Current path	D1	S2	S1	D2
v_{SM}	v_C	0	v_C	0
Faulty SM with OC @ S1 (Fig. 4(a))				
i	>0		<0	
S_1	1	0	1	0
Current path	D1	S2	D2	D2
v_{SM}	v_C	0	0	0
Faulty SM with OC @ S2 (Fig. 4(b))				
i	>0		<0	
S_1	1	0	1	0
Current path	D1	D1	S1	D2
v_{SM}	v_C	v_C	v_C	0

According to the recent literature on fault diagnosis of OC switching faults in MMCs [10-17], a well-established framework of the OC fault diagnostic methods contains two steps, i.e., fault detection and fault location, as illustrated in Fig. 5. In the fault detection step, a characteristic variable, e.g., arm currents, circulating currents, or arm voltages, is utilized to detect whether the phase leg is normal or faulty, as illustrated in Fig. 5(a). If a faulty phase is detected, fault location step is activated. The fault location method is to examine other/more characteristic variables, e.g., SM capacitor voltages in the phase leg, to pinpoint the faulty SM(s), as shown in Fig. 5(b) [18]-[21]. In addition to SM capacitor voltages, another popular characteristic variable in the fault location step is the comparison result of the SM insertion commands and faulty phase detection results: if the faulty phase is always detected when a SM should be inserted, the SM is pinpointed as faulty one. In the model-based fault location method, "trial-and-error" strategy is used to detect the faulty switch, as shown in Fig. 5(c) [10][11][13][22][23]. Another typical strategy of the controllable switch-focused methods is based on SM capacitor voltages directly to pinpoint the faulty SM [14][15][17][24]. More details of the methods are provided in Table II. It is noteworthy that the fault detection duration column just lists the time needed to detect/locate the fault in the specific operation conditions in the literature.

Fault detection time depends on many factors, including hardware parameters, operation conditions, threshold settings of the associated fault detection algorithms, sampling rate and communication delays of control system and so forth. If operation condition and/or some threshold values change, the fault detection time will vary accordingly. For instance, open-circuit fault on upper controllable switch, i.e. S1, of a half-bridge SM cannot be detected until the SM is inserted and arm current is positive. Therefore, even if the same fault location methods are applied to detect the same fault, fault location time still could be different significantly [14][20]. Meanwhile, if no extra sensors added, faulty SM detection time is in the range of tens of milliseconds, even up to around 100 ms . If extra sensors are added, faulty SM detection time will be further reduced [25]. However, extra sensors require higher cost and more complexity. Therefore, a trade-off between faster fault detection speed and lower cost needs to be considered. In addition, under multiple-fault conditions, all the signal processing-based methods can be still effective. However, since mathematical models of the MMC vary with different fault conditions, the model-based methods are only capable to detect faulty phase leg, but not be capable to locate faulty SM any further. To enable the model-based methods to locate multiple faulty SMs, the mathematical models need to be modified, which could further increase computational burden

on the microcontrollers. Thus, the signal processing-based methods are more compatible with different fault types.

A typical model-based two-step method, which is based on sliding-mode observer (SMO), is proposed in [10][11]. The two steps of the SMO-based method are fault detection mode and fault isolation mode, the framework of which is illustrated in Fig. 3(a) and (c). In the fault detection mode, difference between the measured arm currents and the observed values based on a normal MMC configuration is monitored. If the difference exceeds a threshold value for certain time duration, a fault isolation mode will be activated. The fault isolation mode is based on "trial-and-error" principle, where different faults are assumed, the SMO is modified based on the assumed faults, and the observed results are compared with the measurements. If the measurements match the observations based on a certain fault, the faulty switch will be detected. In [11], fault indicators of the SMO-based method are modified: in both the two modes, circulating current is used to indicate whether the SMOs match the MMC configurations. In addition, reference [17] develops a similar SMO-based OC fault detection and isolation method for full-bridge SM-based MMC, in which the observed circulating currents based on SMO is used as the fault indicator in the fault detection step and differences between the SM capacitor voltages and their minimum one are used to locate the faulty SM. Likewise, another similar approach is proposed in [13], in which the difference is that the "mathematical model" is substituted with an extended state observer and the modified switching models.

A Kalman filter based two-step fault diagnostic method is proposed in [18] to locate faulty SMs under switching OC fault. In the fault detection step, a Kalman filter is used to estimate circulating currents of three phase legs. If the difference between the estimated circulating current and the measured value of a certain phase leg is larger than a preset threshold value for a certain time length, the faulty phase leg will be detected and the fault localization command will be activated. In the fault localization step, SM capacitor voltages of the faulty phase are compared with the lowest one among the voltages. If any capacitor voltages are significantly higher than the lowest one for a given time duration, the SMs with the large capacitor voltages will be detected to be the faulty one.

In [19], a four-step strategy is proposed to deal with a single IGBT OC fault, where the first and third steps, i.e., fault detection and fault localization, aim at locating the faulty SM. In the fault detection step, a generic state observer is used to observe circulating currents. Based on the observed circulating currents and measured values, three phase legs are checked to determine the health condition. If a phase leg is determined as faulty, the proposed fault-tolerant method and fault localization methods will be activated successively. The fault localization method is based on measuring the SM capacitor voltages, which is similar to that in [18]. One difference is that the capacitor voltage comparison targets at only one arm in [19], while the comparison in [18] is applied to two arms within the faulty leg.

Two faulty SM detection methods are proposed in [14], i.e. a clustering algorithm based method and a calculated capacitance-based method. For the proposed clustering algorithm based method, a two-dimensional trajectory is plotted based on two characteristic variables of each SM. Subsequent to the fault occurrence, the characteristic trajectories of faulty SMs will deviate from those of normal ones, and a clustering algorithm is applied to recognize the deviated trajectories, i.e., the faulty SMs. The calculated capacitance-based method is based on a generic state observer essentially, in which the faulty switch can be pinpointed.

A fault detection method based on SM output voltages is proposed in [15], where the output voltages of a certain SM are measured to examine whether they match the gating signals of the SM. Since the sensing of output voltages of SMs are generally unnecessary for normal control of MMCs, extra voltage sensors are required for this detection approach. A similar output voltage sensing based method is proposed for a three-level SM based MMC in [17].

Based on measuring the circulating currents and SM capacitor voltages, a framework to detect internal and external electrical faults of MMC is proposed in [21]. If the calculated circulating currents based on the power references mismatch the measured values, an active fault will be designated. If the variance between the capacitor voltage of a certain SM and the voltage reference is larger than a threshold value, the SM is detected to be the faulty one. Sensor faults can also be detected based on the comparisons between the fault indicators, i.e., circulating currents and SM capacitor voltages, and their predetermined references.

In [12], two methods are introduced to estimate SM capacitor voltages, namely, the adaptive neuron algorithm and the recursive least square algorithm. Comparison between the estimated results of the two algorithms as well as the SM capacitor voltage reference is used to detect the faulty SM. If the estimated results based on the recursive least square algorithm of a certain SM is 85% lower than the voltage reference, a fault localization step will be activated, where the changing rate of difference between the estimated values of the two capacitor voltage estimation methods will be checked. Since convergence speeds of the two estimation methods are significantly different, the changing rate could be an indicator of the SM fault. If the changing rate of the variance between the two estimated results of a certain SM is larger than a threshold value, the corresponding SM will be detected to be faulty.

Another two-step diagnostic method to detect switching OC fault of MMCs with nearest level modulation is proposed in [16]. In the fault detection step, voltages across arm inductors are measured, since an OC fault of a switching device causes pulse voltages across the inductors. Subsequent to such fault detection, SM capacitor voltages of the faulty phase are compared to different types of threshold values to determine the fault locations and fault characteristics.

In [20], one more method depending on measuring and monitoring the capacitor voltages is proposed to detect and locate the faulty SM. In this diagnostic method, if any SM capacitor voltage is higher than a threshold value, the fault will be detected. If a certain measured SM capacitor voltage mismatches the corresponding estimated value, the fault will be isolated.

TABLE II.
COMPARISON OF THE EXISTING DETECTION METHODS IN THE LITERATURE FOR SWITCHING OC FAULTS IN MMCS.

Ref	Fault Indicator	Extra Sensors	Type of the Diagnostic Method	Diagnostic Level	Detection Duration
[10][23]	Arm current	No	Model based (sliding mode observer)	Phase leg	1.4 ms
	Arm current, SM capacitor voltage	No	Model based (sliding mode observer)	Device	100 ms
[11]	Circulating current	No	Model based (sliding mode observer)	Phase leg	0.4 ms
	Circulating current	No	Model based (sliding mode observer)	Device	50 ms
[18]	Circulating current	No	Model based method (Kalman filter)	Phase leg	1.5 ms
	SM capacitor voltage	No	Signal processing based method	SM	20 ms
[19]	Circulating current	No	Model based (generic state observer)	Phase leg	2 ms
	SM capacitor voltage	No	Signal processing based method	SM	1 ms
[14]	SM capacitor voltage, commanded current through SM	No	Signal processing based method (clustering algorithm)	SM	~ 30 ms
[14]	SM capacitor voltage	No	Signal processing based method	Device	~ 20 ms
[15]	SM capacitor voltage	No	Signal processing based method	SM	600 μs
[21]	Circulating current	No	Signal processing based method	Phase leg	100 ms
	SM capacitor voltage	No	Signal processing based method	SM	20 ~ 50 ms
[12]	Estimation SM capacitor voltages error based on two algorithms	No	Model based method	SM	~ 30 ms
	Changing rage of estimation error	No	Model based method	SM	
[16]	Voltage across arm inductor	Yes	Signal processing based	Phase leg	10 ~ 20μs
	SM capacitor voltage	No	Signal processing based	SM	~ 100 ms
[25]	SM capacitor voltage, voltage across arm, voltage across some SMs	Yes	Signal processing based	SM	~ 2 ms
[24]	Changing rate of arm currents	No	Signal processing based	Device	10 ~ 40 ms
[13]	Circulating current	No	Model based (extended state observer)	Phase leg	~ 100 ms
	Circulating current	No	Model based (extended state observer)	SM	
[22]	Circulating current	No	Model based (sliding mode observer)	Phase leg	< 1 ms
	SM capacitor voltage	No	Signal processing based	SM	1 ~ 60 ms
[20]	SM capacitor voltage	No	Signal processing based	Phase leg	N/A
	SM capacitor voltage	No	Model-based (generic state observer)	SM	N/A
[17]	SM output voltage	Yes	Signal processing based	Device	N/A
[26]	Arm voltage	Yes*	Signal processing based	Phase leg	1 ms
	Arm voltage and switching pattern	Yes*	Signal processing based	Device	1.2 ms
[28]	SM capacitor voltage	No	Signal processing based	Arm	N/A
	SM capacitor voltage	No	Signal processing based	Device	5~30 ms
[29]	Arm voltage	Yes	Signal processing based	Phase-leg	1.5 ms
	SM capacitor voltage	No	Signal processing based	Device	10.3 ms
[30]	SM capacitor voltage, arm currents, load current	No	Signal processing based	SM	< 100 ms
[31]	SM capacitor voltage	No	Signal processing based	Device	< 25 ms
[32]	Arm current and/or SM capacitor voltage	No	Signal processing based	N/A	0.9~12 ms
	Arm current and switching pattern	No	Signal processing based	Device	0.4~6 ms
[33]	Arm voltage	Yes	Signal processing based	Arm	N/A
	Arm voltage and switching signal	Yes	Signal processing based	SM	N/A
[34]	Capacitor voltage and arm current	No	Signal processing based	Arm	<30 ms
	Capacitor voltage and arm current	No	Signal processing based	Device	< 40 ms

* It should be clarified that the extra sensors needed by the fault detection methods are required by their specific supporting control system for the MMC, which are unnecessary for the conventional control methods. Therefore, for the specific MMC control strategies, no extra sensors are needed for the fault detection methods. However, compared with the conventional control strategies, more sensors are needed.

In [24], a method to diagnose a switching OC fault in MMCs through comparing the estimated changing rate of the arm current to the measured result is developed. Based on the abnormal changing rate of the arm current, position of the OC fault in the SM, i.e., the upper switch or the lower switch, can be identified. Additionally, the faulty SM in the MMC is detected by comparing the occurrence moments of the abnormal arm current changing rate to the combinations of the inserted SMs.

Supervisory set sensors and supervisory arm sensors are added to detect different faults in SM, including voltage sensor fault, switching OC fault, and switching SC fault in the power devices [25]. SMs in each arm are divided into several sets. Output voltage of a set is measured by a supervisory set sensor, and a supervisory arm sensor measures output voltage of an arm. Voltage sensors in the SMs for basic voltage balancing

control are termed to be "individual voltage sensor" in [25]. Within each arm, performances of supervisory sensors are checked by comparing the measurement result of supervisory arm sensor and sum of measurement results of supervisory set sensors in the arm. Faults of individual voltage sensor and controllable switches depend on comparisons among the measured output voltages, the expected output voltages, and the "theoretical output voltage" of each set.

In [26], a single open-circuit fault detection method is proposed for the MMC with model predictive control, which takes two steps, i.e., faulty phase leg detection and faulty SM detection. In the faulty phase leg detection step, the common-mode and differential-mode measured arm voltage is compared with the predicted values. Extra sensors to measure the arm voltages are needed in the method. In the faulty SM detection step, the common- and differential-mode voltage errors are used to pinpoint the position of the SM, i.e., the upper one or lower one, in the faulty SM. To determine the faulty SM, the switching patterns of all the SMs are compared with the faulty output voltage flag: if a certain SM is inserted when output voltage is wrong, the corresponding counter of the SM will count up by one. At the end of a preset period, the faulty SM will have the maximum counter output and, thus, can be detected. The fault detection method in [26] is also used to support a fault-tolerance control proposed in [27].

The method proposed in [28] utilizes the single ring theorem (SRT) to observe the distribution of the SM capacitor voltages of each arm in the faulty arm detection step. Under normal condition, the eigenvalues of a capacitor voltage-dependent matrix distribute within a ring, while mean spectral radius of the eigenvalues will decease subsequent to the occurrence of an open-circuit fault. In the faulty SM detection step, the SMs with quartile rule-based outlier capacitor voltages are marked as faulty ones.

A SM capacitor voltage correlation coefficient-based method is proposed in [29] to determine the faulty SMs. After the faulty SM detection mode is activated, the correlation coefficients between the SM capacitor voltages in each arm are calculated. If all the correlation coefficients related to a certain SM is significantly less than 1, the SMs will be marked as faulty ones. The faulty phase leg detection method in [29] is based on the error between measured arm voltages and the predicted arm voltages.

Neural network is applied to detect the OC faults in [30]. The SM capacitor voltages, arm currents, and load currents are segmented and normalized first. Then, the normalized segments are fed into and train a convolutional neural network offline. The trained neural network will receive real-time normalized segments from the MMC and generate a classification vector. The classification results in certain periods will be buffered, and the majority rule will be used to generate the final classification result of the health status of the SMs.

Since normal SMs and SMs with different faulty device has different numbers of voltage variation periods, [31] proposed an index to quantify distributions of SM capacitor voltages, which depends on the number of voltage variation periods. Quartile rule is used to detect the SMs with abnormal indexes, i.e., faulty SMs.

In [32], a set of faulty SM detection method is proposed for the full-bridge SM-based cascaded H-bridge inverter, which is very similar to the MMC. The method also contains two steps, i.e., fault detection and faulty SM detection. In the fault detection step, the error between the measured current and the predicted current is used to indicate the existence of the fault. In the faulty SM detection step, the switch pattern of each devices is compared with the faulty output current. If the measured output current always deviates the predicted value when a certain device should be conducting, the device will be marked as faulty.

In [33] and [34], multiple OC faults with different types are considered. In [33], arm voltage is measured and compared the predicted value. If the predicted and measured ones do not match, the arm is marked as a faulty one. The faulty SM is located through comparing the switching signal and error of the arm voltages. In [34], the capacitor voltage differences are used to pinpoint the position of faulty SM(s). The faulty devices are located based on the capacitor voltage under different current and switching command conditions.

Regarding the diagnosis of an OC fault in the freewheeling diodes in SMs of MMCs, an on-line diagnostic method is proposed in [35]. The diode OC fault is detected based on sensing the voltages across the associated devices, which apparently requires extra voltage sensors, leading to a cost increase. If the voltage across the upper IGBT and anti-parallel diode is lower than zero, the upper diode will be determined to suffer from an OC fault. Similarly, if the voltage across the lower IGBT and diode is lower than zero, an OC fault of the lower diode will be identified.

B. Diagnosis of SC Switching Fault

The most important criterion for the diagnosis of SC switching fault is fast detection speed (i.e., a few microseconds), since long duration of switching SC fault will damage the power devices due to the significant thermal stress resulting from overcurrent. Thus, short-circuit detection is typically implemented through the gate driver hardware circuits for rapid protection, rather than reply on online diagnostic algorithms. The most well-known SC diagnostic method is desaturation detection in which the on-state voltage of the switching device will be detected by a sensing diode and compared to a predetermined value [7][36][37]. To avoid false diagnosis of the SC fault and trigger the protection, this solution requires a programmed delay, the so-called blanking time, of around 1-5 μs to allow collector-emitter voltage to drop below the predetermined threshold voltage during the turn-on switching transients. However, the fault current could boost to a very large value during the blanking time, resulting in degradation and even damage of the switching devices due to pronounced local heating.

Recently, changes in the gate voltage and *di/dt* have been analyzed to identify a short-circuit fault in semiconductor devices [38]-[41]. These protection methods present fast fault detection speed and are preferable to be integrated within a gate

driver chip. Nevertheless, these methods require complicated detection circuitry and are sensitive to gate loop EMI noise caused by parasitic inductance and diode reverse-recovery current, and thus may be challenging in practical applications.

In [42], a *di*/*dt* feedback-based active gate driver is proposed which could improve switching performance during normal turn-on and turn-off transients and also provide fast overcurrent protection under SC faulty condition, especially for shoot-through faults.

Overall speaking, on-line diagnosis of SC switching fault has been paid intensive attention during the past decades and accordingly has become more technically mature compared to the diagnosis of OC switching faults. Therefore, in the literature on diagnosis of switching faults in MMCs, the majority of the references focus on the development of diagnostic method for OC switching faults.

C. Diagnosis of SC Fault on DC Side

For a large-capacity HVDC system, it is desirable that the MMCs connected to the healthy dc lines continue operating without disruption, in the event of a dc fault. This poses the requirement of fast fault detection and faulty line identification to isolate the dc fault promptly and accurately.

The diagnostic techniques for SC fault on the dc bus can be classified into two categories. One is based on the measurement of dc current or voltage, or the currents flowing through the switching devices. Another category is based on the measurement of the derivative of dc voltage or dc current. Their pros and cons will be discussed next. In [43], the dc currents are measured at both ends of each cable and the current difference is used to detect and locate the fault. However, prompt telecommunication speed is required during the implementation, which leads to increased cost and reduced reliability considering potential communication interruption. In [44], the dc current is measured locally to improve the fault detection reliability, which actually takes longer time to detect the fault and the accuracy of the fault identification is of a concern. Another diagnostic method based on the measurement of derivative of dc voltage is proposed in [45] to quickly detect and locate dc faults in a bipolar HVDC grid. However, the impact of the arm inductor was not considered and it was assumed that the converter output voltage remains unchanged immediately following a dc fault. Moreover, high derivative of dc voltage is observed when the fault is cleared by circuit breakers, resulting in interference to the protection controller. In [46], the dc current derivative is used to detect a dc fault. However, a dc capacitor is connected at the station to support the dc voltage and the circuit breaker opening time is not considered. The severe transients following the fault clearance may also falsely trigger protection on adjacent healthy dc cables.

D. Diagnosis of SLG Fault on AC Side

As mentioned earlier, in a typical MMC-HVDC transmission systems, SLG faults for MMCs are classified into three types depending on the fault location, namely, SLG fault in the primary side of the transformer, SLG fault in the secondary side of the transformer, and SLG fault in transformerless applications. Here, the focus will be on the scenarios when MMCs are operated as the inverter (i.e., power dispatcher). In [57], it shows that monitoring the variation of the double line frequency ripples in the dc voltage can be used to diagnose the SLG fault. Additionally, symmetrical components of the arm voltage and current of the MMCs can also be extracted and monitored to identify an SLG fault, due to the unbalance characteristics once an SLG fault occurs. In [58], dc-bus overvoltage due to the double line frequency oscillation and abrupt SM voltage increase are monitored to determine an SLG fault.

In [59], the presence of zero-sequence current is used as an indication of the SLG fault at the valve side of a FB-MMC, which can be expressed as follows:

$$i_o = \left|\left(i_a + i_b + i_c\right)/3\right| \geq i_T \tag{6}$$

where, i_o is the zero-sequence current and i_T is a threshold value. If the magnitude of i_o is higher than the threshold, a SLG fault will be identified.

Since SLG fault is an asymmetrical fault, negative-sequence components and the doubled frequency fluctuation in the active power are used in [60] as the diagnostic method for SLG faults. Specifically, the active power during normal operation can be expressed in synchronous reference frame as:

$$p_s = \frac{3}{2}\left(u_d i_d + u_q i_q\right) \tag{7}$$

where, u_d and u_q refer to the voltages in synchronous reference frame, and i_d and i_q refer to the current in synchronous reference frame. Once the negative components present in the MMC system, the active power will become:

$$\begin{aligned} p_s = {} & \frac{3}{2}\left(u_d^+ i_d^+ + u_q^+ i_q^+\right) + \frac{3}{2}\left(u_d^- i_d^- + u_q^- i_q^-\right) + \frac{3}{2}\left(u_d^+ i_d^- + u_q^+ i_q^- + u_d^- i_d^+ \right. \\ & \left. u_q^- i_q^+\right) + \cos\left(2\omega t\right) + \frac{3}{2}\left(u_d^+ i_q^- - u_q^+ i_d^- + u_q^- i_d^+ + u_d^- i_q^+\right)\sin\left(2\omega t\right) \end{aligned} \tag{8}$$

here, u_d^+, i_d^+, u_q^+, and i_q^+ refer to the positive-sequence of the voltage and current. Likewise, u_d^-, i_d^-, u_q^-, and i_q^- refer to the negative-sequence voltage and current. Comparing (3) to (2) shows that the active power injected into the converter contains not only the dc component but also the second harmonic component when an SLG fault occurs.

IV. Fault Tolerant Operation Methods

Once a fault in MMC is detected and identified, the availability of a fault-tolerant operation solution will be required to ensure continued system function and minimize downtime cost. Existing fault-tolerant solutions to switching OC fault, dc-bus short-circuit fault, and SLG fault on the ac side will be reviewed in this section. For the switching short-circuit faults, the ultimate consequence will be the same as open-circuit device faults due to the interruption of gate signals, so the associated fault-tolerant operation strategy will be assumed the same as these for open-circuit faults.

A. Switching OC Fault Tolerance

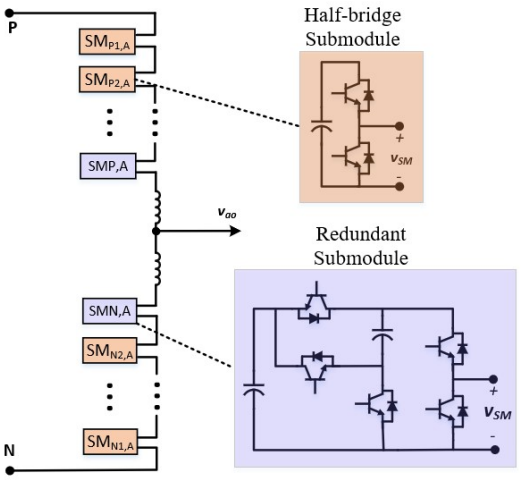


Fig. 6. Circuit topology of the fault-tolerant MMCCC.

The existing fault-tolerant solutions to switching OC faults in MMCs presented in the literature can be classified into two categories, i.e., one is redundant switching states based fault-tolerant operation strategies, another is redundant hardware (converter bridges or SMs) based fault-tolerant strategies. The former typically can keep the system operating continuously without any additional hardware requirements but with derated system output performance (i.e., lower output voltages, higher harmonic distortions, lower power, etc.), while the latter can maintain the rated performance but requiring additional converter bridges or submodules with increased system cost and perhaps reduce converter efficiency. The trade-off between these two solutions depends on a comprehensive consideration of the system cost, reliability priority, and system performance.

1) Redundant Switching States based Strategies

A so-called "seamlessly ride-through" fault-tolerant control strategy was proposed in [15], in which the PWM references are modified on-line for active compensation of the voltage disturbances caused by the OC faults, while the localization of the faulty SM is in the process. Once the localization of the faulty SM is completed, the faulty SM is isolated by closing the bypass switch and the corresponding fault flag will be cleared. Subsequently, the fault-tolerant operation mode will be activated.

In [17], another fault-tolerant approach was developed based on modifying capacitor reference voltages and modulation reference waveforms in the faulty leg of MMC while other legs operate normally. This new approach may cause some degree of overvoltage in faulty leg capacitors. However, such overvoltage can be neglected since the number of SM cells is generally high.

2) Redundant Converter Bridges or SMs based Strategies

In [21], a multilevel modular capacitor-clamped dc/dc converter (MMCCC) is integrated into each arm of the MMC to handle both single and simultaneous OC faults, as shown in Fig. 6. This proposed converter provides both redundancy and modularity and ensures smooth transients subsequent to fault occurrence. In the event of a component failure, the supervisory algorithm diagnoses the fault and isolates the corresponding faulty submodule. Afterwards, the post-fault restoration unit activates a number of redundant modules of the MMCCC by adapting the gate switching signals.

In [22], a novel spare process is proposed to handle an emergency situation when the number of faulty power modules exceeds the module redundancy. Since topological redundancy may cause the switching commutations of power modules in an arm to be unevenly distributed, a mitigation measure is incorporated to keep the energy balance while avoiding the undesired switching stress.

In [24], it shows that a fundamental component is caused in the inner difference current in the faulty phase after bypassing the faulty SMs, which would increase the dc-bus current ripple and capacitor voltage unbalance between the upper arm and lower arm. To eliminate the fundamental component in the inner difference current, a fault-tolerant approach based on PI controller is developed to maintain the performance of the MMC after bypassing the faulty SMs. This fault-tolerant control approach can be realized without the information of the number of faulty SMs in the arm and without extra demand on the communication systems.

In [25], redundant SMs are added to MMC to provide back-up options when a SM failure occurs. However, it should be noted that these redundant SMs are in cold reserve state by closing the bypass switches. When the SM faults occur, the corresponding faulty SMs must be bypassed. Meanwhile, the same number of redundant SMs will be activated by opening their bypass switches and charging the capacitors to the rated values before operating it as normal SMs. Since the capacitor charging will take tens or even hundreds of milliseconds, the output voltage waveforms of the arm will be distorted, which is a major drawback of this fault-tolerant scheme.

Unlike the fault-tolerant scheme proposed in [22], the redundant SMs are kept in spinning reserve state in normal operation. When a SM fails, there are two strategies to be considered. One is bypassing the faulty SMs as well as the same number of SMs in other arms to keep the system balanced. The other is to bypass the faulty SMs and keep the system working under unbalanced condition. To keep the MMC operating normally under SM faulty conditions, an energy-balancing control strategy is proposed in [23].

B. DC Short-Circuit Fault Isolation and Tolerance

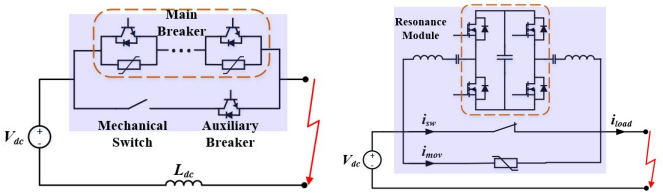
As mentioned in Section II, if a short-circuit fault occurs in the dc side of the MMC, the MMC will perform as an uncontrolled rectifier that allows the ac system to feed the load with very high current through the freewheeling diodes. To retire this potential concern, different solutions have been proposed in the literature, which will be detailed as follows:

1) Circuit Breakers

The most straightforward approach to isolate a dc short-circuit fault is by installing circuit breakers on the dc bus to promptly interrupt the short-circuit inrush current. However, the lack of zero-crossing in the dc current as well as the slow protection speed pose challenges on using the conventional

mechanical breakers for dc fault protection, although it has the benefit of ultra-low on-state conduction losses.

As a result, there are two types of solutions proposed in the literature, one is hybrid dc breaker, another is pure solid-state circuit breaker. In [61], a hybrid dc breaker is introduced, and the circuit topology is shown in Fig. 7(a). The main path consists of an ultra-fast mechanical disconnector in series with a low-voltage solid-state semiconductor switch, as well as a parallel path, i.e., main breaker path built by series connection of solid-state switches. During normal operation, the current will only flow through the main path, and the conduction losses are low due to the utilization of mechanical disconnector and low-voltage switches. Once a dc short-circuit fault occurs, the auxiliary breaker commutes the current to the main breaker, and the mechanical disconnector opens. Afterwards, the main breaker interrupts the dc current, and then the mechanical switch opens with zero current and low voltage stress. Another type of the hybrid dc breaker is based on resonant current modules, as shown in Fig. 7(b). During normal operation, the current flows through the vacuum interrupter, and the on-state conduction loss is very low. Once a dc fault occurs, the resonant current source will be activated and ramps up to oppose the fault current in the vacuum interrupter to force a zero current. During post-fault operation, the metal oxide varistor in the energy absorption branch clamps overvoltage and dissipates residual line current and energy [62]. Other derivatives of hybrid dc breaker are introduced or summarized in [47]-[49].



(a) (b)

Fig. 7. Hybrid dc circuit breakers (a) based on auxiliary switches (b) based on resonant current source modules.

Moreover, there have been attempts to develop pure solid-state dc breakers based on high-voltage semiconductor switches, but the on-state conduction losses will be much higher [63][64]. The recently emerging high-voltage Silicon Carbide MOSFETs, such 3.3 kV, 6.5 kV and 10 kV, may provide a feasible solution in the near future for developing solid-state breakers [65].

2) Full-Bridge SMs

Other solutions to isolate and tolerate a dc short-circuit fault in MMCs is to use full-bridge SMs (FBSMs) instead of the half-bridge SMs [50]-[52]. The FBSMs can be controlled to inject the capacitor voltages of opposite polarity, which can be used to limit or block the fault current. However, this method requires doubling of the number of semiconductor switches in the conduction path, resulting in higher semiconductor device losses and higher system cost.

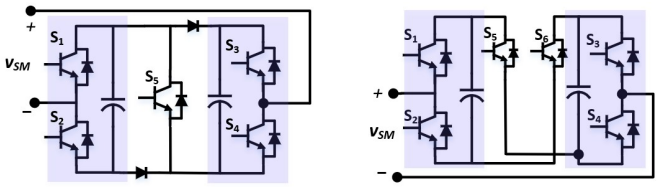
An intermediate solution that utilizes a hybrid combination of the HBSMs and FBSMs is proposed in [71]. In this hybrid MMC, if the series voltage formed by all the FBSM capacitor along a fault current path is higher than the ac line-to-line voltage, a dc fault can be blocked once all the semiconductor switches are turned off. The minimum number of FBSMs within each arm is designated as:

$$\mathrm{F} \geq \frac{\sqrt{3}}{4}(N+M) \tag{9}$$

where, F is the number of FBSMs, N is the total number of SMs in each of the two arms in each phase leg, and M is the number of FBSMs that are allowed to generate negative dc-bus voltage in each arm (M<F). For instance, one scenario is that half of the SMs are FBSMs and another half are HBSMs where the conventional control strategies for HB-MMC can be adopted.

3) Other Modified SMs

In addition to employing FB-MMCs for providing a ride-through strategy to dc short-circuit faults, a few other solutions based on modifying the HBSMs have been developed with dc fault blocking capability [53]-[55]. In [53], a clamp-diode SM (CDSM) circuit is presented, the topology of which includes two serial HBSMs plus one IGBT and two diodes, as shown in Fig. 8(a). In normal operation, the CDSM is equivalent to two serial HBSMs, since the IGBT S_5 is kept constant-off. Whenever a dc fault occurs, S_5 will be turned off to ensure the short-circuit fault current has two parallel conduction paths to flow through half capacitors in each arm, which can provide enough reverse voltage to push the fault current to zero. It can be seen that this strategy has dc fault blocking capability, but the associated device losses and hardware cost will be increased. Likewise, another solution based on a modified SM consisting of two cross-connected HBSMs through two IGBTs and two diodes is introduced in [54], as shown in Fig. 8(b). One benefit of this SM circuit is that it can generate five-level output voltages ($\pm 2V_{dc}$, $\pm V_{dc}$ and 0) in normal operation. If a dc short-circuit fault occurs, the fault current flows through all capacitors in each arm, producing the reverse voltage to reduce the fault current to zero. However, one drawback with this proposed solution is the significant double capacitor voltage stress in the IGBTs S_5 and S_6. More fault-tolerant SM topologies are discussed in [55], and will not be repeated here.



(a) (b)

Fig. 8 Modified HB-MMC (a) clamp-double SM. (b) crossed connected SM.

C. SLG Fault Ride-Through Strategies

As mentioned in Section II, when an SLG fault occurs to the MMC systems, there will be undesired ac voltage sag and reduced instantaneous power. To overcome such issues, a few FRT strategies have been proposed in the literature. In [57], a generalized instantaneous power of a phase unit is derived from the equivalent circuit model of the MMC under unbalanced

conditions. Based on this model, a novel double-line frequency dc voltage ripple suppression control is proposed. Targeting at all the three possible SLG faults, the FRT strategy together with the negative-sequence and zero-sequence current control, is demonstrated to enhance the overall fault-tolerant capability of the MMC system without additional cost. In [66], a voltage margin control method based on using transmission line voltage as a reference signal is proposed to coordinate two MMC stations in the HVDC system to protect the MMCs against the SM capacitor overvoltage in case of the SLG fault. It also demonstrates that the 2nd order voltage and current fluctuations in the transmission lines caused by the grid unbalance are avoided. In [67], a feedback/feed-forward control strategy is proposed to improve the voltage balancing of MMCs under unbalanced grid conditions, which improves the disturbance rejection capability against asymmetrical faults such as SLG faults. Additionally, a control strategy combining the multi-hierarchy control with the arm current control for MMCs under SLG fault is proposed in [68]. Regarding the implementation of this multi-hierarchy control method, the symmetrical ac-side current references and the unevenly distributed dc current references in three legs can be obtained by three voltage controllers in the *abc* coordinate, avoiding coordinate transformation and using numerous filters in the existing methods. In [69], to reduce the significant voltage ripples in MMCs based on FBSMs under SLG fault conditions, a circulating current injection method is proposed to suppress the main components of the fundamental frequency fluctuations.

Targeting at mitigating the overvoltage on the SM capacitors in converter upper arms and the non-zero-crossing currents in the grid-side ac circuit breaker, a double-thyristors hardware approach is introduced in [70]. In this approach, the double-thyristors are installed in parallel with each SM in the lower arms of the converter, as shown in Fig. 9. By triggering the double-thyristors, an SLG fault will be converted into a three-phase short-circuit than ensures current zero-crossing in the ac circuit breaker for fault protection.

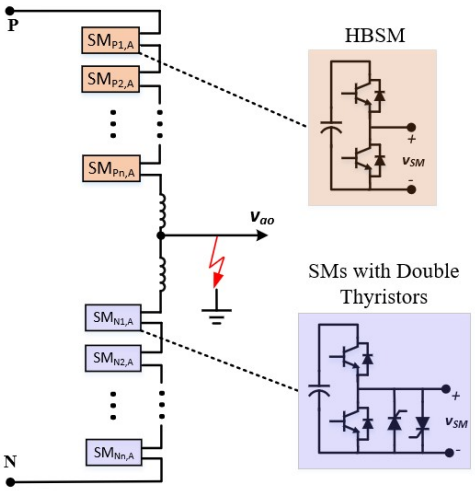


Fig. 9 HB-MMC with double thyristors installed at the lower arm.

V. Conclusion

Fault diagnosis and fault-tolerant operation of MMCs play a paramount important role for their further penetration into broader industrial applications. In this paper, a comprehensive review of existing fault detection methods and fault tolerant strategies for MMCs has been conducted. Diagnostic techniques for internal switch open-circuit faults, short-circuit faults, dc-bus short-circuit faults, and ac-side SLG faults have been reviewed. Accordingly, the fault-tolerant solutions to these various types of MMC faults are investigated. Such a comprehensive review and summary of the fault diagnostic and fault-tolerant solutions of MMCs presented in this paper aims to provide a state-of-the-art reference for the development of high-reliability MMCs in future.

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