A Novel Single-Phase Five-Level Transformer-less Photovoltaic (PV) Inverter

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***Abstract*— Multilevel inverters are preferred solutions for photovoltaic (PV) applications because of lower total harmonic distortion (THD), lower switching stress and lower electromagnetic interference (EMI). In order to reduce the leakage current in the single-phase low-power PV inverters, a five-level transformer-less inverter is proposed in this paper. A total of eleven switches are required, while six of them only withstand a quarter of the dc-bus voltage, so the costs for them are low. Another four switches are turned on or off at the power line cycle, the switching losses for them are ignored. In addition, the flying-capacitors (FCs) voltages are only a quarter of the dc-bus voltage, and they are balanced at the switching frequency, which further reduces the system investment. The experimental results based on a 1 kW prototype show that the proposed modulation strategy can balance the FCs voltages at $V_{dc}/4$ very well. And the leakage current can be reduced to about 27 mA under both active and reactive operations, which satisfies the VDE 0126-1-1 standard.**

***Index Terms*—Leakage current, multilevel inverter, pulse width modulation.**

I. INTRODUCTION

IN the past decades, new energy power generations, such as photovoltaic (PV), have rapidly developed due to their unique advantages in little pollution and emission [1], [2]. The multilevel transformer-less inverters play an important role in the single-phase low-power PV system due to their small size and weight, low cost, and high efficiency [3], [4]. However, a galvanic connection exists between the PV inverter and the ground without isolation; The leakage current will flow through the main circuit and ground. In particular, the leakage current will cause various problems, such as losses, electromagnetic interferences and harmonic distortion. The leakage current will also threaten personal safety if there are directly contacts with the PV panels. Thus, a few German codes, such as VDE 0126-1-1, impose that the PV panels should be disconnected from the grid within 0.3 s if the RMS value of leakage current exceeds 300 mA [5].

The leakage current elimination issue has attracted an increasing attention and has been widely explored by experts and scholars. Generally, the common-mode (CM) filters are often used to reduce the leakage current. The mechanism of CM filter is to increase the impedance of CM paths. Different types of CM filter structures have been presented to reduce the leakage current [6]-[8]. The CM paths for the cascaded inverters are discussed in [9], and two filter-based solutions are provided to cutoff the leakage current paths. Then, the leakage current can be effectively reduced. However, the volume, weight and investment of the total system will increase with the increasement of modules. In order to compensate the influences of parasitic capacitors on the CM paths, the additional capacitor, which connects the dc-bus midpoint and ground, is added in [10]. Generally, the parasitic capacitors are different and depend on the system capacity. Thus, the scope of application of this method is limited. A new structure of active EMI filter (AEF) is proposed in [11], however, the AEF has a drawback in reliability and safety. In short, it is difficult to adapt to all applications by changing the hardware method, and it will increase the complexity of the system.

It is an excellent scheme to reduce the leakage current from the perspective of inverter topology and modulation. Its mechanism is to separate the PV array from the grid in the freewheeling period. Based on this, some active switches are added to the DC or AC side as the decoupling network. For example, the H5 topology in Fig. 1, the Highly Efficient Reliable Inverter Concept (HERIC) topology in Fig. 2, and the H6 topology in Fig. 3 [12]-[14]. An improved H6 transformer-less inverter topology is generated in [15]. Two additional switches are added to the DC side to balance the switching loss distribution for the high-frequency switches. One of the decoupling switches can be shifted from the main branch to the bypass branch, which is given in [16], to reduce the conduction loss. In order to overcome the drawbacks of conventional H6 topologies regarding reactive power capability, some improved H6-type topologies are proposed in [17], [18]. Some extra switches and diodes on the dc side are induced such as H6 dc side-1 and H6 dc side-2 [19] topologies. They are called dc decoupling-based transformer-less inverter topologies.

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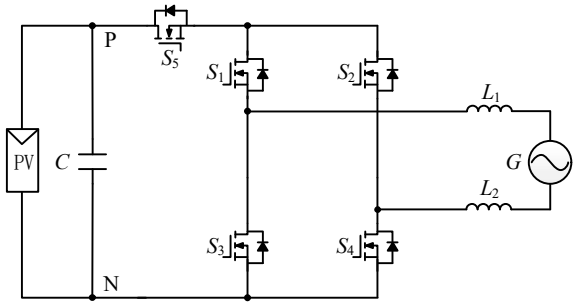

Fig. 1. H5 topology.

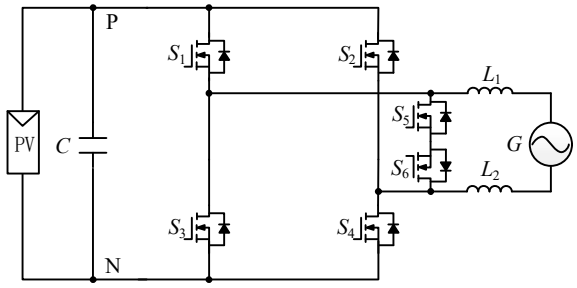

Fig. 2. HERIC topology.

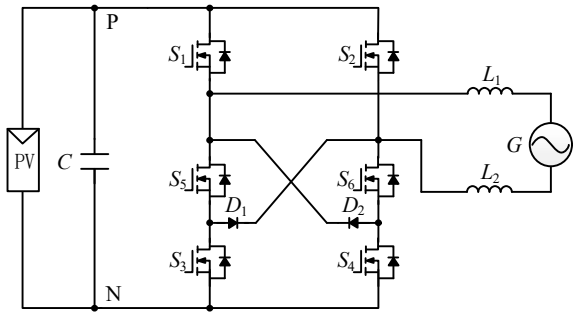

Fig. 3. H6 topology.

Unfortunately, due to the existing of the junction capacitors of active switches, the decoupling network cannot be truly realized. The additional leakage current paths will be established again by the junction capacitors. Thus, the CM voltage should be maintained constant by clamping it to the half dc-bus voltage. In accordance with this principle, some enhanced transformer-less inverter topologies with additional freewheeling paths are presented in [20], [21]. A new solution called oH5 topology [22] is a bidirectional clamping circuit. It is based on the H5 topology and has an additional active switch that turns on in the freewheeling mode to maintain a constant CM voltage. A full-bridge zero-voltage state rectifier (FB-ZVR) topology is proposed [23], however it suffers from high conduction losses because the current flows through four switches in the positive period. In [24], two unidirectional freewheeling paths are added to the AC side of the full-bridge inverter. The branches can clamp the CM voltage at half the dc-bus voltage whenever the potential of the freewheeling path falls or rises. By combining the MOSFETs and SiC diodes, a family of single-phase grid-tied PV inverters are proposed in [25]. They can achieve both the performances of high efficiency and high reliability. Other midpoint clamping topologies such as HERIC Active [26], PN-NPC [27], HB-ZVR-D [28] are proposed in the literature to further reduce the leakage current. In order to find all topologies with leakage

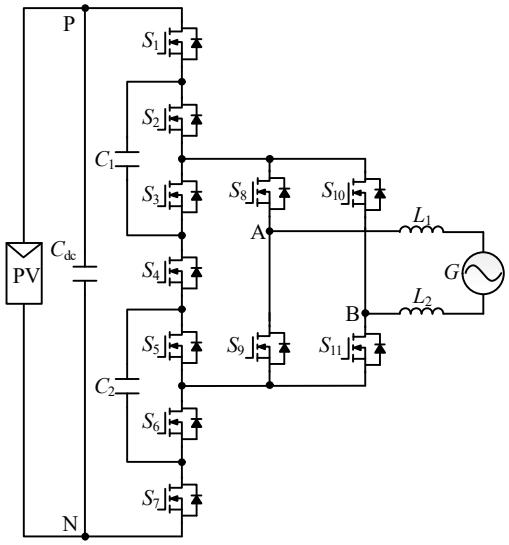

Fig. 4. Proposed single-phase five-level inverter topology.

the transformer-less single-phase full-bridge topology synthesis methods are proposed in [29] and [30].

All the above researches focus on single-phase three-level applications. Unfortunately, the typical single-phase five-level transformer-less topologies such as H-bridge neutral point clamped (HB-NPC) [31], H-bridge flying-capacitor (HB-FC) [32] and cascaded H-bridge (CHB) [33] suffer from the same serious leakage current as three-level topologies. Several topologies have been proposed to deal with the leakage current in the five-level applications. An asymmetrical T-type five-level transformer-less single-phase inverter (5L-T-AHB) is proposed in [34]. However, it cannot maintain a constant CM voltage at the voltage zero crossing. Some cascaded five-level topologies are presented in [35]-[37], they also bring other problems, for example, the insulation voltage to ground of PV panel needs to be doubled. The common ground topologies [38], [39] are also better solutions. However, the negative of the dc-bus cannot be grounded when the inverter is connected with the EMI filters. Further, it is necessary to do more in-depth research for the single-phase five-level PV inverter.

Based on this, a single-phase five-level transformer-less PV inverter is proposed in this paper. The rest of the paper is organized as follows. Section II gives the circuit configuration and operating principles of the proposed inverter. Section III gives the modulation strategy under both active and reactive power conditions, and the FC voltage balance method is also drawn. Section IV gives a comprehensive analysis in terms of devices voltage stresses, and a comparison with some existing topologies has also been provided. Section V presents the simulation and experimental results, and Section VI elaborates the conclusions.

II. Proposed Single-Phase Five-Level Inverter

A. Proposed Single-Phase Five-Level Inverter

Fig. 4 shows the schematic of the proposed inverter. C_{dc} is the dc-bus capacitor, C_1 and C_2 are the FCs, L_1 and L_2 are the symmetrical filter inductors. S_1–S_{11} are eleven switches, of them, switches S_1–S_7 are arranged in I-type, while S_8–S_{11} forms

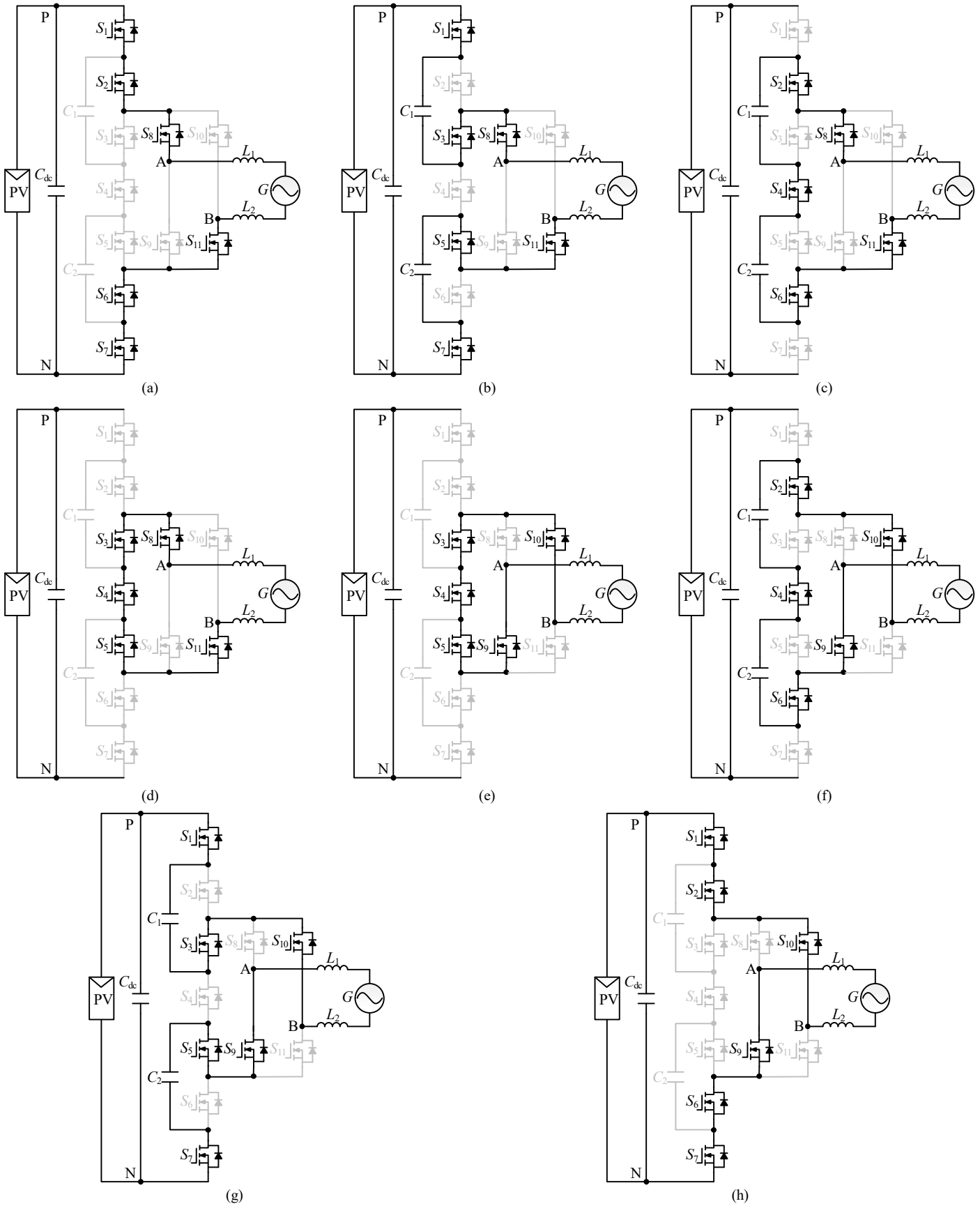

Fig. 5. Switching states for the proposed inverter. (a) State A: $+V_{dc}$. (b) State B: $+V_{dc}/2$. (c) State C: $+V_{dc}/2$. (d) State D: 0. (e) State E: 0. (f) State F: $-V_{dc}/2$. (g) State G: $-V_{dc}/2$. (h) State H: $-V_{dc}$.

TABLE I
SWITCHING STATES, OUTPUT VOLTAGES, CM VOLTAGES AND IMPACT ON THE FCS

	Voltage				$i_{out}>0$		$i_{out}<0$	
No	V_{AN}	V_{BN}	V_{AB}	V_{CM}	C_1	C_2	C_1	C_2
A	+4	0	+4	+2	-	-	-	-
B	+3	+1	+2	+2	↑	↑	↓	↓
C	+3	+1	+2	+2	↓	↓	↑	↑
D	+2	+2	0	+2	-	-	-	-
E	+2	+2	0	+2	-	-	-	-
F	+1	+3	−2	+2	↑	↑	↓	↓
G	+1	+3	−2	+2	↓	↓	↑	↑
H	0	+4	−4	+2	-	-	-	-

"↓" means decrease; "↑" means increase; and "-" means no impact.

a H-bridge. The dc-bus voltage is defined as V_{dc}. For the proposed inverter, five-level voltages, which are V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$, can be obtained. Notably, in order to achieve a constant CM voltage, the voltages of C_1 and C_2 are charged to a quarter of the dc-bus voltage ($V_{dc}/4$) firstly. And then they can be balanced constant by the proposed modulation strategy within one switching period. Thus, the investment cost of FCs may be lower than that of conventional FC-based topologies.

B. Operation of the Single-Phase Five-Level Inverter

The CM characteristic of the proposed single-phase five-level transformer-less inverter is discussed in this section to demonstrate the reduction principle of the leakage current.

The PV inverters are generally equipped with a filter that is composed of a pair of symmetrical inductors. The CM voltage V_{CM} is derived as (1) from the CM loop model [10], where V_{AN} and V_{BN} are bridge voltages with a reference of the negative of the PV panels N.

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{1}$$

The leakage current can be expressed as (2).

$$i_{leakage} = C_{PV} \frac{dV_{CM}}{dt} \tag{2}$$

where C_{PV} is the parasitic capacitor between the PV panels and the ground, $i_{leakage}$ is the leakage current.

According to (2), if the CM voltage is kept constant all the time, the leakage current will be reduced theoretically. In order to obtain the CM voltage of the inverter, the detailed equivalent circuit of each switching state is provided as shown in Fig. 5. Seen from Fig. 5, a total of eight switching states, named from A to H, are obtained. The CM voltage V_{CM} and the output voltage V_{AB} for each switching state can be deduced from each switching state.

State A: Switches S_1, S_2, S_6, S_7, S_8 and S_{11} are on as shown in Fig. 5(a). The potentials at points A and B are V_{dc} and 0, respectively. Thus, V_{AB} is $+V_{dc}$, and V_{CM} is $V_{dc}/2$.

State B: Switches S_1, S_3, S_5, S_7, S_8 and S_{11} are on as shown in Fig. 5(b). Both C_1 and C_2 are charged because the currents flowing them are the output current. The potentials of A and B are obtained by summing the dc-bus and FC voltages. As a result, V_{AN} is $3V_{dc}/4$ and V_{BN} is $V_{dc}/4$. V_{CM} and V_{AB} are all $V_{dc}/2$.

State C: Switches S_2, S_4, S_6, S_8 and S_{11} are on as shown in Fig. 5(c). This is a freewheeling mode. The output current is still positive, but the currents flowing through C_1 and C_2 are negative. Thus, both C_1 and C_2 are discharged. According to the analysis in [15], $V_{AN} \approx 3V_{dc}/4$ and $V_{BN} \approx V_{dc}/4$. Therefore, V_{CM} and V_{AB} are all $V_{dc}/2$.

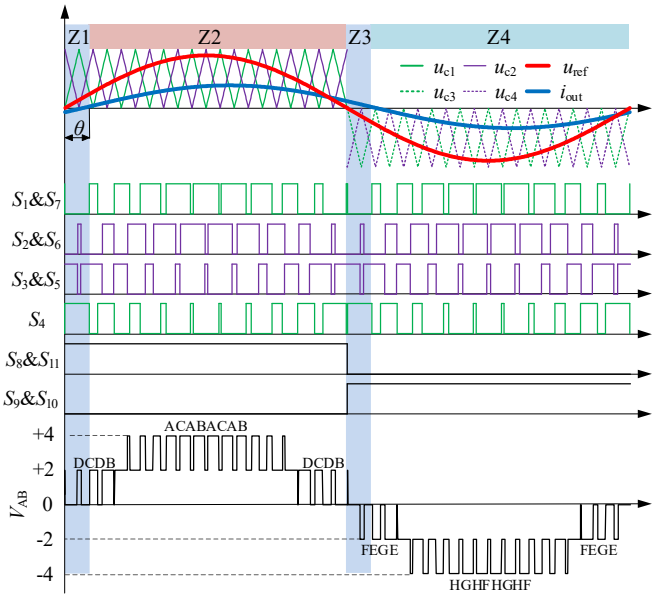

Fig. 6. Modulation method for the proposed inverter.

State D: Switches S_3, S_4, S_5, S_8 and S_{11} are on as shown in Fig. 5(d). C_1 and C_2 are not involved in the output current path, so they are not affected. According to [15], $V_{AN} = V_{BN} \approx V_{dc}/2$. Therefore, V_{CM} is $V_{dc}/2$ and V_{AB} is 0.

State E: Switches S_3, S_4, S_5, S_9 and S_{10} are on as shown in Fig. 5(e). This is similar to state D. The difference is that switches S_8 and S_{11} are switched to S_9 and S_{10}. So the output current is negative. Finally, $V_{AN} = V_{BN} \approx V_{dc}/2$, V_{CM} is $V_{dc}/2$ and V_{AB} is 0.

State F: Switches S_2, S_4, S_6, S_9 and S_{10} are on as shown in Fig. 5(f). The potentials of A and B are similar to that in state C. However, the potentials of A and B are swapped because of the on-state switches S_9 and S_{10}. So V_{CM} is $V_{dc}/2$ according to (1), and V_{AB} is $-V_{dc}/2$.

State G: Switches S_1, S_3, S_5, S_7, S_9 and S_{10} are on as shown in Fig. 5(g). Obviously, V_{AN} is $V_{dc}/4$ and V_{BN} is $3V_{dc}/4$. So V_{CM} is $V_{dc}/2$ and V_{AB} is $-V_{dc}/2$. Both C_1 and C_2 are charged by the output current.

State H: Switches S_1, S_2, S_6, S_7, S_9 and S_{10} are on as shown in Fig. 5(h). V_{AN} is 0, V_{BN} is V_{dc}. So V_{CM} is $V_{dc}/2$ and V_{AB} is $-V_{dc}$.

The aforementioned analysis indicates that the CM voltage in each state is maintained at $V_{dc}/2$ and does not exhibit any high frequency component. The leakage current will be practically reduced. The bridge voltages, output voltage, and CM voltage are summarized in Table I. In Table I, the bridge voltage levels V_{dc}, $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$, and 0 are defined as 4, 3, 2, 1 and 0, respectively. The output current is defined as i_{out}. As shown in the table, three pairs of redundant switching states generate the same output voltage level: states B and C are redundant switching states to generate +2 voltage level; (D, E) and (F, G) are redundant switching states to generate 0 and −2, respectively. However, the effect of different redundant switching states on the FCs is opposite due to the different directions of the charging current. It leads to the possibility of regulating the FCs voltage to a constant value.

TABLE III
COMPARISON WITH EXISTING TOPOLOGIES

	No. of switch			No. of diodes			No. of dc capacitor			No. of dc source	Voltage levels	Constant CMV
	V_{dc}	$V_{dc}/2$	$V_{dc}/4$	V_{dc}	$V_{dc}/2$	$V_{dc}/4$	V_{dc}	$V_{dc}/2$	$V_{dc}/4$			
Pro.	4	1	6	0	0	0	1	0	2	1	5	Yes
HB-NPC	0	8	0	0	4	0	0	2	0	1	5	No
HB-FC	0	8	0	0	0	0	1	2	0	1	5	No
5L-T-AHB [34]	4	2	0	0	2	0	0	2	0	1	5	No
Cascaded-H5 [35]	0	10	0	0	0	0	0	2	0	2	5	Yes
Common Ground [38]	2	4	0	1	0	0	2	1	0	1	5	Yes
H5 [12]	4	1	0	0	0	0	1	0	0	1	3	Yes
HERIC [13]	6	0	0	0	0	0	1	0	0	1	3	Yes
H6 [14]	4	2	0	0	2	0	1	0	0	1	3	Yes

III. MODULATION STRATEGY

The modulation method for the proposed inverter under both active and reactive operations is shown in Fig. 6. The red line represents the reference u_{ref}. u_{c1}, u_{c2}, u_{c3} and u_{c4} are four carriers. The output current i_{out}, which is represented by the blue line, lags behind u_{ref} with a phase angle θ.

Seen from Fig. 6, the full period of u_{ref} is divided into four zones based on the polarities of u_{ref} and i_{out}. When u_{ref} and i_{out} are in opposite direction, they are identified as reactive power zones such as Z1 and Z3. When u_{ref} and i_{out} are in the same direction, they are identified as active power zones such as Z2 and Z4. In each region, the selection of switch state should be based on the principle of keeping capacitor voltage balance. The selection of switch state will be described in detail below.

During zone Z1, V_{AB} switches between the two adjacent voltage levels of +2 and 0. +2 voltage level is generated by switching states B and C, and 0 voltage level is generated by switching state D. Because switching states B and C have opposite effect on the FCs voltages, they are assigned on both sides of the switching state 0, then the switching sequence (BCBD) is obtained. In addition, all these switching states can provide bidirectional current path, that is to say the selection of switching sequence only depends on the output voltage level and has nothing to do with the direction of output current, which makes it easier to implement.

During zone Z2, the output current is positive. The selection principle of switching sequence is the same as that during zone Z1 when the output voltage is switched within +2 and 0 voltage levels. When the output voltage is switched within +4 and +2 voltage levels, the switching state A is used to generate +4 voltage level, and it has no influence on the FCs voltages. Switching states B and C are also used to generate +2 voltage level. In this way, the FCs voltages can also be balanced within the switching frequency.

During zone Z3, the output current is positive, but the output voltage is negative. Similarly, −2 voltage level is generated by two redundant switching states F and G, so as to balance the FCs voltages. 0 voltage level is generated by switching state E. Thus, the switching sequence (EFEG) is acquired in zone Z3.

During zone Z4, both the output voltage and current are negative. Two redundant switching states F and G are used to balance the FC voltage and switching state H is used to generate +4 voltage level. Finally, the switching state rotates in the sequence of (FHGH).

By the selection of the redundant switching states, the voltages of two FCs can be balanced at $V_{dc}/4$ at the switching frequency. In addition, the voltage stresses of two FCs are only $V_{dc}/4$, which will lead to a reduction in system cost and volume. The equivalent switching frequency of the output voltage V_{AB} is twice the actual switching frequency because of the phase shift between the carriers. As a result, the size and cost of the filter can be very small. In general, the investment in passive components of the proposed topology is relatively small.

IV. COMPREHENSIVE ANALYSIS

A. Voltage Stress on Switching Devices

The voltage stress and switching frequency for all switches are listed in Table II. Four switches S_2, S_3, S_5 and S_6 are clamped by two FCs. So the voltage stresses of them are all $V_{dc}/4$. The voltage stress of S_4 can be obtained from switching state B as shown in Fig. 5(b), and the voltage stresses of S_1 and S_7 can be obtained from switching state C as shown in Fig. 5(c). The last four switches need withstand the whole dc-bus voltage as shown in Fig. 5(a) and Fig. 5(h).

In addition, seven switches (S_1−S_7) are turned on or off at the switching frequency (f_s), while four switches (S_8−S_{11}) are at the power line frequency (f_L). In order to reduce the total system investment, MOSFETs can be selected for S_1−S_7 and IGBTs are selected for S_8−S_{11} in actual application.

TABLE II
VOLTAGE STRESS AND SWITCHING FREQUENCY OF DEVICES

Device	Voltage Stress	Switching Frequency
S_1, S_2, S_3, S_5, S_6, S_7	$V_{dc}/4$	f_s
S_4	$V_{dc}/2$	f_s
S_8, S_9, S_{10}, S_{11}	V_{dc}	f_L

B. Comparison with Existing Topologies

Table III presents a comparison of several key features of the proposed topology with some existing topologies. These topologies include conventional H-bridge inverters, cascaded inverters and common ground inverters. The number of active and passive components, voltage stress, required dc source and CM voltage (CMV) are concisely shown here for comparison.

Compared with conventional single-phase five-level topologies such as HB-NPC, HB-FC and 5L-T-AHB, the investment cost of switches may be higher. However, the CMV of the proposed topology is clamped at $V_{dc}/2$, achieving low leakage current. Thus, the isolation transformer and EMI filters

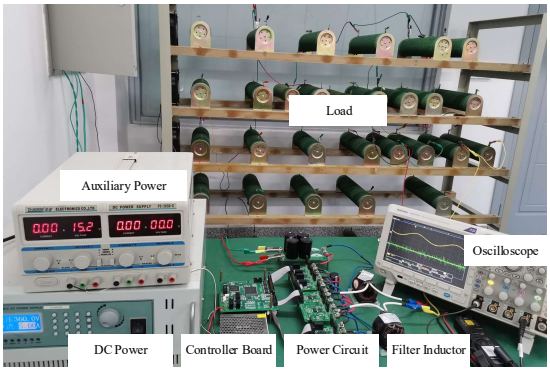

Fig. 7. Picture of the prototype.

TABLE IV
SYSTEM PARAMETERS

Description	Symbol	Value
Input Voltage	V_{dc}	360 V
Grid Voltage	V_g	220 V @ 50 Hz
FC Capacitance	C_1, C_2	220 uF
Filter Inductance	L_1, L_2	1.6 mH
Switching Frequency	f_s	10 kHz
Parasitic Capacitance	C_{pv}	50 nF
Power	P	1 kW
Switch	S_1-S_7	IKW40N60
	S_8-S_{11}	IKW40N120

are reduced, it contributes to reduce the total investment cost and volume of passive elements, increase power density. Compared with cascaded H5 topology, the proposed topology has less investment cost in terms of PV panels because the insulation voltage level of PV panels to the ground is doubled when the inverters are cascaded. Compared with common ground topology, the investment cost of passive element is low. This is because the FCs in common ground topology can only be balanced at power frequency, so large capacitance is required, the power density is also reduced. Moreover, the voltage stress of FCs in the proposed topology is 1/4 of that in common ground topology, thus the power density can be further improved. Compared with the well-known H5, HERIC and H6 topologies, the proposed five-level inverter provides better waveform quality.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

In order to verify the effectiveness of the proposed inverter, both the simulations and experimental tests are carried out. The simulations are done with the MATLAB software. The hardware prototype is depicted in Fig. 7. The modulation strategy is implemented in a Texas Instruments TMS320F28335 DSP plus Altera EP2C8Q208 FPGA digital platform. The system parameters are listed in Table IV.

A. Simulation Results

Fig. 8 shows the steady-state and dynamic simulation results of the inverter under grid-connected mode. Fig. 8(a) shows the waveforms of output five-level voltage V_{AB}, grid voltage V_g, grid current i_g, CM voltage V_{CM} and leakage current $i_{leakage}$. It is observed that the RMS value of V_g is 220 V and the RMS value of i_g is 4.55 A. The THD of i_g is about 1.4%. V_{CM} is also

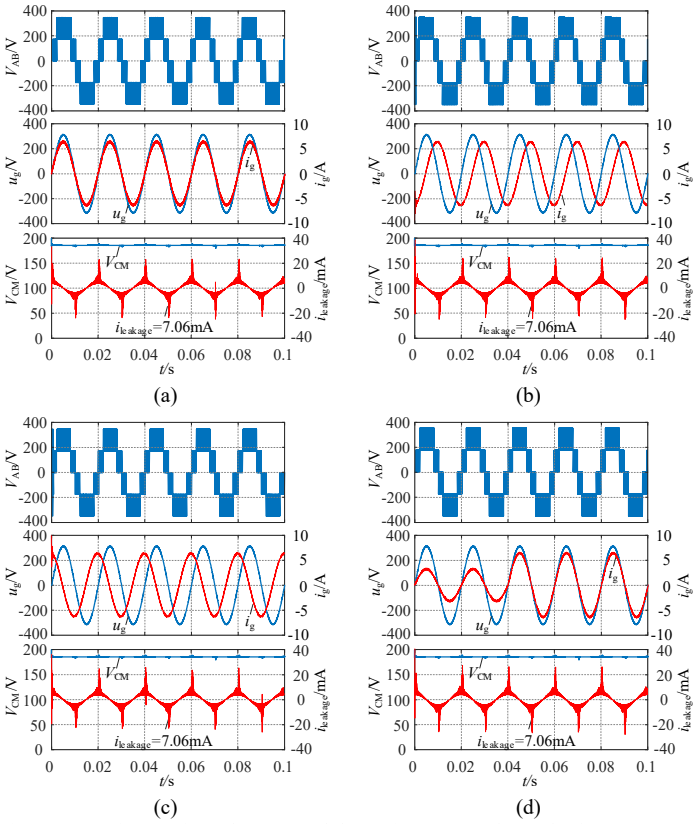

Fig. 8. Waveforms of steady-state and dynamic tests. (a) θ=0°. (b) θ=-90°. (c) θ=90°. (d) Dynamic tests.

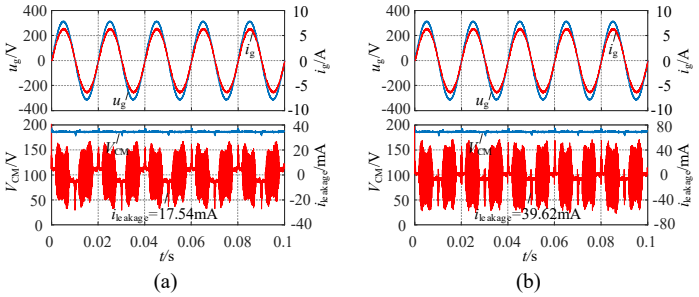

Fig. 9. Simulation waveforms under asymmetry filter inductance conditions. (a) L_1=1.6 mH and L_2=1.44 mH. (a) L_1=1.6 mH and L_2=1.28 mH.

maintained at 180 V with little fluctuation and the RMS value of leakage current is about 7.06 mA. Figs. 8(b) and (c) show the simulation waveforms under lagging power factor (θ=−90°) and leading power factor (θ=90°), respectively. The THDs of the output currents all below 2%, and the leakage currents are still about 7.06 mA. In order to test the dynamic performance of the inverter, the dynamic tests are carried out as shown in Fig. 8(d). The output power changes from 500 W to 1000 W at 0.04 s. The smooth transition process of the output current can be observed, and the leakage current is not affected.

Fig. 9 shows the simulation waveforms of the inverter under asymmetry filter inductance. When the filter inductance has 10% error, the leakage current waveform is shown in Fig. 9(a). The RMS value of leakage current is about 17.54 mA, which is twice of that under symmetrical filter inductance. Fig. 9(b) shows the waveforms of leakage current when the filter inductance has 20% error. It is observed that the RMS value of leakage current is about 39.62 mA. As the error in filter inductance increases, the leakage current increases as well.

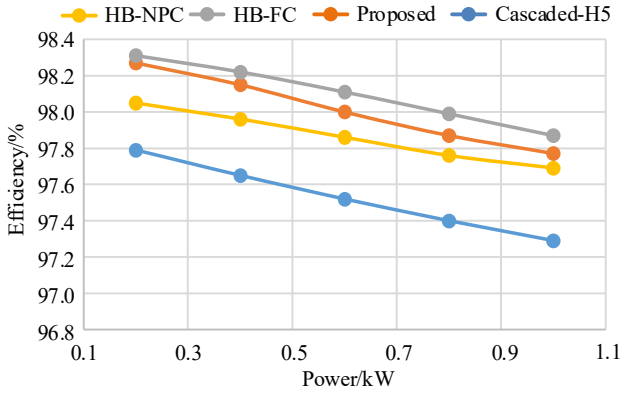

Fig. 10. Efficiency curve with power.

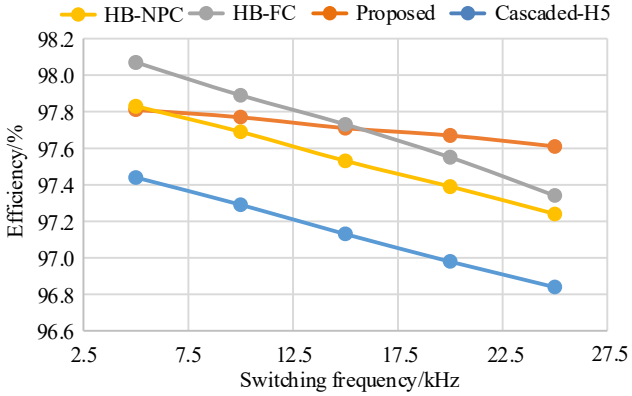

Fig. 11. Efficiency curve with switching frequency.

However, the leakage current is still meet the requirement of the VDE 0126-1-1 standard.

Figs. 10 and 11 show the efficiency curve with power and switching frequency for different five-level topologies based on the PLECS software. These topologies include HB-NPC, HB-FC, cascaded-H5 and the proposed inverter. It can be observed that the efficiency of the proposed topology is lower than HB-FC topology but higher than other topologies within the full power range when the switching frequency is 10 kHz. As shown in Fig. 11, when the switching frequency is low, the efficiency is lower than HB-FC topology, but higher than other topologies. As the switching frequency increases, the efficiency of the proposed inverter is highest among four topologies. This is because the low voltage stress devices contribute to low switching losses.

B. Experimental Tests

Fig. 12 provides the DM performance of the proposed inverter under unite power factor. From top to bottom are the bridge voltage V_{AB}, output voltage V_{out} and output current i_{out}. As can be seen, the RMS value of V_{out} is 220 V, and the i_{out} is about 4.6 A. The THD of i_{out} is only 1.45%. Fig. 13 shows the bridge voltage V_{AB} and FCs voltages V_{C1} and V_{C2}. Obviously, the FCs voltages are well stabilized at 90 V with little ripples. In actually applications, the volume and investment cost will be greatly decreased due to the low voltage stress.

Fig. 14 shows the CM characteristics of the proposed inverter. From top to bottom are bridge voltage V_{AN}, CM voltage V_{CM}, bridge voltage V_{BN} and the leakage current $i_{leakage}$. The two

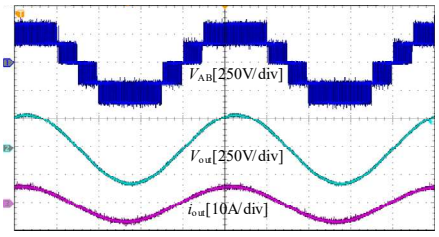

Fig. 12. Waveforms of output voltage V_{AB}, V_{out} and current i_{out}.

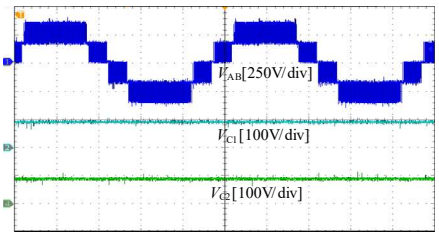

Fig. 13. Waveforms of output voltage V_{AB} and FC voltages V_{C1}, V_{C2}.

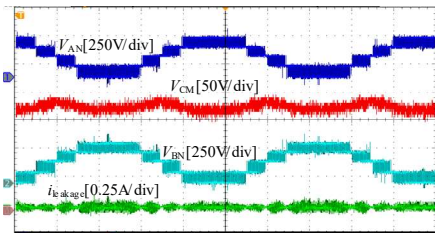

Fig. 14. Waveforms of V_{AN}, V_{BN}, V_{CM} and $i_{leakage}$.

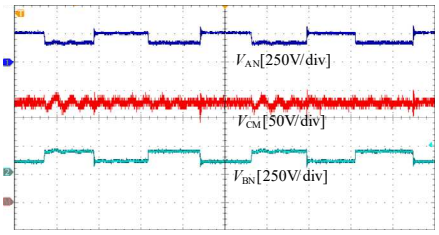

Fig. 15. Waveforms of V_{AN}, V_{BN} and V_{CM} in the positive half cycle.

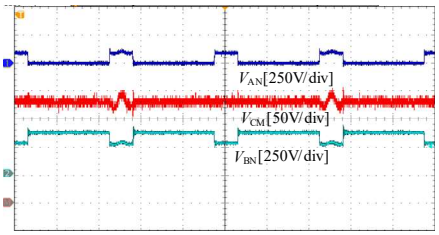

Fig. 16. Waveforms of V_{AN}, V_{BN} and V_{CM} in the negative half cycle.

bridge voltages have five voltage steps, namely, 0, 90, 180, 270, and 360 V. Moreover, V_{CM} is almost constant within the entire period of the utility grid with little power frequency fluctuation. The detail waveform for V_{AN}, V_{BN}, and V_{CM} are shown in Figs. 15 and 16. In the positive half line period, as shown in Fig. 15, V_{BN} is 90 V when V_{AN} is 270 V; V_{BN} is 180 V when V_{AN} is 180 V. As a result, the voltage of V_{CM} is always maintained at 180 V. Similarly, in the negative half line period, as shown in Figs. 16, the voltage of V_{CM} is also kept at 180 V. Evidently, the experimental results agree closely with the results from theoretical analysis. The RMS value of leakage current is only about 27 mA, which complies with the VDE0126-1-1 standard.

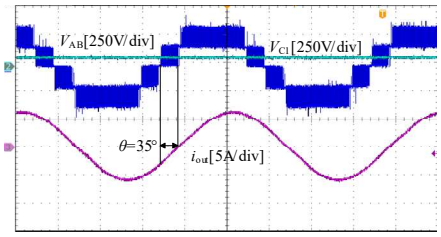

Fig. 17. Waveforms of V_{AB}, V_{C1} and i_{out} when θ is 35 degrees.

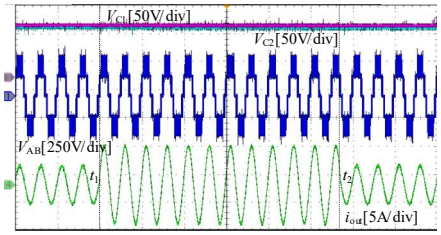

Fig. 18. Transient experiment in load.

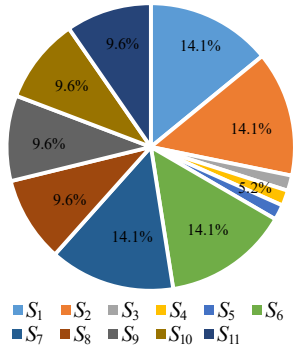

Fig. 19. Losses ratio of each switch.

Fig. 17 shows the experimental results when θ is 35 degrees. From top to bottom are V_{AB}, V_{C1} and i_{out}. It can be seen that the FC voltages are well balanced at 90 V with little fluctuation. At the same time, the excellent DM performance is obtained. The measured THD of the output current is only about 1.62%.

Transient response of the experimental prototype was also conducted as shown in Fig. 18. At t_1, the output power changes from 500 W to 1000 W. And at t_2, the output power changes from 1000 W to 500 W. It can be seen that the FCs voltages V_{C1}, V_{C2} and the output voltage V_{AB} remains stable. What's more, the current change is also very smooth. Therefore, the proposed topology has good dynamic response performance.

Fig. 19 shows the losses ratio of each switch, the results come from the simulation by PLECS. It can be seen that the losses mainly concentrated in S_1, S_2, S_6, S_7 and S_8-S_{11}. The total losses of the last three switches S_3-S_5 accounts for only 5.2%. The simulation results correspond to the modulation strategy described in Section III. The efficiency curve measured in the experiment is shown in Fig. 20. As we can see, the efficiency is increase with the increasement of output power. And the measured maximum efficiency is about 96.02% when the power is about 820 W.

VI. Conclusions

In this paper, a single-phase five-level transformer-less inverter and its modulation strategy for the PV systems are proposed. It adopts the symmetrical filter inductor configuration. The difference from the traditional FC-based topologies is that the FCs voltages are controlled at $V_{dc}/4$. Through the combination of dc-bus voltage and FCs voltages, the CM voltage is theoretically maintained at a constant value during the whole power frequency of unite grid, and then the leakage current is reduced. The two FCs voltages can be balanced at $V_{dc}/4$ automatically at the switching frequency through the selection of the redundant switching states. Finally, the volume and investment cost of the FCs are decreased. The theoretical analysis and experimental verifications are presented. In conclusion, the proposed topology and modulation strategy can ensure a constant CM voltage without any high-frequency components throughout the power frequency cycle. Consequently, the leakage current can be significantly reduced below 300 mA, which meets the specification in the standard VDE-0126-1-1.

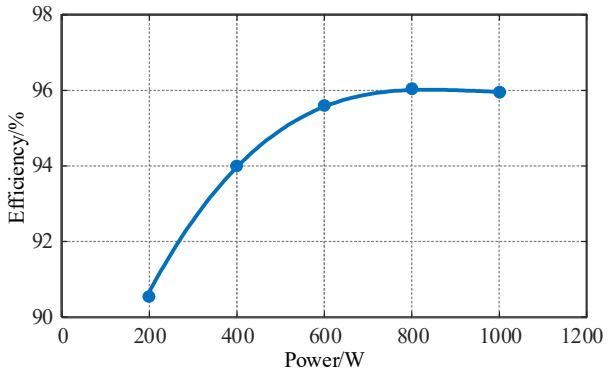

Fig. 20. Measured efficiency.

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