Arm Voltage Balancing Control of Modular Multilevel Resonant Converter

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***Abstract*—Modular multilevel resonant converter is an promising candidate for high voltage applications since it has advantageous features, such as high efficiency, high voltage capability and easy fault-tolerant operation. However, the inequality of arm inductance in practice will lead to imbalance between the upper and lower arm voltages, which will induce large ripples in the circulating current and a dc bias on the voltage generated by modular circuits. To compensate for the voltage imbalance, effects of arm duty cycle changes on arm voltages are discussed. An arm voltage balancing control method is proposed: adjust arm duty cycle according to arm voltage deviation in every switching cycle. Simulation and experimental results are presented to validate the theoretical analysis and the proposed control method.**

***Index Terms*— modular multilevel resonant (MMR) converter, arm voltage balancing, duty cycle.**

I. Introduction

DC Transformers (DCTs) have gained lot of attention with the rapid development of DC distribution systems. They are crucial components in dc grids to interconnect different voltage levels and achieve the necessary isolation. Therefore, high power converters with high voltage capability, high efficiency and smaller volume and weight are desired for DC transformers [1] [2].

At the present time, the voltage and power ratings of commercial semiconductor devices are far below the requirements of high voltage applications. So converters are supposed to be designed carefully to meet the demand. Various efforts have been made to provide DC transformer topologies. With advantages such as modularity, high reliability and high power rating, the modular multilevel converter (MMC) is one of the widely employed high-voltage techniques [3]-[5]. Combining MMC with the dual active bridge (DAB) converter is a solution to construct an isolated DC transformer [6]. To reduce the transformer size, quasi-two-level modulation can be implemented for the converter, where the fundamental ac frequency is the same as the switching frequency [7]. The converter operates similar to the traditional DAB, hence zero voltage switching (ZVS) of power devices cannot be achieved in the whole operation region, which means considerable switching loss [8]. In addition, the reactive current in the converter is high which increases the conduction loss of power devices. To avoid the drawbacks, LLC resonant converter can be used. Based on this idea, a modular multilevel resonant (MMR) dc-dc converter with wide voltage regulation range was proposed in [9].

As shown in Fig. 1, the primary-side single power transistor in LLC resonant converter is replaced by modular structure and the square voltage generated by the modular circuits is applied to a resonant circuit. The switching frequency of submodule power transistors is equal to the fundamental ac frequency which is similar to conventional LLC converter, hence the power transistors can achieve ZVS-on. Besides, compared with conventional resonant converters, the MMR converter can operate in a wide input voltage range by inserting certain number of submodules according to the input voltage level. To limit the circulating current in the modular circuits, two inductors (L_1 and L_2) are inserted into the arms and they also operate as the resonant inductor. However, in practice, the arm inductance deviation is inevitable, which will lead to imbalance between the upper and lower arm voltages. As a result, the generated square voltage is not symmetrical which will induce negative effects on the converter. Therefore, arm voltage balancing is a significant issue for the MMR converter.

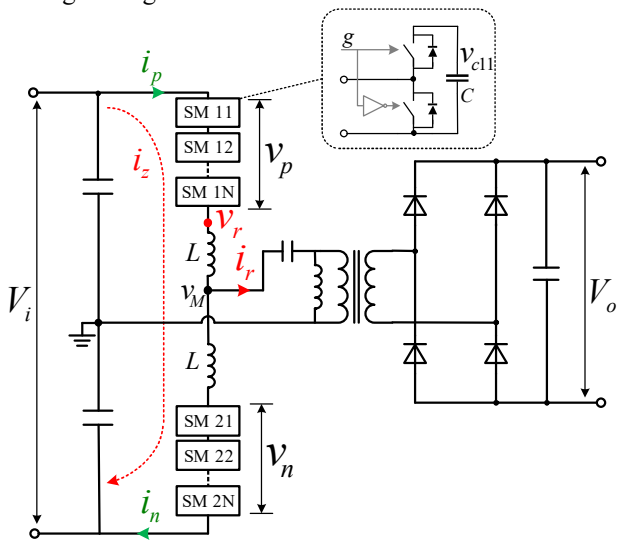

Fig. 1. Topology of MMR dc-dc converter.

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Various arm voltage-balancing strategies have been proposed to compensate for the arm voltage imbalance in MMCs. In [10], the operation of MMCs is studied under asymmetry of the upper and lower arm impedance. Then a controller based on the instantaneous power theory and proportional-resonant scheme is designed. In [11], decoupled control model of MMC under asymmetric parameter conditions is established, and an optimized control method of arm capacitor voltage balancing is proposed. Similar control strategies for arm voltage balancing are also presented in [12]-[14]. However, these control strategies are not suitable for a MMR converter because it operates at medium-frequency which makes the accurate sampling of arm currents difficult. To avoid current sampling, an arm voltage balancing control method based on inter-arm phase-shift modulation scheme is presented in [15], which needs to combine the scheme with inter-submodule phase-shift modulation scheme and increases the complexity of control system.

To achieve arm voltage balancing in MMR converter, the generating mechanism and effects of arm voltage imbalance are studied in this paper. Meanwhile, the effects of arm duty cycle changes on arm voltage are discussed. On this basis, a control method to balance arm voltages in MMR converter is proposed: adjust arm duty cycle according to the arm voltage deviation in every switching cycle. Simulation and experimental results demonstrate the capability of the proposed method in arm voltage balancing.

II. Mechanism and Effects of the Arm Voltage Imbalance

Similar to MMC, the arm current in MMR is composed of a dc component and an ac component. Hence, the arm currents i_p and i_n can be expressed as:

$$\begin{cases} i_p = i_z + \frac{1}{2} i_r \\ i_n = i_z - \frac{1}{2} i_r \end{cases} \tag{1}$$

where i_z is the circulating current, i_r is the resonant current.

Ignoring the small phase-shift between submodules, the theoretical waveforms of arm voltages (v_p and v_n) and currents (i_p and i_n) are shown in Fig. 2. Assume $i_r = I_r \sin(\omega t - \theta)$, then the equivalent current flowing through the submodule capacitors during a switching cycle can be obtained as:

$$\begin{aligned} i_{eq} &= \frac{1}{T_s}\int_0^{T_s/2}(i_z - \frac{1}{2} i_r)dt = \frac{1}{T_s}\int_{T_s/2}^{T_s}(i_z + \frac{1}{2} i_r)dt \\ &= \frac{I_z}{2} - \frac{I_r \cos\theta}{2\pi} \end{aligned} \tag{2}$$

where θ is phase shift between the arm output voltage v_r and the resonant current i_r, T_s is the switching period; I_z is the amplitude of i_z. Considering $\Delta Q = C\Delta V = i\Delta t$, the sign of i_{eq} determines the charge/discharge of submodule capacitors. Hence, (2) reveals that, in every switching cycle, the circulating current i_z charges the submodule capacitors, whereas the ac current discharges them since θ is much smaller than 90 degree.

In steady state, i_{eq} must be equal to 0, otherwise the capacitor voltage will keep increasing or decreasing, therefore

$$I_z = \frac{I_r \cos\theta}{\pi} \tag{3}$$

The arm voltages v_p and v_n can also be considered as composed of a dc component ($V_p/2$, $V_n/2$) and an ac component (v_{pa}, v_{na}). The equivalent circuits of dc current path and ac current path are illustrated in Fig. 3. The ac voltage and current directions have been redefined in Fig. 3 (b) for convenience. According to Kirchhoff's voltage and current law, the following equations can be obtained:

$$\begin{cases} i_{pa}(t) + i_{na}(t) = i_r(t) \\ v_{pa}(t) = v_M(t) + L_1 \dfrac{di_{pa}(t)}{dt} \\ v_{na}(t) = v_M(t) + L_2 \dfrac{di_{na}(t)}{dt} \end{cases} \tag{4}$$

where i_{pa} and i_{na} are the ac components of i_p and i_n respectively, L_1 and L_2 is the arm inductance.

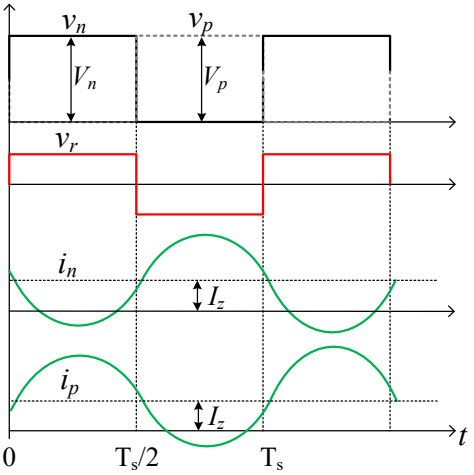

Fig. 2. Theoretical waveforms of voltages and currents in MMR.

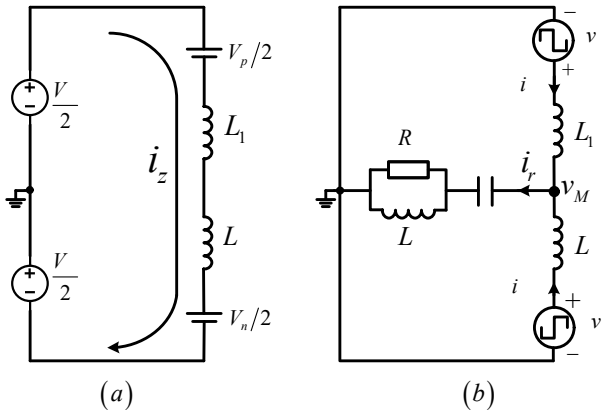

Fig. 3. Equivalent circuits of (a) dc current path and (b) ac current path

According to (4), when the arm voltages are balanced ($v_{pa} = v_{na}$), if L_1=L_2, we will have $i_{pa} = i_{na} = 0.5 i_r$ which is consistent with (1). However, the component variation is inevitable in practice. Take $L_1 < L_2$ for example, assume the upper and lower arm voltages are initially balanced ($v_{pa} = v_{na}$),

then i_{pa} will be larger than i_{na} according to (4) while the dc current i_z in the upper and lower arms is equal. As a result, the capacitors in the upper arm are discharged more than the capacitors in the lower arm, as (2) reveals. Hence, the upper arm voltage v_p will be lower than the lower arm voltage v_n during the next switching cycle. Referring back to (4), as v_p decreases, i_{pa} will become smaller. Similarly, i_{na} will become larger as v_n increases. Therefore, this is a negative feedback process, which ends when i_{pa} and i_{na} become equal again. Therefore, the converter will enter into another steady state with a constant deviation between the upper and lower arm voltages.

In Fig. 1, according to the Kirchhoff's voltage law, the voltage across the arm inductors can be obtained as

$$u_L = V_i - v_p - v_n \tag{5}$$

where V_i is the input voltage. In the steady state, when the lower arm is inserted, u_L is equal to $V_i - V_n$. When the upper arm is inserted, u_L is equal to $V_i - V_p$. If the arm voltages are balanced, $V_p = V_n$, then u_L will be 0 in every switching cycle. Otherwise, a square-wave voltage (u_L) will be applied across the arm inductors, which will induce large ripples in circulating current i_z and may saturate the arm inductors.

Similarly, the voltage generated by the modular circuit (v_r) is written as

$$\begin{cases} v_r = V_n - \dfrac{V_i}{2}, & 0 \sim \dfrac{T_s}{2} \\ v_r = \dfrac{V_i}{2} - V_p, & \dfrac{T_s}{2} \sim T_s \end{cases} \tag{6}$$

which reveals that the imbalance of arm voltages will lead to a dc bias on the arm output voltage v_r and increases voltage stress of the resonant capacitor.

III. Arm Voltage Balancing Control Method

In order to compensate voltage imbalance caused by the inequality of arm inductance, a control method is proposed in this section. The basic idea is to adjust the arm duty cycle according to the arm voltage deviation.

Add a small disturbance to the duty cycle of the upper arm (Δd), according to (2), the equivalent current flowing through the submodule capacitors in upper arm during a switching cycle is calculated as:

$$\begin{aligned} I_{eq} + \Delta i_{eq} &= \frac{1}{T_S}\int_{(\frac{1}{2}-\Delta d)T_S}^{T_S} (I_z + \frac{1}{2} I_r \sin(\omega t - \theta))dt \\ &= (\frac{1}{2} + \Delta d) I_z - \frac{I_r}{4\pi}\left[\cos\theta + \cos(2\pi \cdot \Delta d + \theta)\right] \end{aligned} \tag{7}$$

Substitute (3) into (7), then the variation of i_{eq} caused by duty cycle change Δd can be derived as:

$$\begin{aligned} \Delta i_{eq} &= \Delta d \cdot I_z - \frac{I_r}{4\pi}\left[\cos(2\pi \cdot \Delta d + \theta) - \cos\theta\right] \\ &= I_z(\Delta d + \frac{1}{4} - \frac{1}{4}\cos(2\pi \cdot \Delta d)) + \frac{I_r}{4\pi}\sin(2\pi \cdot \Delta d)\sin\theta \end{aligned} \tag{8}$$

Considering Δd and θ are very small, Δi_{eq} can be simplified as:

$$\Delta i_{eq} \approx I_z \Delta d \tag{9}$$

which reveals that the equivalent current flowing through the submodule capacitors will increase as the arm duty cycle increases. In other words, the arm voltages can be balanced by adjusting the arm duty cycle: increase the duty cycle of the arm with lower voltage (decrease the duty cycle of the arm with higher voltage).

Fig. 4 shows the block diagram of the proposed arm voltage balancing method. Considering a MMR converter with N submodules in each arm, v_{c11}~v_{c1N} and v_{c21}~v_{c2N} are the sampling voltages of submodule capacitors in the upper and lower arms, respectively. The upper and lower arm voltages are obtained as the sum of their submodule capacitor voltages. Then the difference between the arm voltages is calculated: $\Delta v_{arm} = V_p - V_n$. Δv_{arm} is the input of a PI controller whose output is the duty cycle variation Δd and is limited by a saturation. Finally, the duty cycle d of the upper arm for the next switching cycle (while the duty cycle of the lower arm is $1 - d$) is calculated by 0.5 minus Δd and sent to the gate signal generation unit.

The proposed arm voltage balancing method does not rely on accurate current sampling, and the voltage sampling of submodule capacitors is also necessary for inter-submodule voltage balancing [17]. In addition, the control algorithm is not complicated to implement. Hence, the proposed method will not increase the complexity of control system and is also suitable for other converters with MMC structure.

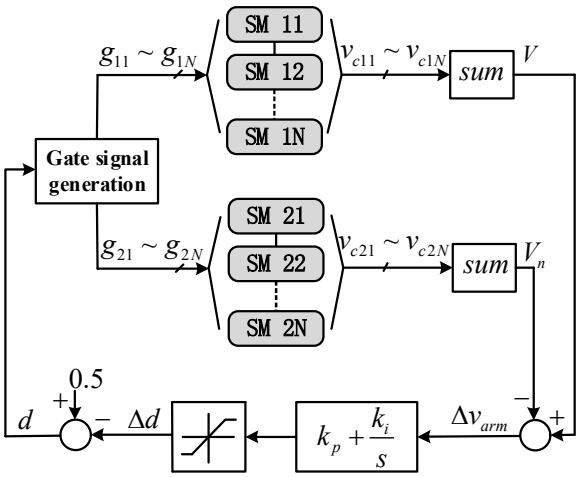

Fig. 4. Control block diagram of the proposed voltage balancing method.

IV. Simulation Results

To verify the above theoretical analysis and the proposed method, simulations with parameters listed in Table I, are conducted in PLECS. The lower arm inductance is 4% larger than the upper arm inductance. Fig. 5 shows simulation results without the proposed arm voltage balancing method. Voltage of the upper arm v_p is lower than that of the lower arm v_n obviously, which is consistent with the analysis in Section II. In addition, the voltage across arm inductors is a square-wave voltage and induces large ripples in the circulating current. With the proposed method, as shown in Fig. 6, the upper and lower arm voltages are well balanced, and the dc bias in arm

TABLE I
PARAMETERS OF PROTOTYPE FOR SIMULATION

Input voltage	V_i	3000V
Number of devices each arm	N	6
AM capacitance	C	$20\mu F$
Upper arm inductor	L_1	$240\mu H$
Lower arm inductor	L_2	$250\mu H$
Resonant capacitor	C_r	$1.6\mu F$
Magnetizing inductance	L_m	$5mH$
Switching frequency	f_s	$10kHz$

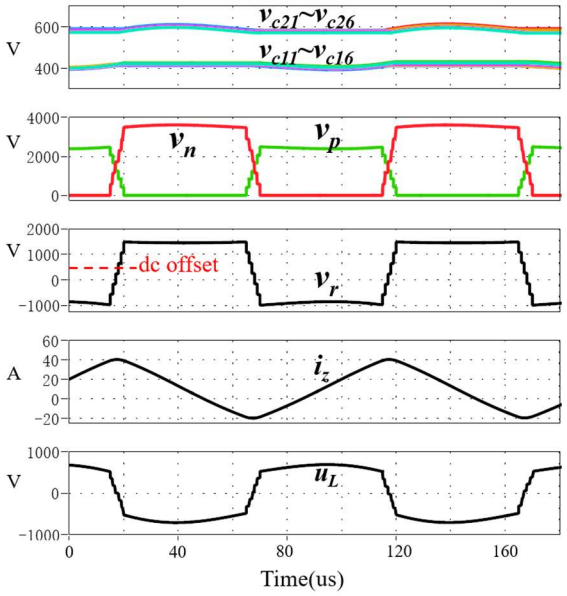

Fig. 5. Simulation results without arm voltage balancing method when 4% difference in arm inductance is considered.

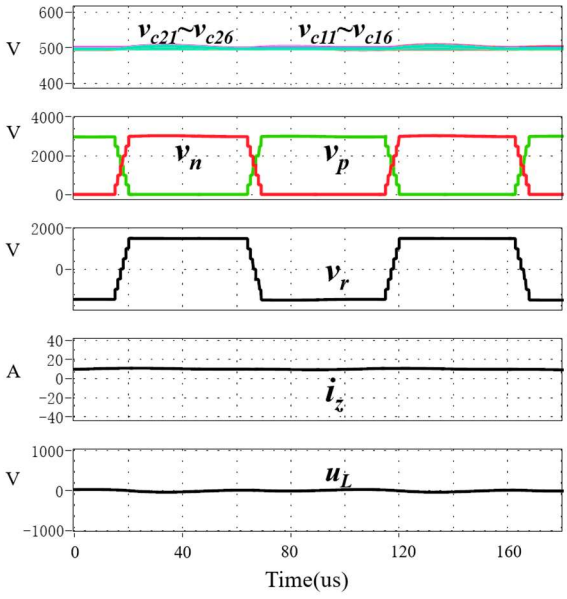

Fig. 6. Simulation results with the proposed balancing method when 4% difference in arm inductance is considered.

output voltage v_r and the large ripples in the circulating current i_z are both eliminated.

V. Experimental Results

To validate the presented analysis and simulations, downscaled experiments are conducted on a MMR prototype with parameters listed in Table II. Photographs of the prototype hardware is shown in Fig. 7. The proposed control method is implemented by a hierarchical control system in the prototype, similar to the inter-submodule voltage balancing method in [17]. The core controller is implemented with FPGA where the sampling voltages are processed and gate signals are generated. Experimental results without and with the proposed arm voltage balancing method are shown in Fig. 8 and Fig. 9, respectively. v_{c11} and v_{c21} are the submodule capacitor voltages from the upper and lower arms. As illustrate in Fig. 8, parameter even though the nominal value of two inductors are both 240uH. The variations are inevitable which results in the obvious deviation of arm voltages without the proposed method. The results in Fig. 9 demonstrate that the arm voltages are well balanced when the proposed method is implemented.

TABLE II
PARAMETERS OF PROTOTYPE FOR EXPERIMENTS

Input voltage	V_i	250V
Number of devices each arm	N	6
AM capacitance	C	$20\mu F$
Upper arm inductor	L_1	$240\mu H$
Lower arm inductor	L_2	$240\mu H$
Resonant capacitor	C_r	$1.6\mu F$
Magnetizing inductance	L_m	$5mH$
Switching frequency	f_s	$10kHz$
Transformer ratio	n	2:1

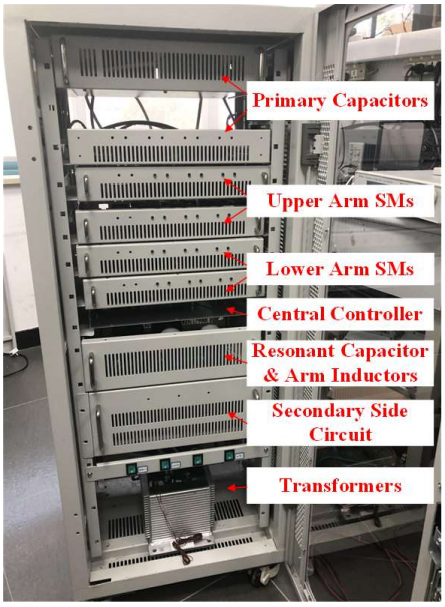

Fig. 7. Photographs of the prototype hardware.

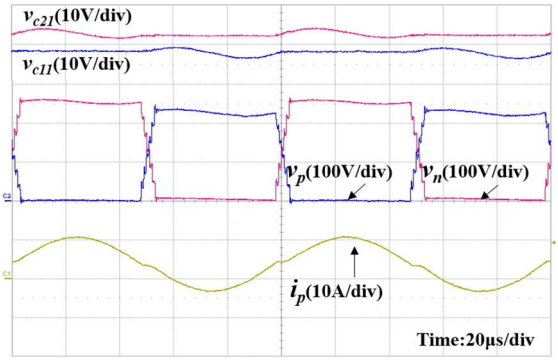

Fig. 8. Experimental results without arm voltage balancing method.

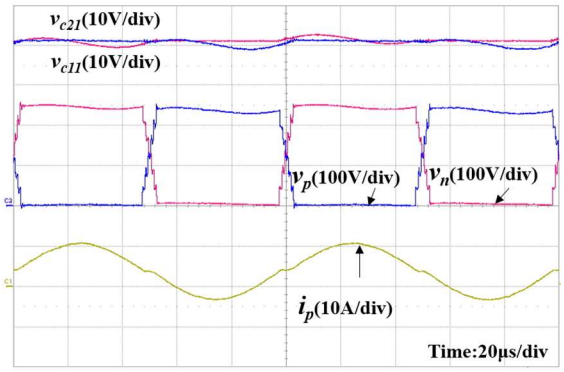

Fig. 9. Experimental results with arm voltage balancing method.

VI. Conclusion

This paper analyzes the mechanism of arm voltage imbalance caused by inequality of arm inductance in MMR converter. Then an arm voltage balancing method by adjusting the arm duty cycle is proposed. Simulation and experimental results demonstrate that, with the proposed method, arm voltages are well balanced. The ripples of the circulating current and the dc bias in resonant voltage caused by the arm voltage imbalance are suppressed. The proposed method does not rely on arm current sampling and can be combined with the inter-submodule voltage balancing method, which is easy to be implemented.

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