Common Mode EMI Reduction through PWM Methods for Three-Phase Motor Controller

Dong Jiang, *Senior Member*, *IEEE*, Jianan Chen, *Student Member*, *IEEE*,
and Zewei Shen, *Student Member*, *IEEE*
(Invited)

***Abstract*—Pulse-width sequences are identified as the determining factor for common-mode (CM) voltage, which together with CM path generate CM current. This paper introduces a series of pulse-width modulation (PWM) methods, which are focusing on reducing CM noise of three-phase inverters as motor controller. Firstly, theoretic analysis and PWM reduction methods of CM voltage for general three-phase two-level inverters are introduced. Analysis results indicate that the realization of CM noise reduction should take switching frequency and loop impedance into consideration together to avoid CM resonant phenomenon. The regular three-phase two-level inverter is incapable of eliminating CM voltage because of the limitation of topology. Then, optimal PWM methods applied to for advanced topologies can be utilized to eliminate the CM voltage theoretically. Two typical typologies presented in this paper are three-level inverters and paralleled inverters. Three-level inverters can achieve zero-CM output voltage by selecting zero-CM voltage vectors at the expense of power quality. However, for paralleled inverters, zero-CM PWM method is able to achieve zero CM voltage output, as well as the improved output current harmonics and voltage balancing.**

***Index Terms*—Common-mode voltage, conducted EMI, PWM methods, paralleled inverters.**

I. Introduction

THE concept of "common-mode (CM)" is associated with the concept of "differential-mode (DM)" that means the electrical parameters conduct in the opposite direction in transmission lines. Therefore, common-mode voltage and current mean the electrical parameters exist in the same conducted direction. In electromagnetic interference (EMI) analysis, CM conducted EMI, which is usually represented as high frequency CM current, means the EMI noise conduct in the same direction in all transmission lines.

In ideal linear circuit, CM noise problem does not exist due to the balanced voltage in each phase will generate zero voltage in the common conducted direction. For example, in three-phase balanced circuit, the sum of three-phase AC voltage defined as CM voltage keeps to be zero all the time. In addition, there is no parasitic path in the ideal circuit for CM current to conduct through. On that account, the CM noise problem is caused by non-ideal factors including CM noise source (high frequency CM voltage) and CM conducted loop (parasitic capacitance and grounding) in the practical physical system.

Because of the applications of power electronics inverters, high frequency CM voltage appears in the system and causes the CM EMI problem. Power electronics converters usually generate rectangle pulse-width voltage sequences through pulse-width modulation (PWM) that determines the general waveform of CM voltage, but the instantaneous dv/dt of CM voltage is affected by switching transient. Therefore, the CM noise source is related to both PWM methods and switching transient. These two factors determine different frequency range of EMI spectrum: PWM methods determine the harmonics of switching frequency varying from 150kHz to several MHz, whereas switching transient represented as high dv/dt and di/dt mainly contributes to the high frequency components between several MHz to 30MHz. The two ranges have no exact boundary for their interaction, and they also relate to other factors such as switching frequency.

Besides, the factor of parasitic path further adds the complexity of CM noise in practical physical system. There are two kinds of CM loops for motor system according to power supply. The AC-fed motor drive system is normally consisting of front-end rectifier and inverter, so the CM loop is related to two kinds of converters together [1], [2]. For the sake of simplicity, this paper only selects DC-fed motor drive system as the research objective because its mechanism of CM is relatively simple and sufficient to characterize the CM problem. Fig. 1 shows the DM and CM EMI for motor drive system with DC supply. DC neutral point O is connected to the ground directly, forming the CM loop together with the load neutral N through the parasitic capacitor C_s. The output CM voltage is expressed by (1), so the CM voltage could be acquired by measuring the output voltage of each phase and calculating their mean value.

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Dong Jiang, is with State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, CO 430074 China. (e-mail: jiangd@hust.edu.cn).
Jianan Chen, is with State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, CO 430074 China. (e-mail: chen_jianan@hust.edu.cn).
Zewei Shen, is with State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, CO 430074 China. (e-mail: shenzw@hust.edu.cn).
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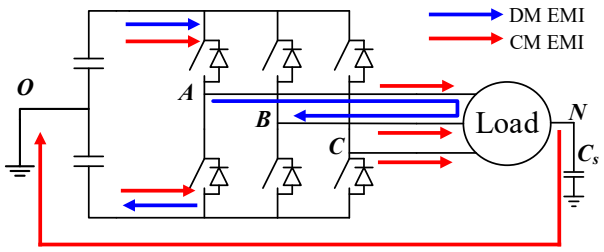

Fig. 1. Conducted DM and CM EMI for motor drive system with DC-fed.

$$V_{cm} = \frac{1}{3}\left(V_{AO} + V_{BO} + V_{CO}\right) \tag{1}$$

Fig. 1 just exhibits the external CM loop of motor drive system whereas the real conducted loop inside the motor is rather complicated [3]−[5]. Fig. 2 shows possible CM current conducted paths caused by high frequency CM voltage and parasitic capacitors inside the motor. Take the main parasitic capacitance C_{s1} in Fig. 2 for example, C_{s1} is the parasitic capacitor caused by the area between the stator winding and stator iron in the electrical machine, making the CM path connect to the ground through machine frame. CM capacitance is usually with nF level for kW to MW level motor, which can block most of the low frequency CM components. Unfortunately, high frequency switching of the inverter generates plenty of high frequency components in the CM voltage, which can conduct through the parasitic capacitors. With the application of novel wide-band-gap (WBG) power electronics devices, the switching speed and switching frequency are further increasing, making the CM current even bigger and becomes a serious problem [6], [7].

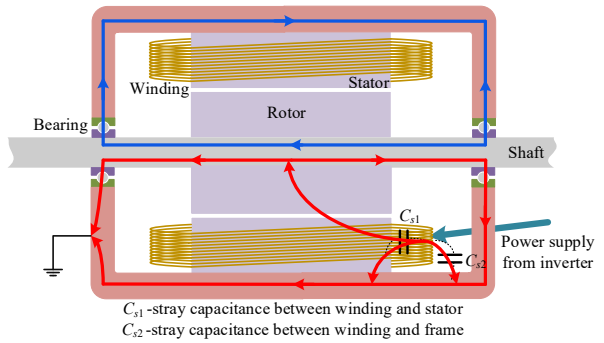

Fig. 2. Illustration of mechanism for CM current in motor.

All CM current eventually flow into ground no matter which path they prefer, so Fig. 1 could perfectly represent the external CM loop of motor drive system. The output voltage of inverters is modeled as pulse sequences V_{AO}, V_{BO}, V_{CO}, the equivalent circuit of motor drive system is Fig. 3, which also contains stator resistor R_s, stator inductor L_s, CM inductor L_{cm} and parasitic capacitor C_s. Fig. 4 is the CM loop equivalent circuit. It is clear that the CM loop includes noise source CM voltage and impedance *R-L-C* that mean a resonant frequency determined by CM inductor and parasitic capacitance will appear. Therefore, the CM conducted EMI represented as CM current is not only associated with CM voltage but also with CM impedance [8].

CM noise can bring serious problems for the power conversion system. Firstly, based on DM EMI, conducted CM

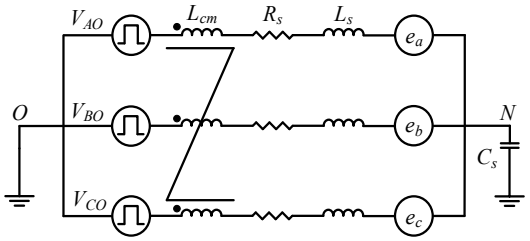

Fig. 3. Equivalent circuit of motor drive system.

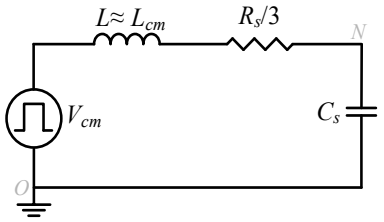

Fig. 4. Equivalent circuit of CM loop.

EMI could also conduct in power line, making the EMI problem even more complicated. DM EMI noise inherently exists in phase current even without CM loop inducing CM current. When parasitic capacitance conducting CM current, the current flowing through phase leg includes DM current and CM current, which make the EMI noise in transmission line rather complicated. What is more, CM problem could also bring bearing damage. As shown in Fig. 2, high frequency CM current may conduct through shaft, resulting in unbalanced flux encircling shaft. The time-varying flux induces voltage in shaft called shaft voltage. Shaft voltage is also characterized with high *dv*/*dt*, when it exceeds the breakdown voltage of the lubrication film of bearing, large discharge current will pass through the bearing and bring damage [3]−[5]. The closed loop of circulating bearing current is the blue line in Fig. 2. Bearing current can bring damage to the bearing and impair the reliability of motor drive system, too. Fig. 5 shows the damage of bearing ring caused by CM current in practical applications. All these problems make the CM current reduction to be an urgent requirement. According to previous analysis, reducing CM voltage and blocking conducted paths are the two effective solutions to suppress CM noise.

Fig. 5. Bearing ring damage caused by CM current.

The major approach to reduce CM current in power conversion system is through CM filter, with CM choke as the main part. The function of CM filter is adding CM loop impedance to reduce the CM current and CM noise [9], [10]. CM choke is based on a CM inductor with big CM inductance. Its size and weight are determined by the flux saturation in the core, which is also determined by the CM volt-seconds [11]. In industry application, CM choke is usually with a big portion in

the size and weight of power conversion system, especially for the application with strict EMI requirement. Then, the reduction of CM filter size and weight become an important issue for industry applications. In the design of passive CM filter, power density is always a pursuit and there are many optimization methods with consideration of parasitic and couplings [12]−[16]. Based on passive CM filter, active EMI filter has been developed to further reduce the CM noise and reduce the size and weight of the filter [17], [18]. The idea of active CM filter is compensating the CM noise with controlled power amplifier. Nevertheless, it still needs extra hardware to do the filtering.

The approach of CM filter is essentially a solution through the CM path. Another solution is aiming at the CM noise source: the switching function of power electronics inverters. Since the PWM methods determine the amplitude and frequency characteristics of the CM noise source, CM noise can be reduced at source by modifying PWM method. Then, the requirement for CM filter can be further reduced. This kind of modification is utilizing the freedom of pulse arrangement and aiming at reducing CM noise.

Compared with the main CM reduction approach (CM filter) that has been well studied in recent years, the approach of PWM for CM noise reduction is another attractive solution. PWM methods about CM reduction for widely applied topologies such as general two-level inverters, three-level inverters and paralleled inverters will consist the most significant part of this paper. In addition, some of other advanced typologies also have ability to restrain CM voltage. The modified topology like the three-phase four-leg inverter can be used to reduce CM voltage [19] because of more control freedom for the extra phase-leg, but the modulation scheme for this topology is complex. Besides, filter should be added between the inverter and motor where the parameters of the filter should be tuned. Compared with regular three-level inverter, the H-bridge inverter fed open-end winding AC motor drive has certain advantages–the absence of neutral point fluctuations and the redundancy of space vector combinations. [20], [21] introduced the principle of the bearing current and shaft voltage in open-end winding motor which confirmed that the total CM voltage is the instantaneous average voltage for all phase-legs and the corresponding modulation schemes are proposed to restrain the bearing currents and shaft voltage. In addition, for multi-phase machine with multi-phase inverter, combination of PWM can be applied to reduce and even eliminate CM voltage.

This paper will review a great deal of work about the modified PWM methods of the CM noise reduction of three-phase inverters, especially for motor drive applications. For regular three-phase two-level inverter application, CM voltage cannot be eliminated with PWM methods, but the reduction of CM voltage amplitude can be achieved. Series work of modified PWM on CM noise reduction in three-phase two-level inverters is introduced in part II. For three-level inverter, the pulse combination can achieve zero CM voltage theoretically. Nevertheless, the strategy will bring by-products such as poor power quality and bigger switching loss, which impede the practical applications. Related study of zero-CM PWM for three-level inverter is introduced in part III. Similar like three-level inverter, paralleled two-level inverter can achieve zero CM voltage theoretically, too. Initially, interleaved PWM can reduce the CM voltage for paralleled inverter. Then, a novel zero-CM PWM in paralleled inverter can further eliminate CM voltage. The series work of modified PWM for paralleled inverter is introduced in part IV. In part V, the summary of all PWM methods presented in paper are concluded and the prospect for PWM methods to reduce CM voltage is provided.

II. CM Noise Reduction through PWM for General Two-Level Inverters

Two-level voltage source inverter shown in Fig. 1 is the most typical topology for power conversion including motor drive and grid-connected inverters. Therefore, this part chooses the two-level inverter to analysis its CM voltage with different kinds of normal and modified PWM methods.

PWM methods can be ascribed to two major approaches: space vector PWM (SVPWM) and carrier based PWM (CBPWM). It has been well proved that the two approaches are equivalent in effect [22]. Each space vector PWM method is equivalent to a certain carrier based PWM method, through a certain zero-vector arrangement to achieve that. CBPWM is easier for realization and the CM voltage analysis is firstly introduced by CBPWM.

Fig. 6 shows the gate drive signals of three-phase and the corresponding CM voltage with different PWM methods in single switching cycle. Without losing generality, assuming the duty cycles as $da > db > dc$. The case with SVPWM is shown in Fig 6(a). The CM voltage is with four steps: $-V_{dc}/2$, $-V_{dc}/6$, $V_{dc}/6$, and $V_{dc}/2$. It is obvious that the maximum and minimum CM voltage appear when 111 and 000 voltage vectors are applied. For discontinuous PWM (DPWM), the maximum duty cycle is clamped to 1 (Fig. 6(b)) or the minimum duty cycle is clamped to 0 (Fig. 6(c)). The amplitude of CM voltage is still $V_{dc}/2$, with 111 or 000 voltage vectors. It can be found that the zero voltage vectors (111 and 000) cause the amplitude of CM voltage of $V_{dc}/2$, and non-zero voltage vectors cause the amplitude of CM voltage of $V_{dc}/6$. From this point, it is obvious that the major approach for CM voltage amplitude reduction is to avoid utilization of zero voltage vectors 000 and 111.

In Fig. 6(a), Fig. 6 (b), and Fig. 6 (c), zero voltage vectors appear because of the identical alignment of the three pulses, which results in 000 appearing in the two sides and 111 in the center. If doing 180-degree phase-shift for the phase with mid-length duty cycle (phase-*b* in Fig. 6), the 000 vector in the two sides will be changed to 010 and the 111 vector in the center will be changed to 101, which is shown in Fig. 6(d) for SVPWM. Then the zero voltage vectors can be eliminated in the whole switching cycle and the CM voltage amplitude can be reduced from $V_{dc}/2$ to $V_{dc}/6$. Similar modification can also be done for DPWM, as shown in Fig. 6(e) and Fig. 6(f). CM voltage amplitude can also be reduced from $V_{dc}/2$ to $V_{dc}/6$. The modified CBPWM methods with CM voltage reduction have

their corresponding explanation through space vector method. Fig. 6(d) is equivalent to active zero state PWM (AZSPWM) and Fig. 6(e) and Fig. 6(f) are the same as near state PWM (NSPWM) [23]−[29].

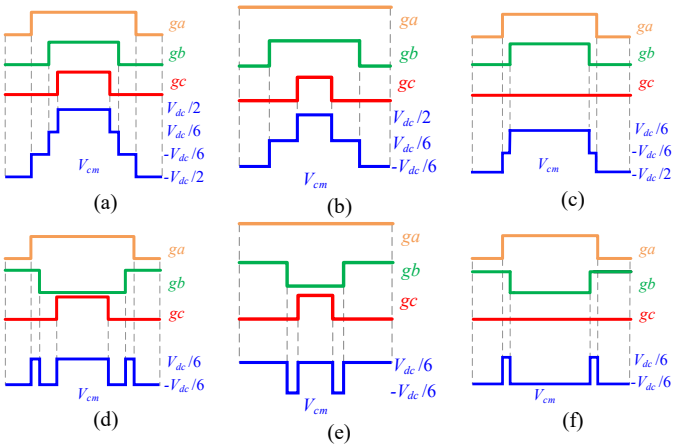

Fig. 6. Output voltage logics and the CM voltage for carrier-based PWM. (a) SVPWM. (b) DPWM (max). (c) DPWM (min). (d) AZSPWM. (e) (f) NSPWM.

Reference [23]−[29] have analyzed this kind of modification through space vector approach on detail. Fig. 7(a) and Fig. 7(b) show the space vector combination of the reference voltage V^* with AZSPWM and NSPWM. With AZSPWM, V^* is still combined by the two adjacent voltage vectors, as V_1 and V_2 in Fig. 7(a). Nevertheless, the rest of the time in the switching cycle is not occupied by zero vectors, but by the two opposite active voltage vectors that can cancel each other for volt-seconds output, as V_3 and V_6 in Fig. 7(b). The combination of the two opposite active voltage vectors is called “active zero vector”. With AZSPWM, no zero vector appears and CM voltage amplitude can be reduced to $V_{dc}/6$. For NSPWM, V^* is combined by three adjacent voltage vectors instead of the two adjacent. The effect is equivalent to Fig. 6(d) voltage vectors, as V_1, V_2 and V_3 shown in Fig. 6(h). By arranging the action time t_1, t_2 and t_3 for the V_1, V_2 and V_3, the volt-seconds can be balanced with V^* in each switching cycle and there is no need for zero voltage vector. CM voltage amplitude can be reduced to $V_{dc}/6$. The effect of space vector modulations mentioned above are equivalent to Fig. 6(e) and Fig. 6(f).

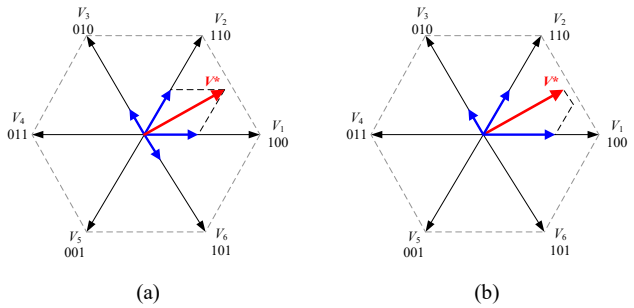

Fig. 7. The corresponding SVPWM realization for modified PWM. (a) AZSPWM (space vector). (b) NSPWM (space vector).

AZSPWM and NSPWM can significantly reduce the CM voltage amplitude in experiments. However, the real problem is not CM voltage, but the CM noise that is with characteristics of CM current. It is not only associated with CM noise source, but also with conducted path impedance. Since the CM loop is highly relying on parasitic and with non-linear characteristics, the reduction of CM voltage amplitude does not mean the reduction of CM current.

Fig. 8 and Fig. 9 show the CM voltage and their spectrum of the experimental results. The amplitude of CM voltage has assuredly reduced with modified PWM applied. AZSPWM and NSPWM can significantly reduce the CM voltage around the switching frequency, but not sure for other frequency areas. In some harmonics of switching frequency, the modified PWM method can be with even bigger component than the conventional SVPWM or DPWM. For example, NSPWM has bigger value near the 3rd order harmonics of switching frequency than DPWM.

The CM loop is mainly with the load motor inductors and the parasitic capacitor to the ground. By identifying the CM loop impedance, it is with an obvious resonant peak, which is by the resonance between the main inductance and capacitance. The CM voltage components near this frequency will be amplified and dominating the CM current. It means that proper PWM design for CM noise reduction should be together with switching frequency and loop parameters, and then the CM current can be reduced.

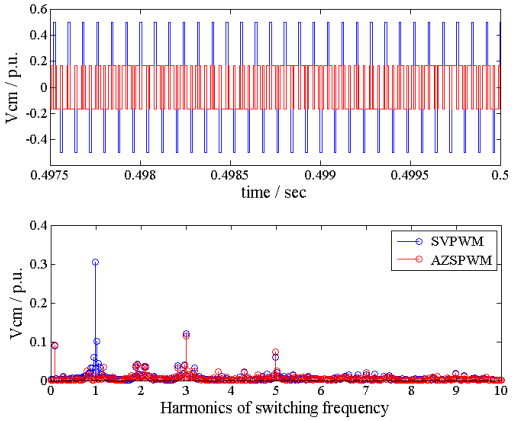

Fig. 8. Experimental results of CM voltage and spectrum comparison. (SVPWM vs. AZSPWM).

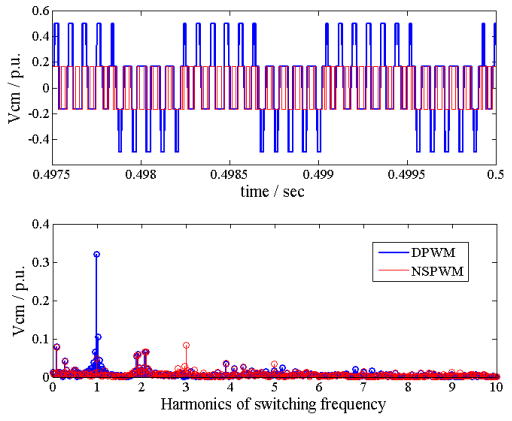

Fig. 9. Experimental results of CM voltage and spectrum comparison. (DPWM vs. NSPWM).

The modification of pulse alignment in AZSPWM and NSPWM also changes the output voltage stress on the load. A

typical result is the output current change. AZSPWM and NSPWM change the output voltage distribution in each switching cycle. Although the output current fundamental value is the same as SVPWM and DPWM, its current ripple is different from DPWM. When designing PWM for the purpose of CM noise reduction, other factors including current ripple should be also taken into consideration.

For DC-fed motor drive, the modified PWM methods including AZSPWM and NSPWM can reduce the CM voltage amplitude by not using zero vector. However, the CM voltage cannot be eliminated by the nature of three-phase two-level inverters, because the three terminal voltages are either positive or negative DC voltage and the phase number is odd, adding them together cannot be zero.

More advanced topologies can provide more pulse combinations and will be able to achieve zero CM voltage output theoretically. One approach is to make the phase voltages with more choices than two-level inverter; the other is to make the phase-leg number to be even for two-level inverter. In the next two parts, PWM with more advanced topologies will be studied for CM noise reduction.

III. CM Noise Reduction for Three-Level Inverters

Three-level inverters have been widely applied for the advantages of better waveform and lower harmonics, as well as feasibility of higher voltage rating and power rating. Major topologies for three-level inverter include neutral-point-clamped (NPC), flying capacitors, cascaded H-bridges and T-type inverters. In the view of output voltage, they are equivalent with each other. NPC inverter is selected as the target for PWM analysis of CM noise reduction in this part, whose topology is shown in Fig. 10. The DC-link is connected with two capacitors, with voltage of $V_{dc}/2$ for each. Each phase-leg voltage is switching between positive DC voltage (p), zero (o) and negative DC voltage (n) with reference to the DC mid-point *O*.

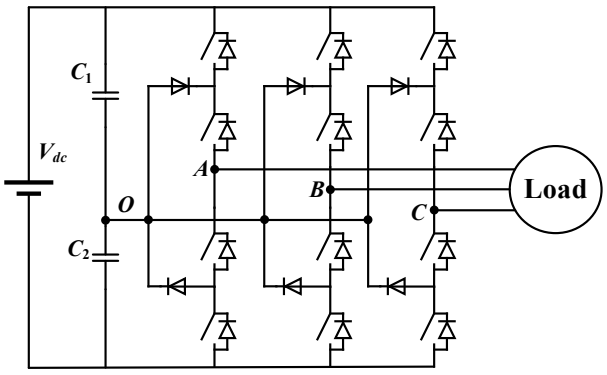

Fig. 10. Topology of three-level NPC inverter.

Fig. 11 shows the voltage space vectors for three-level inverter. There are totally 27 voltage vectors in the plane, including 3 zero vectors, 12 small vectors, 6 medium vectors and 6 large vectors. Among them, the six medium vectors (210, 120, 021, 012, 120, 201) and the zero vector 111 are with zero CM voltage. By only selecting the medium vectors and 111 highlighted by red arrows in Fig. 11 to combine the reference voltage, zero-CM SVPWM can be achieved and CM voltage can be eliminated theoretically [30]−[32].

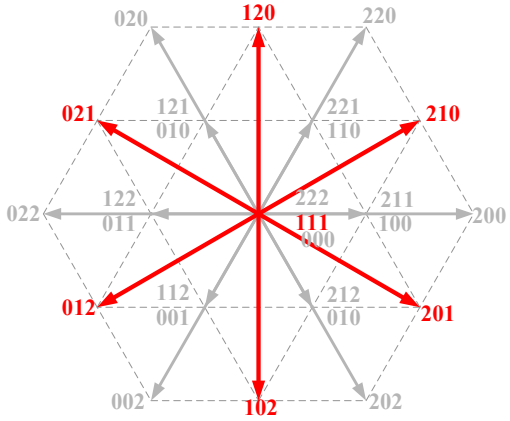

Fig. 11. Voltage space vectors for three-level inverter.

Fig. 12 shows the experimental results of CM voltage comparison between normal SVPWM and zero-CM SVPWM in three-level inverter, with the same experimental parameters. It can be noticed that the zero-CM SVPWM can significantly reduce the CM voltage from normal SVPWM and make it negligible. Nevertheless, common-mode voltage could not be completely reduced to zero for none-ideal effects, including the switching transient and dead-time effect [33].

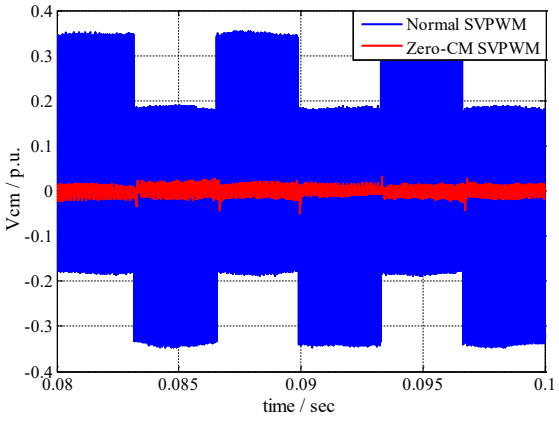

Fig. 12. CM voltage comparison between SVPWM and zero-CM SVPWM. (Experimental results)

The three-level inverter possess the predominance of suppressing CM noise at source, while several problems can be found for the zero-CM SVPWM. Firstly, the range of modulation index becomes smaller. Without using the large voltage vector, the modulation index of three-level inverter is reduced to 0.866 times of normal SVPWM.

Secondly, switching loss is twice of the conventional SVPWM. As shown in Fig. 13(a), there are four switching events during one switching period, which is two times of traditional SVPWM as shown in Fig. 13(b). The absence of redundancy zero vector to guarantee zero-CM voltage output results in extra switching events.

In addition, for zero-CM SVPWM, the selected voltage vectors can be with only 7 vectors rather than 27, which can make larger voltage stress on the load inductors and generate bigger current ripple and THD. The current ripple of zero-CM

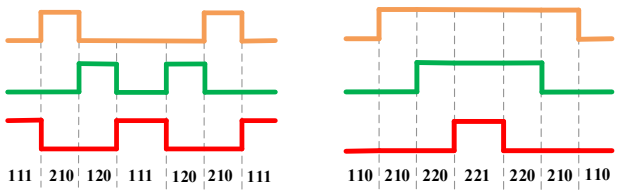

Fig. 13. (a) Sequence of voltage space vector in sector I for zero-CM SVPWM. (b) Sequence of voltage space vector in sector I for normal SVPWM.

SVPWM is obviously bigger than normal SVPWM, and THD increases from 2.78% to 4.65% under the condition of inductor 0.5mH and modulation index 0.9.

What's more, only using medium voltage vector is difficult for voltage balancing. Usually, the small vector in pairs have opposite effect on neutral point and make the neutral point potential (NPP) balancing to be possible for normal SVPWM. However, the existence of only medium vector makes NNP variation more serious. Therefore, zero-CM SVPWM with only medium vector is hardly capable of balancing neutral point voltage with modulation.

Table I summarizes the comparison between normal SVPWM and zero-CM SVPWM. Zero-CM SVPWM pays the prices of higher THD, more difficult neutral voltage balancing and lower modulation index to achieve theoretical elimination of CM voltage.

TABLE I
THE COMPREHENSIVE COMPARISON BETWEEN SVPWM AND ZERO-CM

Performance	Normal SVPWM	Zero-CM SVPWM
Current ripple	Smaller	Bigger
NPP balance	Easier	Difficult
Modulation index	1	0.866
CM voltage	V_{dc}/3 (amplitude)	0 (theoretically)

IV. CM NOISE REDUCTION FOR PARALLELED INVERTERS

With analogy to the three-level inverters, another major topology is the paralleled inverters. Three-level inverter can achieve zero CM voltage by introducing phase voltage of zero. Paralleled inverters are still with positive or negative DC voltage for each phase-leg output, but with six phase-legs, which is also able to achieve the sum of all phase voltages to be zero. Compared with three-level inverter, paralleled inverter is able to achieve zero CM voltage together with improved current ripple and THD, which will be discussed in this part.

Fig. 14 shows the topology of paralleled inverters with three-phase load. Two inverters share the same DC-link with mid-point of O. The AC output of the two inverters should be connected with three coupling inductors whose main inductance is used to limit the circulating current caused by the voltage difference between two inverters. The common terminals (A, B, C) of the coupling inductors is connected to the three-phase load, which could be motor or grid and so on. The three terminals CM voltage can conduct through the load grounding capacitors to the ground. The CM voltage, expressed in (2), is the average value of six switching voltage values of the six phase-legs, which are switching between V_{dc}/2 and -V_{dc}/2 with reference to O. Because the phase-leg number is even, it is possible to achieve the sum to be zero, and realize zero CM voltage output.

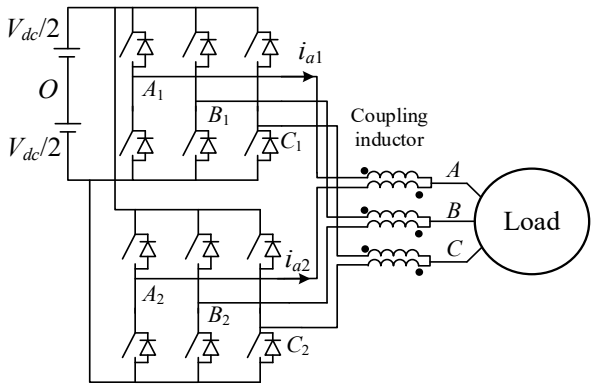

Fig. 14. Topology of paralleled inverters.

$$V_{cm} = \frac{1}{3}\left(V_{AO} + V_{BO} + V_{CO}\right) = \frac{1}{6}\left(V_{A_1O} + V_{B_1O} + V_{C_1O} + V_{A_2O} + V_{B_2O} + V_{C_2O}\right) \quad (2)$$

[34]−[36] introduced the most popular modification of PWM for paralleled inverters in recent years which is the interleaved PWM, whose CM voltage can reduce to V_{dc}/6 rather than zero. A novel zero-CM PWM has been developed for paralleled inverter, which is different from interleaved PWM and can achieve zero CM voltage output theoretically [37]−[40]. The zero-CM PWM for paralleled inverters is based on the paralleled voltage vectors, which are from the normal voltage vectors for two-level inverters, shown in Fig. 15. The red arrows are the paralleled voltage vectors (210,120,021,012,102,201), which are the combination of two adjacent normal vectors.

For example, paralleled voltage vector 210 is combined by 100 and 110. It means that the two inverters are with 110 and 100 vector each, and the effective output voltage vector of the paralleled inverters could be 210. All these six paralleled voltage vectors are with three "1" and three "0" in the six switching status, which means the CM voltage is zero. Also, paralleled zero vector 111 (111+000 and 000+111) is with zero CM voltage, too. The paralleled voltage vectors divide the plane into six sectors. The reference voltage V^* can be combined by the two adjacent paralleled voltage vectors and the paralleled zero vector. Similar like SVPWM in normal three-phase inverter, the action time t_1 and t_2 can be calculated in each switching cycle T_s for the two adjacent paralleled voltage vectors, with the remaining time t_0 for the paralleled zero vector.

Then, the action time for the paralleled voltage vectors should be distributed to the two inverters. The regular distribution method is following the seven-segment SVPWM. With the case in the first sector, the vector distribution is shown in Fig. 16. In the first and last segment, such zero vector 111 is applied that inverter 1 is with 111 and inverter 2 is with 000. In the 2nd and 6th segment, they are the paralleled vector of 210.

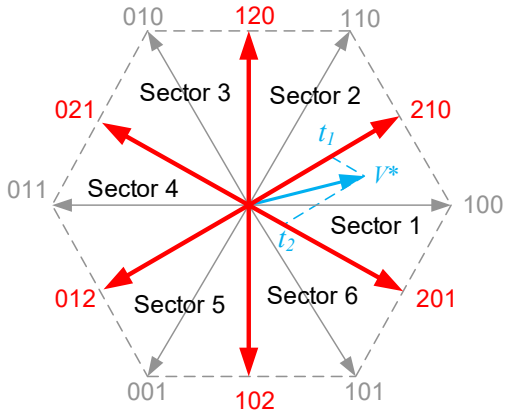

Fig. 15. Voltage vectors for paralleled inverter.

Inverter 1 is with 110 and inverter 2 is with 100. In the 3rd and 5th segment, they are with the paralleled vector of 201 so that inverter 1 is with 100 and inverter 2 is with 101. In the central zone, it is with zero vector so that inverter 1 is with 000 and inverter 2 is with 111.

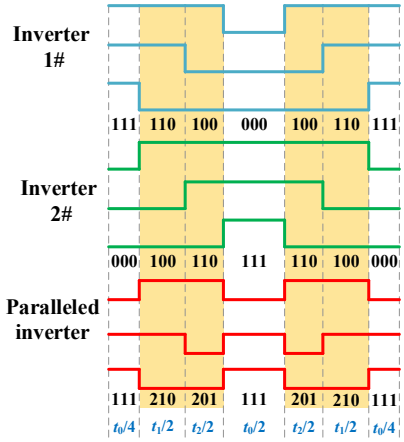

Fig. 16. Zero CM PWM Vector Distribution: Normal Seven-Segment.

However, the vector distribution in Fig. 16 has a serious problem: the voltage difference between the two inverters cannot be balanced in the switching cycle. This can bring a low frequency circulating current between the two inverters and make the coupling inductors to be big. For example, in t_1 period, inverter 1 is with 110 and inverter 2 is with 100, there is a fundamental difference between the voltage vectors in two inverters, and a low frequency coupling inductor is needed to limit the circulating current. Modification can be made in Fig. 16: in the 5th and 6th segment, the vectors for inverter 1 and inverter 2 are switched to each other and be opposite of that in the 2nd and 3rd segment. Then in the whole switching cycle, the difference between the voltages in two inverters will be balanced and the circulating current can be balanced in the switching cycle, too. Fig. 17 shows the modified vector distribution.

However, the switching sequence in Fig. 17 also has a problem that some phases (Phase-*C* of inverter 1 and Phase-*B* of inverter 2) are switching four times in one switching cycle, which is twice of the normal SVPWM and will bring extra switching losses. A further modification has been done for Fig. 17: exchanging the sequence of segment 5 and segment 6, and

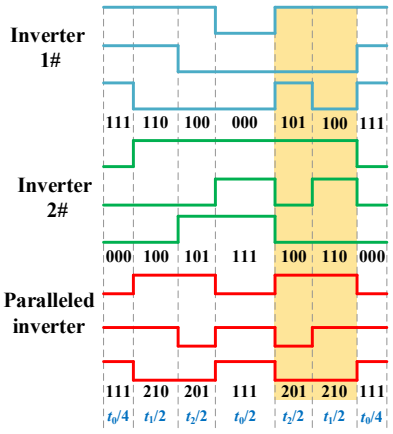

Fig. 17. Zero CM PWM Vector Distribution: Modification with voltage balancing.

the new final distribution is shown in Fig. 18. Then, the switching actions for every phase-leg is twice in every switching cycle. Also, the voltage balancing between two inverters can be kept in each switching cycle, too. Nevertheless, the change of sequence of segment 5 and segment 6 will make some pulses not symmetrical in the switching cycle.

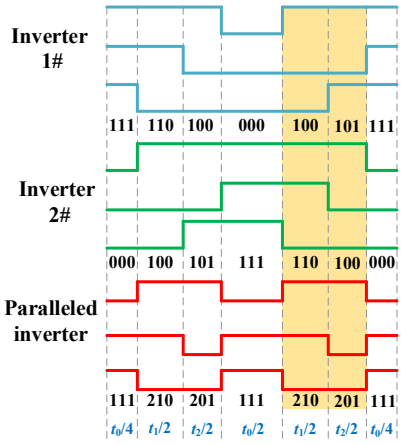

Fig. 18. Zero CM PWM Vector Distribution: Modification with voltage balancing & switch actions.

Discussion from Fig. 16 to Fig. 18 have demonstrated the zero-CM PWM for paralleled three-phase inverters in Sector 1 in the space vector plane. The same approach can derive the switching sequence of zero-CM PWM in Sector 2 to Sector 6. Then, zero-CM PWM can be achieved in the whole line cycle in the paralleled three-phase inverters. The algorithm has been implemented in DSP controller and tested in a prototype of paralleled three-phase inverters, the corresponding experimental results are shown in Fig. 19–Fig. 22.

The experiments are with 20kHz switching frequency and 200V DC voltage. Coupling inductor is with main coupling inductance of 0.5mH. Fig. 19 shows the comparison of CM voltage with normal SVPWM, interleaving and zero-CM PWM. It is matching well with analysis that interleaving can reduce the amplitude of CM voltage from $V_{dc}/2$ to $V_{dc}/6$, but zero-CM PWM can further reduce the CM voltage. The burr of CM voltage in zero-CM PWM is caused by non-ideal effect of system, including dead-time and commutation transient. However, the burr is with very short period and has little impact

on the CM current. Fig. 20 is the spectrum of the CM voltage shown in Fig. 19. Both SVPWM and interleaving spectrum concentrate on switching frequency and its harmonics, whereas zero-CM PWM harmonic component is very small, even though the amplitude of CM voltage at switching frequency is only 0.008 p.u.

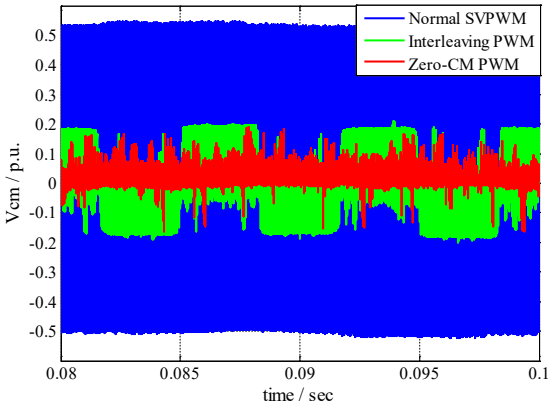

Fig. 19. Experimental results: CM voltage comparison.

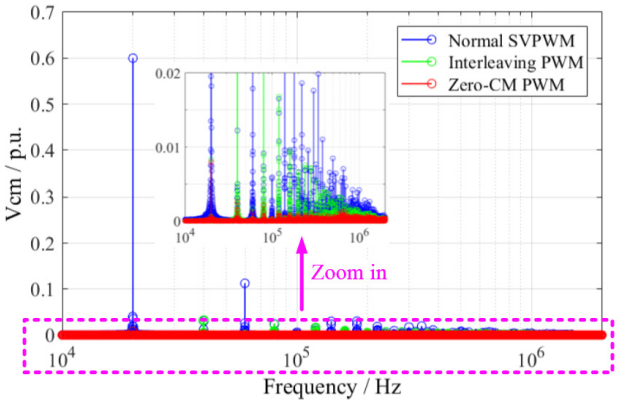

Fig. 20. Experimental results: CM voltage spectrum comparison.

With 5nF CM capacitance in the CM loop, the CM current is measured and compared in Fig. 21. Interleaving can reduce the CM current amplitude to about one quarter of normal SVPWM. Zero-CM PWM can significantly reduce the CM current further and make it close to zero. According to FFT analysis, both interleaving and zero-CM PWM can cancel the odds harmonics of switching frequency greatly, and improve the output current quality. It is better than zero-CM PWM in three-level inverters whose output current quality is much worse than normal PWM.

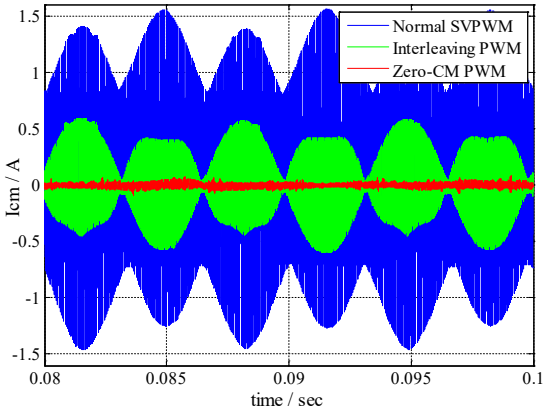

Fig. 21. Experimental results: CM current comparison.

The conducted CM EMI shown in Fig. 22 is measured by EMI test receiver according to standard CISPR11 requirement. Interleaving PWM hardly contributes to reducing conducted CM EMI. For EMI spectrum range from 150kHz to 2MHz, zero-CM PWM has great advantage in reducing EMI compared with other two mentioned methods. Especially the range from 150kHz to 600kHz, the reduction of EMI even has exceeded 20dB. These results verify the fact that zero-CM PWM possesses the ability to suppress conducted CM EMI and PWM series plays a dominant role in the low frequency of EMI.

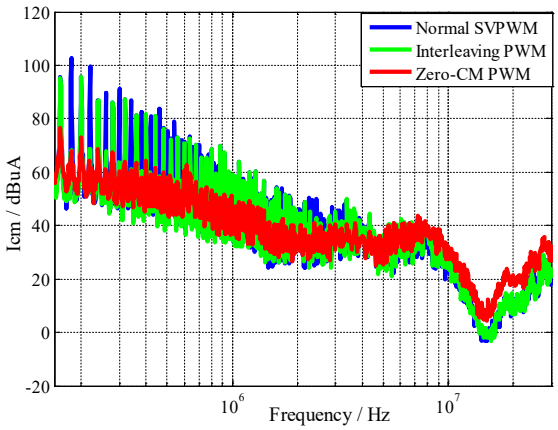

Fig. 22. Experimental results: Conducted CM EMI comparison.

A small coupling inductor can solve the concern of circulating current between the two paralleled inverters since the voltage is balanced between the two inverters in each switching cycle by the improved sequence of zero-CM PWM in Fig. 18, the circulating current is also reset in each switching cycle. In addition, the phase-shift effect in zero-CM PWM can cancel the current ripple in paralleled inverters and make the output current quality to be close to that of interleaving.

V. Conclusions

This paper gives a tutorial introduction of CM noise reduction for three-phase PWM inverters through modified PWM methods. Pulse sequences, considered as the CM noise source, is the key solution in this paper to improve CM noise problem. First, the CM voltage source for regular three-phase two-level is analyzed. Two improved PWM methods can reduce the CM voltage amplitude, and reduce the CM noise current together with the CM loop impedance. More advanced topologies are with the capability of CM voltage elimination, including three-level inverters and paralleled inverters. This paper introduced the series work of zero-CM PWM for three-level inverters and paralleled inverters. The main conclusions from this paper are summarized as follow:

(1) For normal SVPWM and DPWM, CM voltage amplitude is half DC-link voltage, which appears with zero voltage vectors. By avoiding zero vector, improved PWM methods can reduce the CM voltage amplitude to $V_{dc}/3$.

(2) Reduction of CM voltage amplitude does not mean reduction of CM noise current. Spectrum of CM voltage should be analyzed to avoid the resonant frequency of CM loop. PWM method design should be together with switching frequency and system parameters.

(3) For three-level inverters, by combining the reference voltage with particular vectors, zero CM voltage can be achieved theoretically. But it brings problems of reduction of modulation index, higher switching loss, worse harmonics and serious neutral point potential fluctuation.

(4) For paralleled inverters, interleaving can reduce the CM voltage but cannot eliminate it. Zero-CM PWM is achieved by using paralleled voltage vectors for reference voltage combination, and actively distributing to two inverters with consideration of voltage balancing between two inverters.

This paper is mainly presenting recent progress of CM EMI mitigation based on PWM methods. With the development of fast switching wide-band-gap power electronics devices in motor drives, the challenge of CM EMI becomes more serious. For transportation electrification requirement of high power density, large passive filter based CM EMI mitigation methods is rather difficult. The mitigation methods fully considering topologies, modulation and machine are going to be more preferable. As previously analyzed, zero-CM PWM for paralleled inverter is the optimal choice to reduce CM noise, compared to other modified PWM and topologies. However, dead time effect and switching transient have great impact on CM voltage elimination; circulating current, the inherent problem of paralleled topology, is needed to be paid enough attention to and suppressed. The optimization design to weaken the influence of these problems may improve the performance of zero-CM PWM, which can be consider as potential additional work. Further study in this area could be interesting and useful.

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Dong Jiang (S05'–M12'–SM'16) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2005 and 2007, respectively. He started working toward the Ph.D. degree in high density motor controller from the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, in 2007 and was transferred with his advisor in 2010 to the University of Tennessee, Knoxville, TN, USA, where he received the Ph.D. degree in Dec. 2011.

He was with the United Technologies Research Center, Connecticut as a Senior Research Scientist/Engineer from Jan 2012 to July 2015. He has been with the Huazhong University of Science and Technology, Wuhan, China, as a Professor since July 2015. His major research interests include power electronics and motor drives, with more than 50 published IEEE journal and conference papers in this area.

Dr. Jiang is an Associate Editor for the IEEE Transactions on Industry Applications. He received two best paper awards in IEEE conferences.

Jianan Chen (S'17) was born in Nantong, China, in 1992. He received the B.Eng. degree from Nanjing University of Technology, Nanjing, China, in 2015. He received the M.S. degree in Electrical Engineering from Huazhong University of Science and Technology, Wuhan, China, in 2018. Now he is currently working towards Ph.D. degree in Electrical Engineering in Huazhong University of Science and Technology, Wuhan, China.

His current research interests include multilevel converters, PWM for power converters, and electromagnetic interference of power electronics system.

Zewei Shen (S'17) was born in Hubei, China, in 1990. He received the B.S. degree in automation from the Department of Automation, Huazhong University of Science and Technology, Wuhan, China, in 2012. He is currently working toward the Ph.D. degree in electrical engineering at Huazhong University of Science and Technology, Wuhan, China.

His current research interests include paralleled converters and high power density motor drive.