Coordinated Control for Harmonic Mitigation of Parallel Voltage-source Inverters

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(Invited)

***Abstract*—The increasing use of power electronic devices can deteriorate the power quality by introducing voltage and current harmonics. In islanded microgrids, the presence of nonlinear loads can distort the point of common coupling (PCC) voltage, while the dead-time effect can also bring additional circulating current harmonics among parallel inverters. To simultaneously attenuate the PCC voltage harmonics and suppress the dead-time induced circulating current harmonics, this paper proposes a coordinated control strategy for harmonic mitigation of parallel inverters. The proposed control strategy allows inverter impedances to be properly reshaped at selective harmonic frequencies. As a consequence, the PCC voltage harmonics are filtered by the inverter operating in the harmonic compensation mode (HCM), whereas the dead-time induced circulating current harmonics are suppressed by the inverter operating in the harmonic rejection mode (HRM). Experimental results from an islanded microgrid prototype with two parallel inverters are provided to validate the effectiveness of the proposed control strategy.**

***Index Terms*—Dead-time, harmonic mitigation, impedance shaping, parallel inverters, nonlinear load.**

I. INTRODUCTION

A MICROGRID is a small-scale power grid formed by electrical loads and distributed generation (DG) units. It can either operate in the grid-connected mode to exchange power with the main grid or run autonomously during grid faults [1]. In the islanded operation mode, parallel voltage-controlled inverters are normally employed as the interfaces between DG units and the AC microgrid [2–3]. To properly share the load power among parallel inverters, the well-known droop control, which emulates the characteristic of a synchronous generator, has been extensively studied and developed over the last decade [4–7].

Apart from the power sharing issue, power quality becomes another concern due to the intensive use of power electronic devices. On one hand, switching dead-time, which is originally employed to prevent the shoot-through between the lower and upper switches, can introduce extra voltage harmonics [8–9] into the inverter output voltage. Since the induced low-order voltage harmonics can hardly be attenuated by LC filters, large current harmonics will circulate among parallel inverters [10]. As a consequence, inverter output current waveforms are distorted, and additional harmonic power has been produced. To address this problem, advanced voltage controllers are designed based on the internal model principle (IMP) [11–14]. In specific, the harmonic mitigation can be readily achieved by implementing either a multiple resonant (MR) or a repetitive controller (RC) in the stationary frame [11–13]. Moreover, a proportional integral (PI) controller in the synchronous *dq* frame also has a similar effect [14], as periodical signals are mapped into corresponding DC components through the *abc* to *dq* transformation. However, it has been pointed out that the harmonic components in inverter output voltage cannot be eliminated, as the sampled voltage harmonics may not reflect their real values due to the precision limit of voltage sensors [15]. Although the remaining voltage harmonics are quite small, the induced circulating current harmonics are still significant since grid impedances have little blocking effect against such low-order harmonics. Alternatively, a more effective solution is to increase inverter output impedances at selective harmonic frequencies. To accomplish this objective, virtual impedance controls and current feedforward controls are utilized based on the feedback of the inverter output current [16–18]. In [15] and [19], large virtual impedances are adopted to effectively suppress the current harmonics and allow inverters to operate in the harmonic rejection mode (HRM).

On the other hand, the current harmonics of nonlinear loads can also distort the point of common coupling (PCC) voltage [20]. Such voltage quality degradation is essentially caused by the harmonic voltage drops across grid impedances and inverter output impedances, and may still occur even if pure sinusoidal reference voltages are provided for inverters. In [21], the implementation of the resonant controllers effectively reduces inverter harmonic impedances so that the PCC voltage harmonics can be attenuated. In order to further improve the PCC voltage quality, negative/capacitive virtual impedances are adopted to compensate grid impedances in [22–24]. Similar techniques are also reported in [25]–[26], which can equivalently reduce grid impedances by feeding the PCC voltage harmonics to the reference voltage through a pre-defined damping factor. The above control algorithms

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allow the inverter to operate in the harmonic compensation mode (HCM) and actively supply the current harmonics of nonlinear loads.

Nevertheless, the superposition of the nonlinear load and dead-time effect further complicates the controller design for parallel inverters. As inverter output impedances are equally designed to ensure the power sharing accuracy in conventional scenarios [27]–[28], a compromise has to be made between the PCC voltage harmonics compensation and the circulating current harmonics suppression. Specifically, large inverter output impedances can degrade the PCC voltage quality due to nonlinear loads, while small inverter impedances will lead to considerable circulating current harmonics because of the dead-time.

To simultaneously mitigate the PCC voltage harmonics and dead-time induced circulating current harmonics, this paper proposes a coordinated harmonic mitigation strategy for parallel inverters. By properly shaping inverter output impedances, the PCC voltage harmonics are attenuated by the HCM inverter, while the suppression of dead-time induced circulating current harmonics is accomplished by the HRM inverter. The proposed impedance-shaping control is achieved by directly feeding the inverter output current to the PWM modulator, and hence its feasibility is not limited by the voltage control bandwidth. This paper starts with modeling the parallel-inverter system in the harmonic-frequency domain. Then, the influence of dead-time is analyzed, and the proposed harmonic mitigation strategy is also elaborated in details. Finally, experimental results from an islanded microgrid with two parallel inverters are provided to validate the effectiveness of the proposed control strategy.

II. System Configuration and Modeling

A. System Configuration

Fig. 1 depicts a typical configuration of an islanded AC microgrid, where DG units supply power to both linear and nonlinear loads at the PCC through interfaced parallel inverters. Z_{g1} and Z_{g2} denote grid impedances between inverters and the PCC. Since parallel inverters are distributed at different locations, only local measurements, *i.e.*, the output voltage and current, are utilized in the inverter controllers.

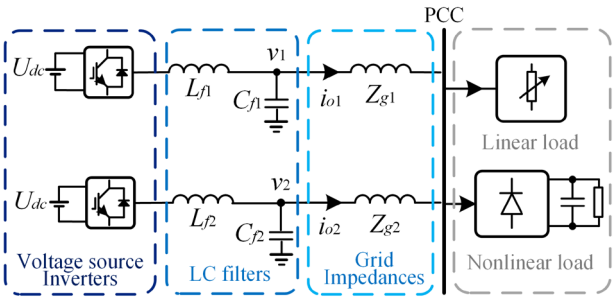


Fig. 1. Typical configuration of an islanded AC microgrid.

The detailed control algorithm for an individual inverter is illustrated in Fig. 2, and the overall controller consists of an outer-power loop and an inner-voltage loop. The outer-power

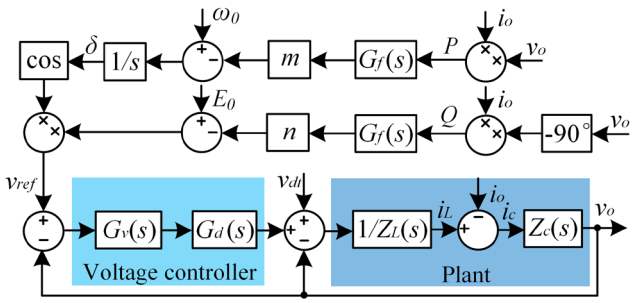


Fig. 2. Control scheme of a voltage-controlled inverter.

loop is utilized to ensure the fundamental power sharing performance by dropping the reference voltage magnitude and frequency from their nominal values ω_0 and E_0, respectively [2]. Notice that for single-phase inverters, first-order low-pass filter $G_f(s)$ are also utilized to attenuate the double-line frequency power ripple. The synthesized reference voltage v_{ref} is tracked by an inner-loop voltage controller, and the fundamental voltage error can be eliminated through a proportional resonant (PR) controller, which can be expressed as

$$G_v(s) = k_p + \frac{2k_i\omega_{c0}s}{s^2 + 2\omega_{c0}s + \omega_0^2} \tag{1}$$

where k_p and k_i are the proportional gain and resonant gain; ω_0 and ω_{c0} are the resonant frequency and cut-off frequency. $G_d(s) = e^{-1.5sT_s}$ denotes the control system delay, which contains one sampling period of the computation delay and a half sampling period of the PWM delay [18]. The AC side output voltage is filtered by an LC filter to remove the switching harmonics, and the transfer functions $Z_L(s)=sL_f$, $Z_c(s)=1/sC_f$ represent the inductor impedance and capacitor impedance, respectively. As dead-time can also impose additional voltage harmonics on the output voltage, a disturbance signal v_{dt} is added after $G_d(s)$ to represent such an influence.

B. Analysis of the dead-time effect

Carrier and voltage waveforms of a single-phase inverter with the unipolar Sinusoidal Pulse Width Modulation (SPWM) scheme are shown in Fig. 3. The modulation wave v_r is compared with the carrier wave u_c to generate the control signals for switches Q_1-Q_4. t_{sw} is the switching period, and t_d represents dead-time. For simplicity, the inverter output current i_o is assumed to be in phase with the modulation wave v_r, and the ideal output voltage v_{o*} (ignore the dead-time) and real output voltage v_o (consider the dead-time) are plotted and compared at different stages according to the corresponding current paths. During the time interval Δt_1, v_o has a positive output voltage since Q_1 and Q_4 conduct, whereas during the time interval Δt_2, v_o has a negative polarity since Q_2 and Q_3 conduct. Within the dead-time interval t_d, none of the four switches conduct, and inverter output current i_o flows through anti-parallel diodes. Therefore, the output voltage polarity is negative during the time interval Δt_3, and positive during Δt_4. By comparing v_{o*} and v_o, dead-time equivalently imposes additional voltage pulses v_{dt} on the ideal voltage v_{o*}. Through the Fourier decomposition [15], the magnitude of harmonic content in v_{dt} can be derived as

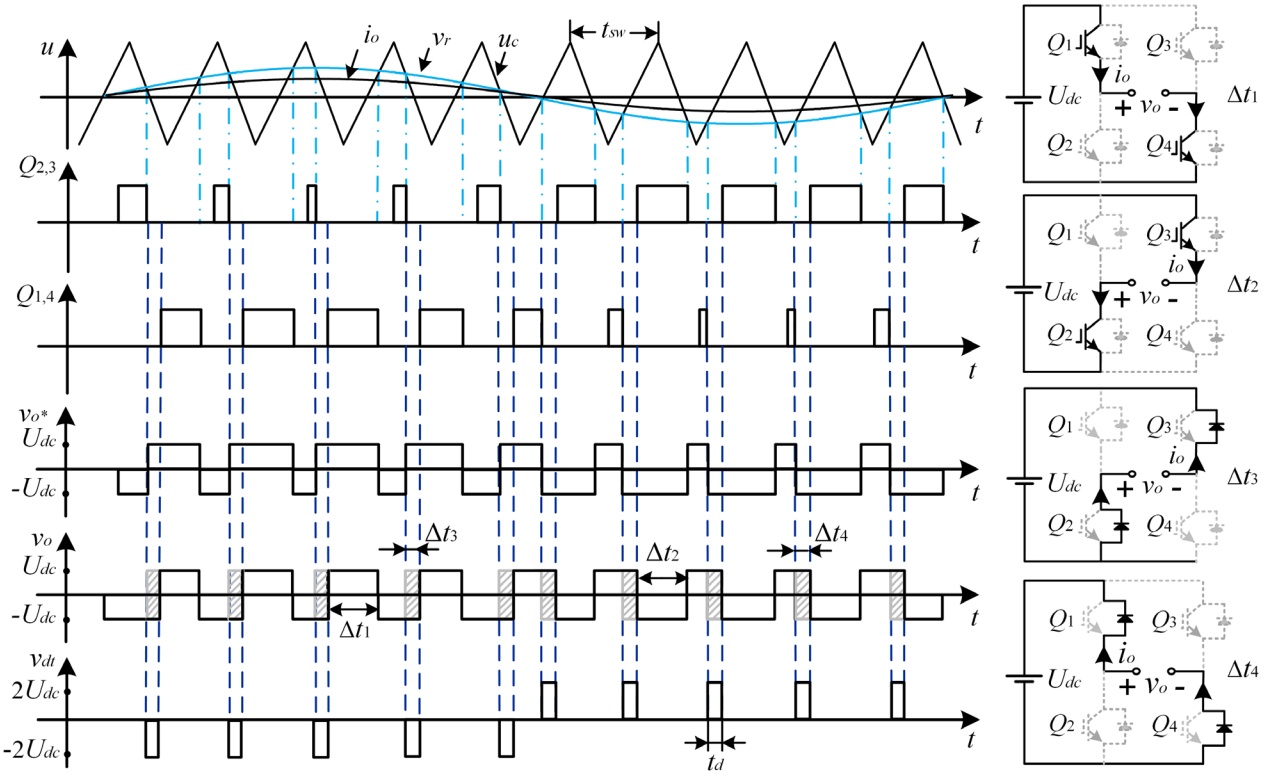


Fig. 3. Unipolar SPWM modulation scheme and corresponding current paths for an H-bridge inverter.

$$\left|v_{dt}^{h}\right| = \frac{8U_{dc}}{h\pi}\frac{t_d}{t_{sw}} \quad (h = 1,3,5,...) \tag{2}$$

where U_{dc} is the DC input voltage. The magnitude of voltage harmonics in v_{dt} will reduce as the harmonic order h goes up. Therefore, the dominant voltage harmonics introduced by the dead-time are the low-order ones. A more intuitive illustration is shown in Fig. 4, which plots the 1st, 3rd, and 5th order harmonic components after the Fourier expansion. Notice that the magnitude of the original voltage pulses v_{dt} is intentionally scaled down since it is much larger than its harmonic contents. Besides, higher-order harmonics also exist, although not shown in Fig. 4 for clarity. From Fig. 4, the phases of voltage harmonics are synchronized with the voltage pulses v_{dt} as well as the output current i_o

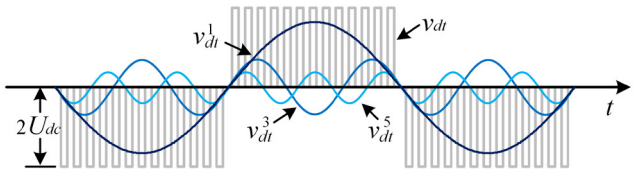


Fig. 4. 1st, 3rd, and 5th-order voltage harmonics introduced by dead-time.

To further investigate the dead-time influence on parallel inverters, the phase difference δ between the inverter output current and the PCC voltage can be calculated as

$$\delta = \arctan\frac{Q}{P} \tag{3}$$

For the parallel-inverter system shown in Fig. 1, the phase difference between i_{o1} and i_{o2} can thus be expressed as

$$\Delta\delta = \delta_1 - \delta_2 = \arctan\frac{Q_1}{P_1} - \arctan\frac{Q_2}{P_2} \tag{4}$$

Suppose that real and reactive power can be accurately shared between the two inverters, *i.e.* $P_1/P_2 = m_2/m_1 = n_2/n_1 = Q_1/Q_2$, the phase difference $\Delta\delta$ would become zero, which means i_{o1} and i_{o2} are exactly in phase with each other. However, this cannot happen in practice due to the imperfect fundamental power sharing. Although real power can always be accurately shared between inverters, the reactive power sharing accuracy is influenced by mismatched grid impedances [2], [7]. Therefore, a small angle difference $\Delta\delta$ normally exists. Fig. 5 shows the dead-time impact on parallel inverters. Although the phase difference $\Delta\delta$ is small for fundamental currents i_{o1} and i_{o2}, it still leads to a large phase difference ($h\Delta\delta$) between the dead-time induced voltage harmonics v^h_{dt1} and v^h_{dt2}. Since grid impedances have little blocking effect against low-order

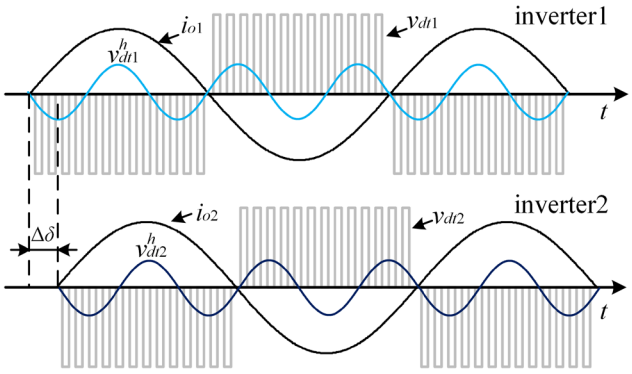


Fig. 5. Dead-time influence on parallel inverters.

harmonics, the difference between v^h_{dt1} and v^h_{dt2} can cause considerable circulating current harmonics between the two inverters.

C. System Modeling in the Harmonic-frequency Domain

From a control perspective, an inverter can be regarded as a multiple input-single output (MISO) system. The input signals include the reference voltage v_{ref}, the dead-time induced voltage harmonics v_{dt}, and the output current i_o. Among them, v_{ref} is the desired signal that needs to be accurately tracked, whereas v_h and i_o are regarded as disturbance signals. According to the block diagram in Fig. 2, the transfer functions from three inputs to the output voltage v_o are derived as

$$G_{c1}(s)=\frac{V_o(s)}{V_{ref}(s)}=\frac{Z_c(s)G_v(s)G_d(s)}{Z_L(s)+Z_c(s)+Z_c(s)G_v(s)G_d(s)} \quad (5)$$

$$G_{c2}(s)=\frac{V_o(s)}{V_{dt}(s)}=\frac{Z_c(s)}{Z_L(s)+Z_c(s)+Z_c(s)G_v(s)G_d(s)} \quad (6)$$

$$Z_o(s)=\frac{V_o(s)}{-I_o(s)}=\frac{Z_c(s)Z_L(s)}{Z_L(s)+Z_c(s)+Z_c(s)G_v(s)G_d(s)} \quad (7)$$

With the control and circuit parameters listed in TABLE I, bode diagrams of the three transfer functions are plotted in Fig. 6. Among them, $G_{c1}(s)$ reflects the inverter reference-voltage tracking capability. Since $G_{c1}(s)$ has a unity gain at 50 Hz, the fundamental voltage error is significantly reduced. On the other hand, the closed-loop controller has a very limited attenuation ability against the voltage harmonics in v_{dt}, as the gain of $G_{c2}(s)$ is almost unity at low-order harmonic frequencies. Besides, the

TABLE I
CONTROL AND SYSTEM PARAMETERS

Parameters	Descriptions	Values
U_{dc}	DC-link Voltage	130 V
E_0	AC voltage magnitude	100 V
k_p	Proportional gain for G_v(s)	0.1
k_i	Integral gain for G_v(s)	50
ω_0	Fundamental frequency	50 Hz
ω_{c0}	Cut-off frequency for G_v(s)	0.05 Hz
f_{sw}	Switching frequency	5 kHz
t_d	Deadtime	2 μs
L_f	Filter inductor	1 mH
C_f	Filter capacitor	20 μF

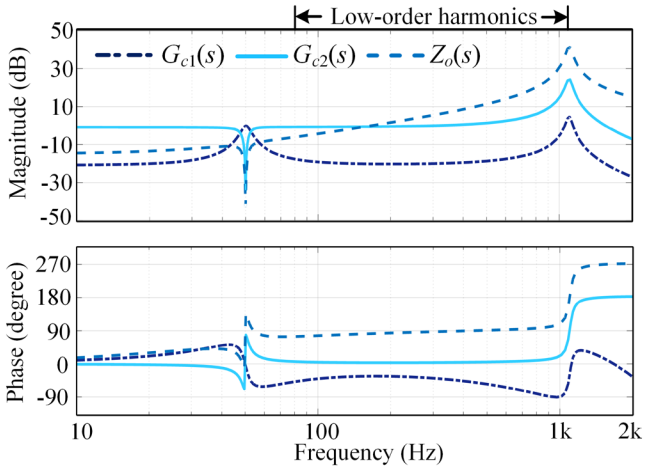


Fig. 6. Bode diagrams of $G_{c1}(s)$, $G_{c2}(s)$, and $Z_o(s)$ with given parameters.

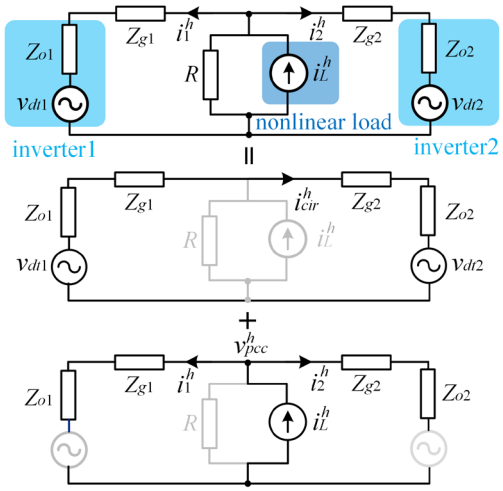


Fig. 7. System equivalent circuit in the harmonic-frequency domain.

output impedance $Z_o(s)$ reflects the inverter's rejection ability against current harmonics, and this impedance can be reshaped for different harmonic mitigation objectives.

Based on the aforementioned analyses, the parallel-inverter system in Fig. 1 can be equivalently modelled by the circuit shown in Fig. 7. The nonlinear load is regarded as a harmonic current source [27], whereas parallel inverters are modelled in their Thevenin's forms. According to the superposition theorem, the total voltage/ current in any part of a circuit equals the algebraic sum of voltages/currents produced by individual sources. Therefore, the dead-time effect and the nonlinear load effect can be analysed separately. The dead-time induced circulating current harmonics i^h_{cir} can be expressed as

$$i^h_{cir}=\frac{v^h_{dt1}-v^h_{dt2}}{Z_{o1}+Z_{g1}+Z_{o2}+Z_{g2}} \quad (h=3,5,7,...) \quad (8)$$

Given that the phase difference between inverter output currents is $\Delta\delta$, the magnitude of i^h_{cir} can be calculated by combining (2) and (8)

$$\left|i^h_{cir}\right|=\frac{8U_{dc}t_d}{h\pi t_{sw}}\cdot\frac{1-\cos(h\Delta\delta)}{Z_{o1}+Z_{g1}+Z_{o2}+Z_{g2}} \quad (h=3,5,7,...) \quad (9)$$

On the other hand, the current harmonics of the nonlinear load can also distort the PCC voltage when flowing across grid impedances Z_g and inverter output impedances Z_o. The PCC voltage harmonic v^h_{pcc} is calculated as

$$v^h_{pcc}=i^h_L\cdot(Z_{g1}+Z_{o1})//(Z_{g2}+Z_{o2}) \ (h=3,5,7,...) \quad (10)$$

From (10), decreasing inverter output impedances Z_o is beneficial for the PCC voltage harmonics mitigation. However, an inherent trade-off exists, since large inverter output impedances lead to serious PCC voltage distortions, whereas small impedances can cause considerable circulating current harmonics. Therefore, a compromise has to be made for the inverter impedance value tuning.

III. PROPOSED CONTROL STRATEGY

A. Basic Principle

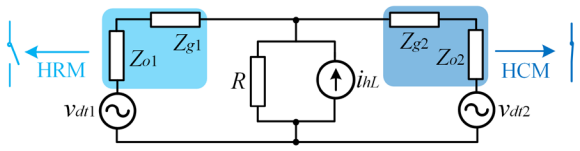


Fig. 8. Principle of the proposed harmonic mitigation technique.

To simultaneously mitigate the PCC voltage harmonics and suppress the dead-time induced circulating current harmonics, a coordinated harmonic mitigation control strategy is proposed to properly shape inverter output impedances, and the basic principle is illustrated in Fig. 8.

In Fig. 8, the inverter output impedance Z_{o1} is greatly increased at selective harmonic frequencies so that inverter 1 operates in the harmonic rejection mode (HRM). Therefore, the circulating current harmonics i^h_{cir} can be suppressed. In the meanwhile, a capacitive Z_{o2} is synthesized to compensate the grid impedance Z_{g2} in the harmonic-frequency domain, which allows inverter 2 to operate in the harmonic compensation mode (HCM). As a consequence, the PCC voltage quality can be improved since the harmonic voltage drops across Z_{o2} and Z_{g2} are eliminated. Notice that almost all the current harmonics of the nonlinear load will be supplied by the HCM inverter. To prevent the overloading, the HCM inverter is intentionally designed to share only a minority of the fundamental power by properly tuning droop coefficients. In this paper, the fundamental power sharing ratio for the HCM and HRM inverters is set as 1:2, yet it can also be flexibly changed to meet specific requirements for different situations.

B. Impedance-shaping Control

To achieve the aforementioned control objectives, output impedances for the HCM and HRM inverter are properly reshaped at selective harmonic frequencies, and Fig. 9 shows the impedance-shaping control for the hth-order harmonic signal. In this paper, the inverter output current is directly fed to the PWM modulator rather than the reference voltage v_{ref}. As a consequence, the feasibility of the impedance-shaping control is not affected by the voltage control bandwidth.

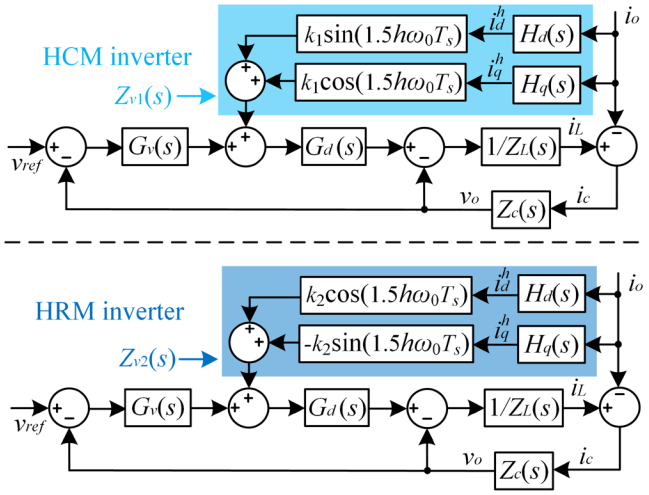


Fig. 9. Impedance-shaping control for the hth-order harmonic signal.

To reshape the inverter output impedance and compensate the control system delay, $Z_{v1}(s)$ and $Z_{v2}(s)$ are employed for the HCM and HRM inverters, respectively. $H_d(s)$ and $H_q(s)$ are the transfer functions of a second-order generalized integrator (SOGI) [29], which can extract the hth-order orthogonal current harmonics from the output current i_o. Without loss of generality, $H_d(s)$ and $H_q(s)$ are given by

$$H_d(s)=\frac{i_d^h(s)}{i_o(s)}=\frac{kh\omega_0\cdot s}{s^2+kh\omega_0\cdot s+h^2\omega_0^2} \tag{11}$$

$$H_d(s)=\frac{i_q^h(s)}{i_o(s)}=\frac{kh^2\omega_0^2}{s^2+kh\omega_0\cdot s+h^2\omega_0^2} \tag{12}$$

where k is a constant that determines the bandwidth of the SOGI filter. The reshaped impedance for the HCM inverter is expressed as

$$Z_o(s)_{HCM}=\frac{Z_c(s)Z_L(s)+Z_c(s)G_d(s)Z_{v1}(s)}{Z_L(s)+Z_c(s)+Z_c(s)G_v(s)G_d(s)} \tag{13}$$

At the harmonic frequency $jh\omega_0$, $H_d(s)$ and $H_q(s)$ are equal to

$$H_d(jh\omega_0)=jh\omega_0/jh\omega_0=1 \tag{14}$$

$$H_q(jh\omega_0)=kh^2\omega_0^2/(kh\omega_0\cdot jh\omega_0)=-j \tag{15}$$

$Z_{v1}(jh\omega_0)$ is calculated as

$$Z_{v1}(jh\omega_0)=k_1\sin(1.5h\omega_0T_s)-jk_1\cos(1.5h\omega_0T_s) \tag{16}$$

According to the Euler's formula, (16) is equivalent to

$$Z_{v1}(jh\omega_0)=-jk_1e^{1.5h\omega_0T_s} \tag{17}$$

Notice that at low-order harmonic frequencies, $Z_c(jh\omega_0)>>Z_L(jh\omega_0)$. Therefore, (13) can be approximated as

$$Z_o(jh\omega_0)_{HCM}\approx jh\omega_0L_f-jk_1 \tag{18}$$

In addition, the reshaped impedance for the HRM inverter is given by

$$Z_o(s)_{HRM}=\frac{Z_c(s)Z_L(s)+Z_c(s)G_d(s)Z_{v2}(s)}{Z_L(s)+Z_c(s)+Z_c(s)G_v(s)G_d(s)} \tag{19}$$

Similarly, $Z_{v2}(jh\omega_0)$ is calculated as

$$Z_{v2}(jh\omega_0)=k_2\cos(1.5h\omega_0T_s)+jk_2\sin(1.5h\omega_0T_s) \tag{20}$$

According to the Euler's formula, (20) is equivalent to

$$Z_{v2}(jh\omega_0)=k_2e^{1.5h\omega_0T_s} \tag{21}$$

Based on the previous assumption that $Z_c(jh\omega_0)>>Z_L(jh\omega_0)$, $Z_o(s)_{\mathrm{HRM}}$ can also be approximated as

$$Z_o(jh\omega_0)_{HRM}\approx jh\omega_0L_f+k_2 \tag{22}$$

C. Tuning of Impedance Values

For the HCM inverter, its output impedance can compensate the gird impedance at the harmonic frequency $h\omega_0$ for the condition that

$$k_1=h\omega_0\cdot(L_f+L_g) \tag{23}$$

where L_g is the grid inductance. Therefore, the PCC voltage harmonics can be mitigated by the HCM inverter. On the other hand, by selecting a positive and large k_1 value, a resistive HRM inverter impedance can be reshaped at the harmonic frequency $h\omega_0$. According to (9), the magnitude of i^h_{cir} for the worst case ($L_g=0$ and $\cos\Delta\delta=-1$) is expressed as

$$\left|i_{cir}^h\right|=\frac{16U_{dc}t_d}{h\pi t_{sw}}\cdot\frac{1}{k_2} \tag{24}$$

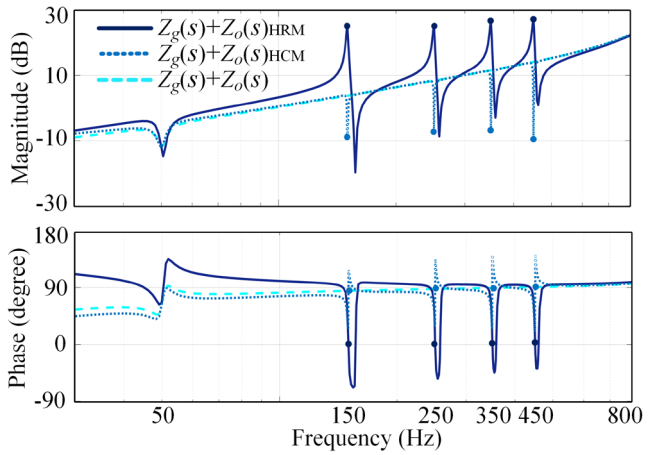


Fig. 10. Impedances for the HCM and HRM inverters.

In order to ensure the magnitude of i^h_{cir} is below a% of the rated output current I_N, the value of k_2 is determined as

$$k_2 \geq \frac{16U_{dc}t_d}{a\%I_N h\pi t_{sw}} \tag{25}$$

In this paper, k_2=15 is selected for the HRM inverter. Notice that the impedance-shaping control shown in Fig. 9 is only implemented at the hth-order harmonic frequency. A more generalized control scheme can be achieved by utilizing multiple parallel SOGI blocks to reshape the inverter output impedances at the 3rd, 5th, 7th, and 9th-order harmonic frequencies. Fig. 10 shows the impedance bode diagrams of the HCM and HRM inverters. Compared with the original case $Z_{sum}(s)=Z_g(s)+Z_o(s)$, the proposed control strategy increases the value of $Z_g(s)+Z_o(s)_{HRM}$ and decreases the value of $Z_g(s)+Z_o(s)_{HCM}$ at selective harmonic frequencies. Therefore, the dead-time induced circulating current harmonics and the PCC voltage harmonics can be simultaneously compensated by different inverters.

IV. Experimental Results

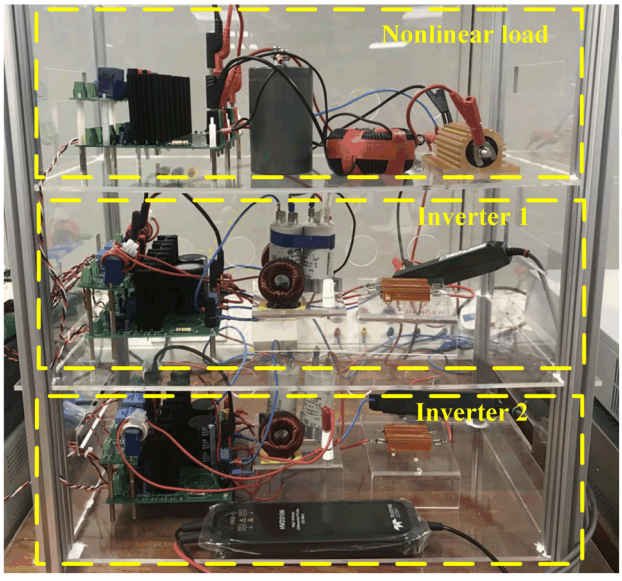


Fig. 11. Laboratory setup for the experimental verification.

Hardware experiments were done to verify the feasibility of the proposed control strategy. Fig. 11 shows the laboratory setup, where two H-bridge inverters were connected in parallel thorough grid impedances. To achieve the proposed harmonic mitigation function, inverter 1 was in the HRM to compensate the dead-time induced circulating current harmonics, while inverter 2 was in the HCM for the PCC voltage harmonics compensation. Grid inductances for inverter 1 and 2 were 0.55mH and 0.63mH, respectively. All the digital samplings and controls were implemented by a PLECS RT box.

A. Parallel Inverters Supply a linear load.

Initially, only a resistive load is connected at the PCC, and Fig. 12 shows the experimental results. Without the proposed control strategy, the values of inverter output impedances and grid impedances are limited for suppressing low-order current harmonics. Consequently, inverter output currents are highly distorted in Fig. 12(a) even if nonlinear loads are not supplied. The FFT analysis result in Fig. 12(c) shows that the current harmonic magnitudes for the two inverters are almost the same, indicating that current harmonics are circulating between the two inverters. According to previous analyses, the circulating current harmonics are introduced by dead-time under the condition that i_{o1} is not exactly in phase with i_{o2}. In order to suppress the circulating current harmonics, the proposed

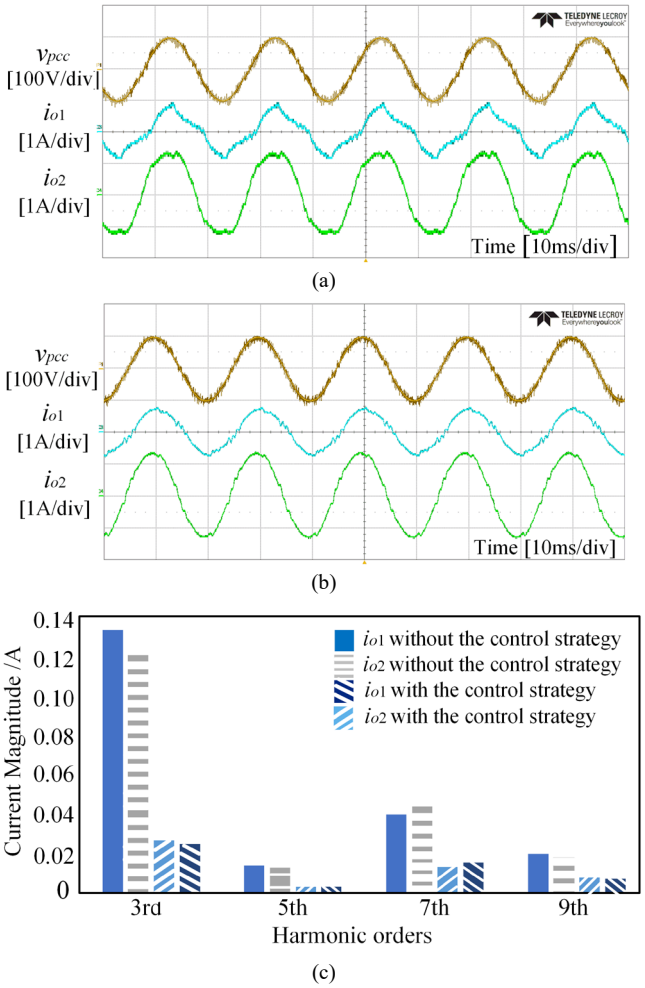
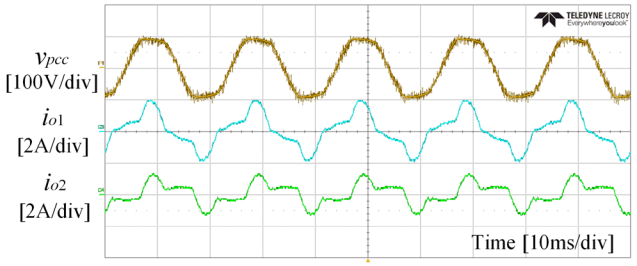


Fig. 12. Experimental results when parallel inverters supply a linear load. (a) without the proposed control strategy (b) with the proposed control strategy (c) current FFT analysis for the two cases.

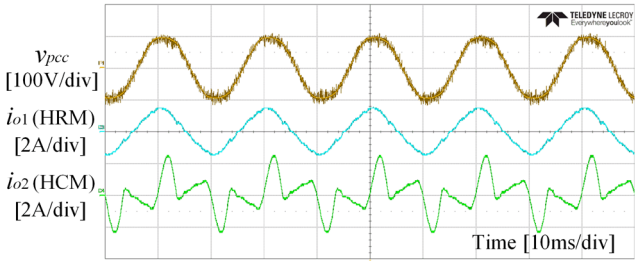
harmonic mitigation technique is tested, and the result is shown in Fig. 12(b). Compared with the previous situation, the current harmonics are effectively damped since inverter 1 operates in the HRM.

B. Parallel Inverters Supply Linear and Nonlinear Loads.

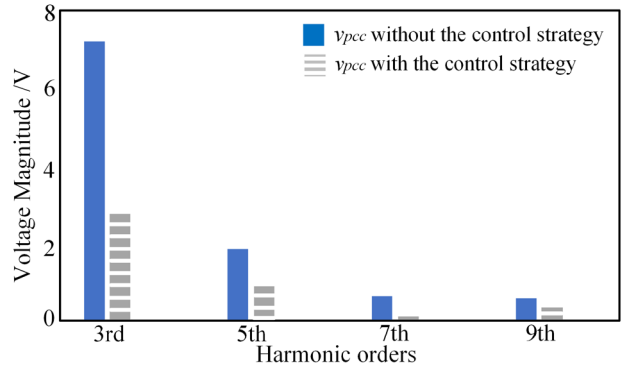
For the next scenario, both linear and nonlinear loads are connected at the PCC, and Fig. 13 shows the experimental results. Originally, the current harmonics of the nonlinear load seriously deteriorate the PCC voltage quality if the proposed control strategy is disabled, and a flat-top PCC voltage waveform can be observed in Fig. 13(a). By implementing the coordinated harmonic mitigation technique, the PCC voltage harmonics are effectively compensated by the HCM inverter, as shown in Fig. 13(b) and Fig. 13(c). Moreover, since almost all the current harmonics are compensated by the HCM inverter, the HRM inverter can supply the majority of the fundamental current with an improved power quality.



(a) without the proposed control strategy



(b) with the proposed control strategy



(c) PCC voltage FFT analysis for the two cases.

Fig. 13. Experimental results when parallel inverters supply both linear and nonlinear loads.

V. CONCLUSION

Power quality is an important aspect for parallel inverters. It is found that apart from nonlinear loads, switching dead-time also causes circulating current harmonics due to an inaccurate fundamental power sharing performance. The superposition of the dead-time and nonlinear load effect introduces considerable low-order harmonics and further complicates the control strategy design. To overcome this problem, a coordinated control strategy for harmonic mitigation is proposed in this paper. The PCC voltage harmonics and the dead-time induced circulating current harmonics are simultaneously mitigated by the HCM inverter and the HRM inverter, respectively. Experimental results from an islanded microgrid prototype with two parallel inverters confirm the effectiveness of the proposed harmonic mitigation technique.

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