A Graphical Analysis on Compensation Designs of Large-gap CPT systems for EV Charging Applications

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Abstract— Capacitive power transfer (CPT) technology is a newly emerging research focus for EV charging applications. Due to the absence of eddy current loss and light weight of the capacitive coupling metal plates, CPT technology is considered to be a promising alternative to the inductive power transfer (IPT) technology. In this paper, the recent designs of large-gap CPT systems designed for EV charging applications are summarized. And a graphical method based on Smith chart is proposed to analyze the characteristics of the compensation designs. With the design objectives graphically represented, the Smith chart can be used to visually analyze the performance of a compensation design, which could be helpful in multi-objectives design of the CPT system. The graphic features of three major design objectives on the Smith chart are investigated. Several guidelines of a good compensation design are concluded.

***Index Terms*—Capacitive power transfer, compensation design, matching network.**

I. Introduction

CAPACITIVE power transfer (CPT) technology transfers energy through the electric field between the air gap. This idea can be traced back to Nikola Tesla's bold idea of transferring wireless energy through the capacitance of the ionosphere. Recently, with the increase of the power capacity of CPT system, it has become a new research focus in the field of wireless charging for electric vehicles.

CPT technology has several unique advantages against the widely-used inductive power transfer (IPT) technology. First, the electric fields do not generate eddy current in the metal material nearby as the magnetic fields do. Besides, the plate capacitive coupling is usually composed of several conductive pairs with no ferrite required, so the coupling part of the CPT is in low cost and light in weight. With these advantages, CPT is considered to be a promising technology in wireless EV charging [1]. The structure of a typical CPT system is shown in Fig. 1

The main challenge in the CPT technology is the small capacitance of the air gap. Unlike the inductive coupling which the coupling coefficient can be enhanced through ferrite, the capacitance between two square metal plate of $1m^2$ at a distance of 10 cm is about 100pF [2]. The small capacitance between the air gaps limited the power transferred through it. High power density could only be achieved either at a high frequency or at a short distance [3]. Therefore, there was few research on CPT systems transferring power above 1kW. And its application on high-power devices such as EV wireless charging was limited.

In 2011, Masahiro [4] proposed the idea of transferring energy through the capacitance between aluminum hubs and metal plates below the tires. In the following researches, a 60W system was built in 2013 at the frequency of 52MHz [5].

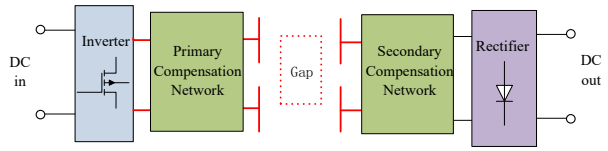

Fig. 1. Common structure of CPT system.

However, this work is based on specialized wheel hubs, which requires modification of the chassis, and realization of the 52MHz inverter is not mentioned. These limitation make it hard to repeat their work, so there is few following research conducted.

In 2015, Jiejian Dai proposed a design composed of conducting foil at the rear of the EV and a foam-based bumper at the charging station. By pressing the foil against the bumper, the coupling capacitance can reach over 10nF. Thus, 1kW power is transferred through a surface area about $0.2m^2$ at a frequency of 540kHz [6].

The two researches above both tend to extend the power limit by means of increasing the coupling capacitance, that is, narrowing the gap distance or enlarging the coupling area. However, with new compensation circuit design, CPT was

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proved to be capable to transfer kW power at a distance of hundreds of millimeters with coupling capacitance of only several picofarad.

The double-sided LCLC CPT system proposed by Lu in 2015 is a breakthrough in designs of high-power long-distance CPT system. The prototype system transfers 2.4kW power at a distance of 150mm with coupling capacitance of only 18.35pF (36.7pF each pair of plates) [7]. This work provides a complete design of CPT system for EV charging which reaches a DC-to-DC efficiency of over 90% and works on a relatively low frequency of 1MHz. The system comprises a ZVS full-bridge converter with SiC MOSFETs, coupling capacitors made with aluminum plates, compensating inductors made with air-core Litz wire solenoids, compensating capacitors combined by film capacitors in series and full-bridge rectifier with SiC diodes. Following the step of this work, various researches have been carried out.

In San Diego State University, Lu refined LCLC compensation to CLLC compensation, which reduces the inductance needed for compensation [8]. A simpler LC compensation is also analyzed comparing with the LCLC topology which seemed to be more feasible as it has less components to tune [9]. Due to its simplicity, it is more likely to be realized on EV charging scenario [10]. Based on the kilowatt CPT system, Hua Zhang proposed a more compact four-plate coupling [11] and six-plate coupling [12], which helps to integrate the capacitor in the compensation network into the coupling and shielding mechanism. In these works, the system is designed to have a constant current output characteristic and is tuned to be slightly inductive, which helps to achieve ZVS condition of the full-bridge inverter.

Siqi Li of Kunming University of Science and Technology developed a dynamic CPT system [13] with a similar design methodology as LCLC-compensate, which is based on the idea of constructing resonant circuit. In order to enhance the power output, Li proposed a compromised design for the capacitors in the compensation network, which enlarges the voltage phase delay between the capacitive gap and helps to achieve a higher power output with a limited voltage on the capacitors. An on-rail CPT system was built in this work which illustrated that CPT system is flexible to be extended in length and thus suitable for road-charging scenarios.

Thanks to the application of SiC MOSFETs and high-voltage GaN FET, the ZVS full-bridge topology is able to work at frequency reaching the ISM band at 6.78MHz or even higher with output power of kilowatts, which helps CPT system to have a higher power density. However, the high-frequency loss caused by the ac resistance of the compensate inductance and the self-resonant frequency of these large inductors deteriorates the performance in high frequency [14]. Thus, the loss on the compensation network must be concerned.

Brandon Regensburger [15] and Kate Doubleday [16] of Colorado Boulder adopted the compensation topology of LC compensation and applied an optimization process in design of the compensation network which minimize the loss in inductor. Sreyam Sinha analyzed the design methodology of the multi-staged compensation network in concern of the stray loss in inductance [17]. Ashish Kumar further developed his conclusion and a more detailed analytical solution of the optimal design with its efficiency upper bound was given [18]. These works lead to a general methodology of multi-stage matching for CPT system.

Toyohashi University of Technology continued their work on the EV CPT system through wheel hubs and is now able to drive the vehicle with power supplied by CPT system[19][20]. Besides, a lot of work focused on the efficiency of the compensation network is done [21]-[23].

To summarize, the compensation design of the high-power large-gap CPT system concerns three main objectives, which are higher power, higher efficiency and desired output and input characteristics. Based on different design objectives, varies methodologies are proposed and several high-power

TABLE I
LIST OF RECENT LARGE-GAP CPT SYSTEM PARAMETERS

	Frequency	Power Out	DC-DC efficiency	Distance	Couple C	Plate Size	Couple Voltage	Plate Voltage	Voltage In	Voltage Out	Rout
LCLC [7]	1MHz	2.4kW	90.80%	150mm	18.35pF	2*610mm* 610mm	3.2kV	7.2kV	265V	280V	33Ω
CLLC [8]	1MHz	2.57kW	89.30%	150mm	14pF	2*610mm* 610mm	3.73kV	4.63kV	400V	450V	79Ω
LC [9]	1.5MHz	112.4W	70.60%	180mm	2.8pF	2*300mm* 300mm	1.73kV	2.51kV	60V	61V	33Ω
Four-Plate [11]	1MHz	1.88kW	85.87%	150mm	11.3pF	914mm* 914mm	5.29kV	5.12kV	270V	270V	39Ω
Six-Plate [12]	1MHz	1.97kW	91.60%	150mm	9.91pF	2*610mm* 610mm	4.18kV	6.51kV	270V	270V	37Ω
Voltage Limited [13]	2MHz	700W	91%	17mm	24pF	230mm* 150mm	1.8kV	1.8kV	300V	300V	145Ω
Efficiency Optimized [15]	6.78MHz	198W	<90%	120mm	0.9pF	2*122.8mm *122.8mm	5.56kV	2.95kV	100V	90V	42Ω
Efficiency Optimized [15]	6.78MHz	557W	<82%	120mm	0.44pF	2*176.8mm *176.8mm	15kV	8kV	200V	161V	46.6Ω
RF [19]	13.56MHz	780W	<78%	- -	36.33pF	on-wheel	1.2kV	0.82kV	230V	195V	50Ω

CPT systems have been built by the time of this paper. Some of them are listed in Table I. Due to their different design objectives, different power levels and different coupling capacitance, it is hard to make a comparison of them directly. In order to analyze varies designs under the same framework, it is necessary to find a general expression of the compensation design.

Taking advantage of their RF research background, Kyohei Yamada and Takashi Ohira promoted a graphical representation of power attenuation on the compensation networks on Smith chart [24]. In fact, for a unique CPT compensation design, its "path" on Smith chart is also unique. And there are several important characteristics of the design besides the attenuation can also be figured out on its path.

In this paper, Smith chart will be used to qualitatively analyze the characteristic of the compensation design in the recent-built large-gap CPT systems. The graphical features of the common design objectives of their design will be summarized and graphically expressed in a graphical way on Smith chart. After that, several guidelines will be proposed for graphically evaluate the compensation for CPT system.

The remainder of this paper is organized as follows. Section II introduces the path of CPT system on Smith chart. Section III, IV and V respectively analyze the graphic features of the three main design objectives. Section VI summarizes the paper and concludes some guidelines that a good compensation should follow and an example design will be given following the proposed guidelines.

II. Path of CPT System on Smith Chart

A. Modeling of CPT system

As a dual model of the IPT system, the common structure of CPT system is similar to an IPT system, which comprises a high frequency inverter, primary compensation network, coupling gap, secondary compensation network and high frequency rectifier (Fig. 1).

Here, we illustrate a demo double-side LC compensation CPT system shown in Fig. 2.

The coupling capacitance can be modeled as an equivalent ∏-section circuit [25] as Fig. 3. The compensation network on both sides are modeled as lumped circuits. As the main power is transferred in the band of the fundamental frequency, the fundamental harmonic approximation method can be used to simplify the model. Thus, the inverter is modeled into a sinusoidal ac voltage source and the load and the rectifier is simplified into an equivalent resistor as

$$R_L = \frac{8}{\pi^2} R_{dc} \tag{1}$$

The lumped circuit model of the demo CPT system under the fundamental harmonic approximation is shown in Fig. 4. It should be noticed that the Capacitor C_{ex} of the compensation network and the Capacitor C_{in} of the equivalent circuit of the gap are combined into C_1 and C_2.

Looking from the power source side, the load resistor R_L is converted to Z_1, Z_2, Z_3, Z_4, Z_5 with the compensation and coupling components connected in cascade.

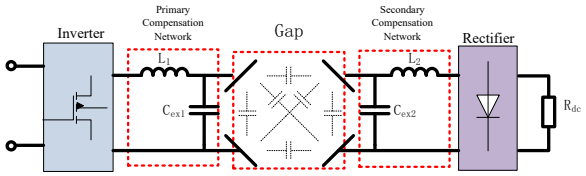


Fig. 2. A typical double-side LC compensation topology.

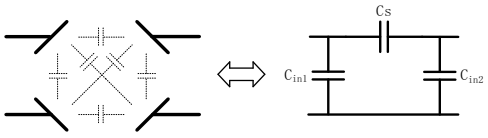


Fig. 3. Equivalent circuit of the coupling gap.

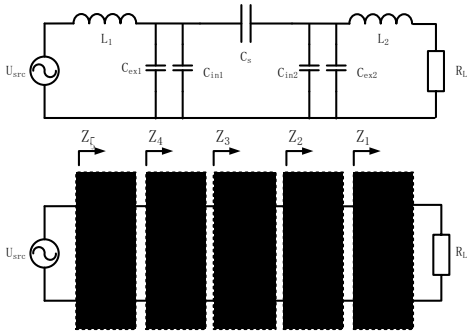


Fig. 4. Simplified model of the double-side LC compensation

B. Path of CPT system

Given the parameters in Table II, the Smith chart of the demo system can be figured in Fig. 5.

To normalize the CPT system with different load, the characteristics impedance of the Smith chart for CPT system is

TABLE II
DEMO CPT SYSTEM PARAMETERS & IMPEDANCE AT EACH STAGE(UNIT : Ω)

R_L	X_{L2}	X_{C2}	X_{Cs}	X_{C1}	X_{L1}
50	350.00j	-384.6j	-2000.0j	-568.3j	489.9j
	Z_1	Z_2	Z_3	Z_4	Z_5
	50+350j	2000 +1000j	2000 -1000j	100- 489.9j	100

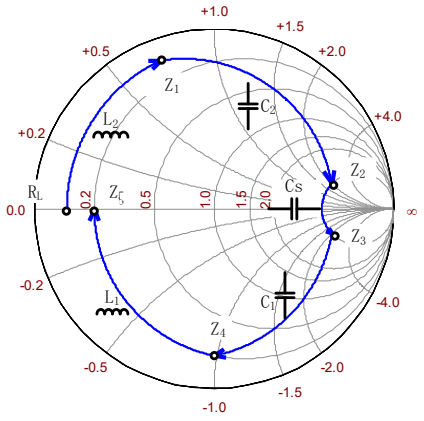


Fig. 5. Smith chart of the Demo CPT system.

selected as $10\times R_L$ in this article. Here, the characteristic impedance is 500Ω.

Depicting the conversion from R_L to Z_5 on Smith chart, the CPT system can be represented by a path in Fig. 5, which composed of arcs representing the lumped reactive components in the circuit model.

As long as the compensation design can be simplified into a circuit model composed of cascaded lumped components, a "Path" similar to Fig.5 can be drawn.

C. *True arc" assumption*

To simplify the analysis of CPT system with Smith chart, a "true arc" assumption is made here. It assumes that all the reactive components in the CPT system are with high quality factor and their dissipative resistors can be neglected when solving the voltages and currents of the circuit. With this assumption, each part of the path can be approximated to pure arcs.

III. Objective of Power

To maximize the power transferred in CPT system, the voltage on the coupling gap need to be increased, which is usually constrained by the breakdown voltage of air gaps.

A. *Graphic features*

Under "true arc" assumption, the active power on the impedance of each stage (Z_1, Z_2, Z_3, Z_4 and Z_5 in Fig. 5.

) equals to the output power P on R_L. With the active power a constant, the follow equation could be deduced as

$$P = U_L^{\,2}\,\mathrm{Re}(Y_L) = U_i^{\,2}\,\mathrm{Re}(Y_i) \tag{2}$$

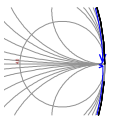
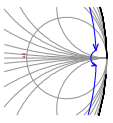
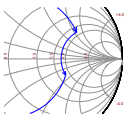
where U_i and Y_i are the voltage and admittance of Z_i.

As for a shunt component in the compensation circuit, the voltage on it is

$$U_i = U_L\sqrt{\frac{Y_L}{\mathrm{Re}(Y_i)}} = U_L\sqrt{\frac{10}{g_i}} \tag{3}$$

Graphically, the shunt components on the right side of the Smith chart will sustain higher operating voltage. Take the systems in [7][9][13] as an example. Their paths on Smith chart and their max voltage on the metal plate normed with output power are listed in Table III. It's obvious that, with the plate voltage limitation, the system with path on the left will be able to transfer larger power.

TABLE III
PLATE VOLTAGE COMPARISON OF THE CPT SYSTEMS

	 [9]LC –Compensate	 [7] LCLC -Compensate	 [13]CLLC Voltage-Limit
$\frac{U_{plate}^{\,2}}{P}$	220 kV²/kW	14 kV²/kW	8.3 kV²/kW

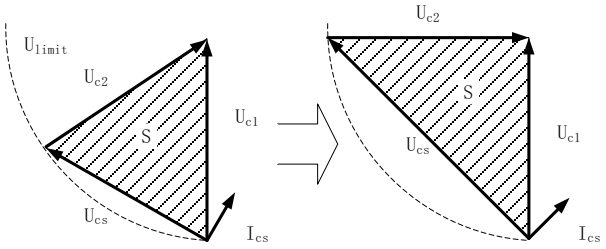


Fig. 6. Maximum of the power under given C_s and U_{limit}.

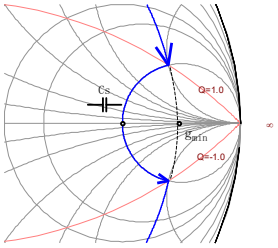


Fig. 7. The path of max power under given C_s and U_{limit}.

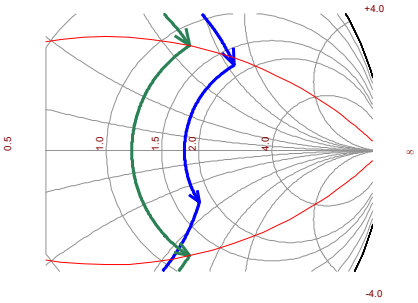


Fig. 8. The path of a real design and the max power optimal result.

B. *Maximal power optimization*

To maximize the power under constrains of voltage limitation. We assume the coupling capacitance is C_s. And the voltage limit of plates on both side is U_{limit}, that is U_{c1}, $U_{c2} < U_{limit}$. The vector diagram of the voltage on the gap is shown in Fig.12. The active power transferred through C_s is

$$P = \dot{I}_{cs}\cdot\dot{U}_{c2} = 2\omega C_s S \tag{4}$$

where S is the area of the slashed triangle in Fig. 6.

Obviously, the power reaches its maximum when U_{c2} is 90 degree in advance of U_{c1}. At this time the reactance of C_s is compensated equally by circuits on both side.

When the maximal power constrain is depicted on Smith chart (Fig. 7), the arc of C_s should be symmetric according to the real axis, starting from the circle of Q=1 and ending at the circle of Q=-1.

As a conclusion, based on the graphic analysis of its path on Smith chart, to further increase the power transmitted in system of [13], whose is the blue path in Fig. 8. The voltages on the plates of two sides need to be balanced. And endpoint of the arc of C_s should be on the circle of Q=±1. The optimized result is the path in green.

IV. Objective of Efficiency

In design of the IPT system, the main loss is considered to be

on the ac resistance of the coupling coils. In CPT system, the loss is considered to be on dissipative resistance of the compensation components, especially the coupling inductors [18]. So the efficiency is usually constrained by the quality factor Q of the components in the compensation network. To maximize the power efficiency, we should minimize the attenuation of the compensation network.

A. Graphic features

There is a simple relationship between the natural logarithm of efficiency and the hyperbolic length of its path on Smith chart [24], which is given by

$$-\log_e \eta = \frac{1}{\sqrt{1+Q^2}} Len_D(\gamma) \tag{5}$$

where η is the compensation efficiency, Q is the quality factor of the component and $Len_D(\gamma)$ is the hyperbolic length of the path D on Smith chart, which is defined by

$$Len_D(\gamma) = \int_\gamma \frac{2}{1-|\gamma|^2} |d\gamma| \tag{6}$$

Here, γ is the complex reflection coefficient which represents a point on Smith chart. And hyperbolic length is a weighted path length of D.

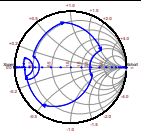
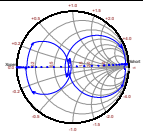
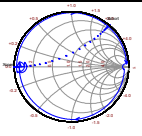
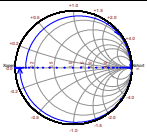
As for the path close to the unity radius circle, $1-|\gamma|^2$ will be close to zero. So the path close to the unity radius circle will result in a higher loss. The paths of the CPT systems designed in reference [7][9][11][13] are listed in Table IV. The hyperbolic length of the arcs and the system loss are also compared in the table. It could be seen that systems with shorter hyperbolic length will have higher efficiency if they use components with the same quality factor to realize the compensation circuit.

Under the "true arc" assumption [24], (6) can be further simplified into

$$Len_D(\gamma) = \frac{1}{R}|X_u - X_0| = |Q_e - Q_s| \tag{7}$$

And the efficiency can be simplified as

TABLE IV
LOSS COMPARISON OF THE CPT SYSTEMS

	 [13]CLLC Voltage-Limit	 [7]LCLC Compensate
loss	9.00%	9.20%
Len_D	10.7218	19.4033
	 [11]LCLC Four-plate	 [9]LC Compensate
loss	14.13%	29.40%
Len_D	71.6305	90.747

$$-\log_e \eta \approx \frac{1}{Q}|Q_e - Q_s| \tag{8}$$

B. Maximal efficiency optimization

Generally, the compensation network in CPT system is based on L-section stage compensations.

To analysis the efficiency of the compensation network, the efficiency of a basic L-section stage in Fig. 9 is investigated. As the loss of the compensation focus mainly on the dissipative resistance of the inductors, the loss on capacitance is neglected. The natural logarithm of the L-section stage efficiency can be deduced from (8) as

$$-\log_e \eta = \frac{1}{Q_L}|Q_u - Q_0| \tag{9}$$

And the Q_u, Q_d subject to

$$\frac{1+Q_u^{\,2}}{1+Q_d^{\,2}} = \frac{R_d}{R_u} \tag{10}$$

where R_d, R_u is the real part of Z_d, Z_u in Fig. 9.

1) Single-stage compensation optimization

In a single-stage compensated CPT system, the primary compensation network and the secondary compensation network are both L-section stages. Take the double-side LC topology shown in Fig.4 as an example. The overall efficiency can be deduced as

$$-\log_e \eta = -\log_e(\eta_1\eta_2) = \frac{1}{Q_L}|Q_{u1}| + \frac{1}{Q_L}|Q_{u2}| \tag{11}$$

The efficiency optimization problem can be expressed as

$$\begin{aligned} \min\ & \frac{1}{Q_L}|Q_{u1}| + \frac{1}{Q_L}|Q_{u2}| \\ s.t.\ & \frac{1+Q_{u1}^{\,2}}{1+Q_{d1}^{\,2}} = \frac{R_{d1}}{R_{u1}} \\ & \frac{1+Q_{u2}^{\,2}}{1+Q_{d2}^{\,2}} = \frac{R_{d2}}{R_{u2}} \\ & R_{d1} = R_{d2} = R_m \\ & Q_{d1} - Q_{d2} = \frac{|X_c|}{R_m} \end{aligned} \tag{12}$$

It should be noticed that R_{u1} is the load resistance and R_{u2} is the resistance at the inverter output.

If we assume that R_{u1} equals to R_{u2}, which means the output

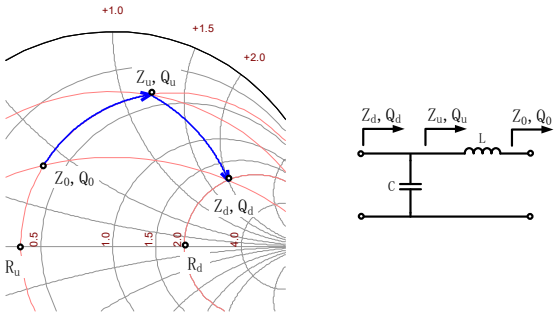


Fig. 9. A L-section stage model.

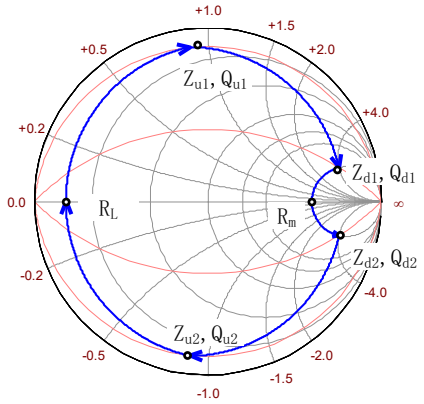


Fig. 10. Efficiency optimization of symmetric single-stage L-section compensation.

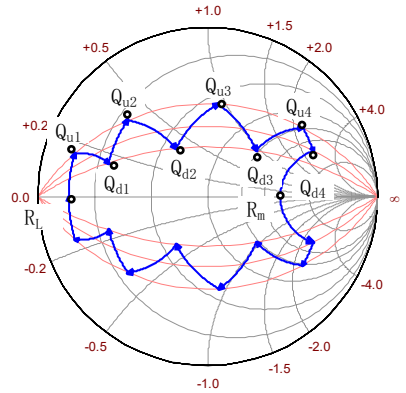


Fig. 11. Efficiency optimization of symmetric multi-stage L-section compensation.

voltage and input voltage will be roughly the same. Then the optimal solution should be vertically symmetric, that is

$$\begin{cases} R_{u1} = R_{u2} = R_L \\ |Q_{u1}| = |Q_{u2}| = Q_u \\ |Q_{d1}| = |Q_{d2}| = Q_d \end{cases} \tag{13}$$

Put (13) into (12), the optimization problem is simplified as

$$\begin{aligned} &\min \ \frac{2}{\mathrm{Q_L}}|Q_u| \\ &s.t. \ \frac{1+Q_u^{\ 2}}{1+Q_d^{\ 2}} = \frac{R_m}{R_L} \\ &Q_d = \frac{|X_c|}{2R_m} \end{aligned} \tag{14}$$

The minimum is reached when

$$\begin{cases} R_m = \dfrac{|X_c|}{2} \\ Q_d = 1 \\ Q_u = \sqrt{\dfrac{|X_c|}{R_L} - 1} \end{cases} \tag{15}$$

And the highest efficiency is

$$-\log_e \eta_{\max} = \frac{2}{Q_L}\sqrt{\frac{|X_c|}{R_L} - 1} \tag{16}$$

So, the maximal efficiency of symmetric CPT system of single-stage compensation is achieved when the arc of C_s is symmetric according to the real axis, starting from the circle of Q=1.0 and ending at the circle of Q=-1.0. And the path of the optimal design on Smith chart is in Fig. 10.

2) Multi-stage compensation optimization

Multi-stage compensation is often used to provide a large voltage or current ratio. For example, the LCLC topology in [7] is a two-stage compensation.

Similar to the analysis of symmetric single-stage compensation, the optimization problem of symmetric multi-stage compensation can be expressed as

$$\begin{aligned} &\min \ \frac{2}{\mathrm{Q_L}}\left(\sum_{\mathrm{i=1}}^{\mathrm{n}} Q_{ui} - \sum_{i=1}^{n-1} Q_{di}\right) \\ &s.t. \ \prod_{\mathrm{i=0}}^{\mathrm{n}} \frac{1+Q_{ui}^{\ 2}}{1+Q_{di}^{\ 2}} = \frac{R_m}{R_L} \\ &Q_{dn} = \frac{|X_c|}{2R_m} \end{aligned} \tag{17}$$

The method of Lagrange multiplier is used here.

$$\begin{aligned} L = &\sum_{\mathrm{i=1}}^{\mathrm{n}} \mathrm{Q_{ui}} - \sum_{i=1}^{n-1} Q_{di} \\ &+ \lambda_1 \left(\prod_{\mathrm{i=0}}^{\mathrm{n}} \frac{1+Q_{ui}^{\ 2}}{1+Q_{di}^{\ 2}} - \frac{R_m}{R_L}\right) + \lambda_2 \left(Q_{dn} - \frac{|X_c|}{2R_m}\right) \end{aligned} \tag{18}$$

The following partial differential equations need to be solved

$$\begin{aligned} 0 &= \frac{\partial L}{\partial \lambda_1} = \prod_{\mathrm{i=0}}^{\mathrm{n}} \frac{1+Q_{ui}^{\ 2}}{1+Q_{di}^{\ 2}} - \frac{R_m}{R_L} \\ 0 &= \frac{\partial L}{\partial \lambda_2} = Q_{dn} - \frac{|X_c|}{2R_m} \\ 0 &= \frac{\partial L}{\partial R_m} = \lambda_1 \left(-\frac{1}{R_L}\right) + \lambda_2 \left(\frac{|X_c|}{2R_m^{\ 2}}\right) \\ 0 &= \frac{\partial L}{\partial Q_{ui}} = 1 + \lambda_1 \left(\frac{2Q_{ui}}{1+Q_{ui}^{\ 2}} \prod_{\mathrm{i=0}}^{\mathrm{n}} \frac{1+Q_{ui}^{\ 2}}{1+Q_{di}^{\ 2}}\right) \\ 0 &= \frac{\partial L}{\partial Q_{di}} = -1 + \lambda_1 \left(-\frac{2Q_{di}}{1+Q_{di}^{\ 2}} \prod_{\mathrm{i=0}}^{\mathrm{n}} \frac{1+Q_{ui}^{\ 2}}{1+Q_{di}^{\ 2}}\right) \\ 0 &= \frac{\partial L}{\partial Q_{dn}} = \lambda_1 \left(-\frac{2Q_{dn}}{1+Q_{dn}^{\ 2}} \prod_{\mathrm{i=0}}^{\mathrm{n}} \frac{1+Q_{ui}^{\ 2}}{1+Q_{di}^{\ 2}}\right) + \lambda_2 \end{aligned} \tag{19}$$

The optimal efficiency is reached, when

$$\begin{cases} R_m = \dfrac{|X_c|}{2} \\ Q_{dn} = 1 \\ Q_{d1} = \ldots = Q_{d(n-1)} = Q_d \\ Q_{u1} = \ldots = Q_{un} = Q_u \\ Q_u = Q_d^{\ -1} \end{cases} \tag{20}$$

The highest efficiency is

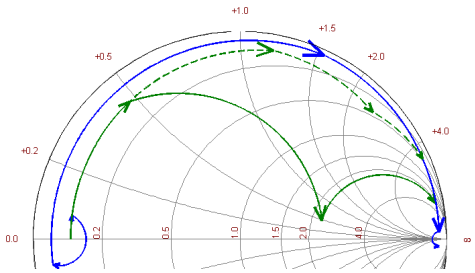


Fig. 12. Efficiency perfection of design in [11].

$$-\log_e \eta_{\max} = \frac{2}{Q_L}(n\mathrm{Q_u} - (n-1)\mathrm{Q_u}^{-1}) \qquad (21)$$

where Q_u satisfied with

$$Q_u^{2(n-1)} + Q_u^{2n} = \frac{|X_c|}{R_L} \qquad (22)$$

The smith chart of a symmetric CPT system with optimized multi-stage compensation is shown in Fig. 11.

It should be noticed that when $|X_c|=2R_L$, according to (22), we have $Q_u = 1$, and the optimal solution of the multi-stage compensation degrades to single-stage compensation. Besides, when $Q_u < 1$, the L-section stages will have negative inductance and capacitance. So in order to get valid solution, the following

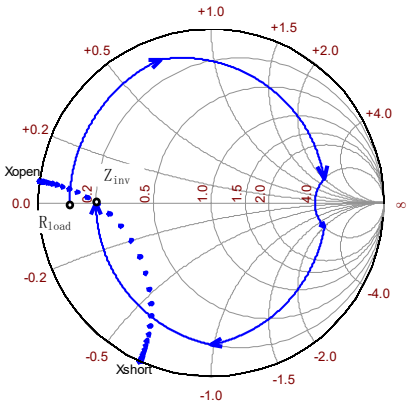


Fig. 13. Input impedance locus.

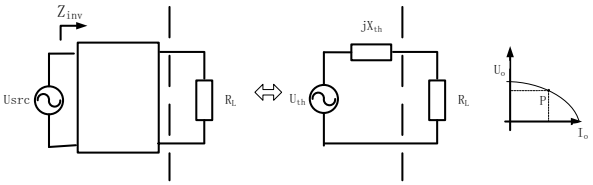


Fig. 14. Output Thevenin equivalent circuit.

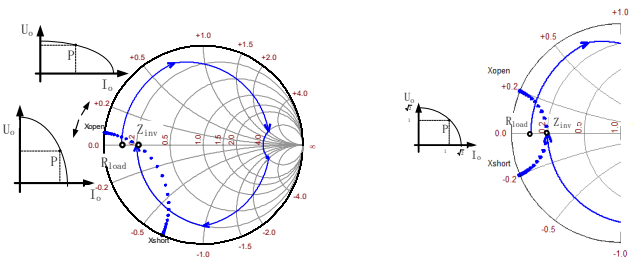
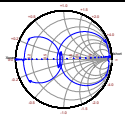
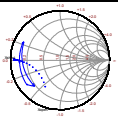
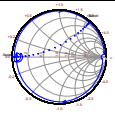
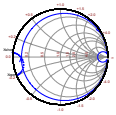


Fig. 15. Output impedance characteristic.

TABLE V
CHARACTERISTICS COMPARISON OF THE CPT SYSTEMS

	 [7]LCLC-Compensate	 [19]1kW 13.56M
Output	Current source	Close to constant voltage
Input	Resistive	Capacitive with no load
	 [11]LCLC Four-plate	 [15]Optimal eff (type 1)
Output	Current source	More likely constant voltage
Input	Slightly inductive	Capacitive with no load

equation must be satisfied.

$$\frac{|X_c|}{R_L} = Q_u^{2(n-1)} + Q_u^{2n} > 2 \qquad (23)$$

However, as the reactance of the coupling capacitance in large-gap CPT system is usually quite small, that is $|X_c| >> R_L$, (23) holds true in most of the cases.

3) *Conclusion*

As a conclusion, based on the graphic analysis of its path on Smith chart, in order to improve the efficiency of [11], whose path on Smith chart is shown as the blue line in Fig. 12, its two stage LC compensation parameters need to be adjusted. When optimized to max efficiency, its path is shown as the solid green line. If its current source output characteristics must be remained, the optimized result is the dotted green line Fig. 12.

V. OUTPUT & INPUT CHARACTERISTICS

Usually, a current source or voltage source output is desired in design of CPT system. And an inductive input characteristic is required for the ZVS operating of the full-bridge inverter.

A. Graphic features

To analyze the input characteristics, a locus of input impedance points covering a range of load resistance is investigated. Based on the characteristics of linear fractional transformation, we could know that as the load resistor vary from infinity to zero, the input locus is a circle as the dotted line shown in Fig. 13. Respectively, the point X_{open}, Z_{inv} and X_{short} correspond to load resistance of infinity, R_L and zero. From Fig. 13, we could tell that the demo system is inductive under light load and is capacitive under heavy load.

To analyze the output characteristics, let a constant voltage source connected to the input port, the source and the lossless network can be replaced at output terminal by an equivalent voltage source in series connection with an equivalent reactance based on The venin theory, which is shown in Fig. 14. So the output characteristic of CPT system with a voltage source input is the equivalent to a voltage source in series with an internal reactance, whose U-I curve is an ellipse arc.

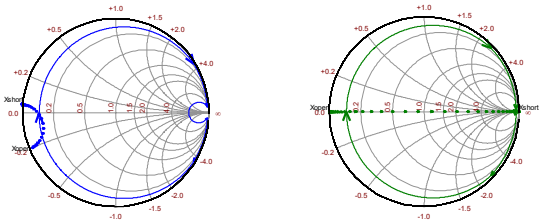


Fig. 16. Characteristic adjustment of design in [15].

Graphically, the output characteristic can also be analyzed through the input impedance locus. If the point X_{open} is close to the point of (-1+0j), the output characteristic will be close to a current source. Otherwise, it will be close to a voltage source, which is shown in Fig. 15.

Here, we take the systems of [7][11][15][19] as an example. Their paths on Smith chart and the input and output characteristics are listed in Table VIII.

The LCLC-compensate [7] is designed to be an ideal current source output. Its input impedance locus is a horizontal line on the real axis with X_{open} at (-1+0j).

In the LCLC Four-plate design [11], the inductor on the secondary side was made larger than design to meet the ZVS condition of the inverter. The impedance locus stays above the real axis in Smith chart, which means that the input is inductive for any resistive load at the output.

The efficiency optimal design of [15] is not designed with any desired output characteristics. From its input impedance locus we could see that X_{short} is slightly closer to (-1+0j) than X_{open}, so the output voltage varies less than the output current. And because X_{open} is capacitive, it will be dangerous on no-load condition when ZVS full-bridge topo is used in inverter.

The input characteristic of [19] is close to [15], but its X_{short} is closer to (-1+0j) than [15], so the output is closer to constant voltage.

B. Graphical design of desired characteristic

Here, we investigate the path of system in [15] whose path is shown in blue path in Fig. 16. In order to achieve a current source output characteristic, the point of X_{open} need to be at point (-1+0j). That means, the clockwise arcs need to be lengthen and the counter-clockwise arcs need to be shorten. And the path of the adjusted system will be similar to the path of [9], which is shown in green path in Fig. 16. It should be mentioned that the adjustment above results in a reduction of efficiency.

VI. Graphical Design Guidelines

As a summary, the large-gap CPT system designed in Table I can be classified according to their different design objectives, which is shown in Fig. 17. From Fig. 17, we could see that most of the current designs are designed under one major design objective. Sometime, compromised design and trade-offs or numerical optimization under certain constrains are conducted to design the system with multiple objectives.

In this case, the path of the CPT system on Smith tool which can simultaneously outline the major design objectives can be of great help.

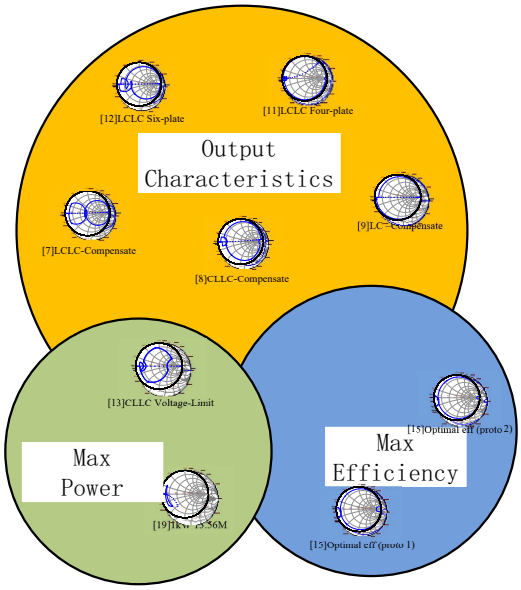


Fig. 17. Classification of the CPT system design in Table I

A. Design guidelines

Based on the analysis in the previous chapters, several guidelines in design of the compensation of large-gap CPT systems can be extracted.

1) Keep the path away from the bounding of unit circle. Path near the bounding represents high reactive energy which leads to high loss.
2) Try to keep the arc of C_s symmetric according to the real axis. This can help to balance the voltages on the coupling plates on both sides and transfer a larger power under voltage limitation.
3) To optimize the compensation efficiency, the max Q of the path should be limited and the Q of each stage in the compensation has to be balanced.
4) To maximize power transferred through coupling, the arc of C_s should be symmetric according to the real axis, starting from the circle of Q=1.0 and ending at the circle of Q=-1.0.
5) To achieve a certain output or input characteristic, the locus of the input impedance should satisfied the corresponding constrain. And the locus can be adjusted through the adjustment to the overall length of the clockwise arcs and the counter-clockwise arcs.

B. Graphical design example

In order to demonstrate usage of the graphical design method following the guidelines above, the LCLC compensation network of the CPT system designed in [11] will be corrected to achieve a higher efficiency. The circuit model of the original design in [11] is shown in Fig. 18.

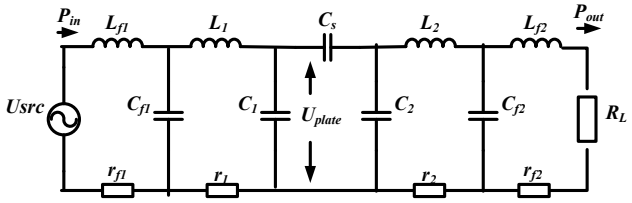


Fig. 18. LCLC compensation topology in [11].

In order to analyze the loss on the compensation network, we assume that the quality factor of the inductors is Q_L=600. Thus, the dissipation resistance r_{L1}, r_{L2}, r_{Lf1}, r_{Lf2} can be derived. The simulation parameters are listed in topology original circuit parameters are listed in Table VI. The path of the original design on smith chart is shown in Fig. 19.

TABLE VI
PARAMETERS OF THE ORIGINAL DESIGN IN [11]

Parameter	Value	Parameter	Value
f	1MHz	L_{f1}, L_{f2}	2.9μH
U_{src}	265V	r_{f1}, r_{f2}	30mΩ
R_L	26.78Ω	C_{f1}, C_{f2}	8.73nF
C_s	11.3pF	L_1, L_2	69.4μH
Q_L	600	r_1, r_2	727mΩ
		C_1, C_2	369.6pF

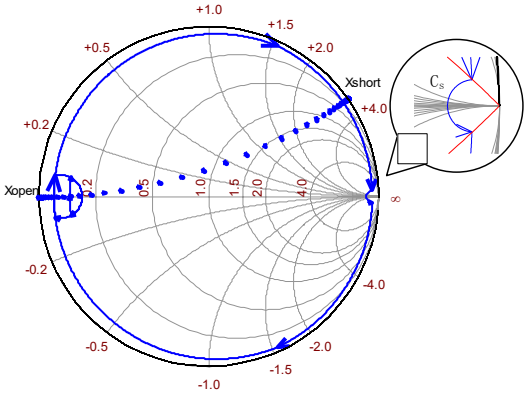


Fig. 19. Path of the original design on Smith chart.

From Fig. 19, the following graphical features can be noticed

1) The path of Cs is symmetric according to the real axis. And the end points is on the circle of Q=±1.0. So the system power under certain voltage limit on the coupling plates is already close to the maximum.
2) The path of the system is close to the unit circle. So the loss on the compensation network is relatively high.
3) The point of X_{open} on the locus of the input impedance is at (-1+0j). So the system has a current source output characteristics.

Based on the analysis above, we could correct the path on smith chart to improve the efficiency of the system. In detail, it takes two steps as follow.

1) Based on the feature of the multi-stage compensation network in chapter IV. We could design a path with optimized efficiency, which is shown as the solid green line in Fig. 20.
2) Adjust the path, moves the point of X_{open} to (-1+0j). So the system will have a current source output characteristics. The result is shown as the dashed green line in Fig.20.

The complete path of the two steps is shown in Fig.21. The finally corrected design has the following features.

1) The path of Cs roughly remains unmoved, which means the voltage on the coupling plates will be roughly the same as the original design.
2) The path of the system is on the inner side of the original path, which means the system efficiency will be improved.
3) The point of X_{open} is adjusted back to (-1+0j). So the system will still have a current source output characteristics.

After the graphical correction, we could convert the path on Smith chart back to the circuit parameters, which is shown in Table VII.

To verify the result of graphical correction, the original design and the corrected design is simulated with PSIM. Under designed load of 26.78Ω, the input power, output power, system efficiency and the voltage on coupling plates are shown in Table VIII. And the output characteristics of the two designs are compared in Fig. 22.

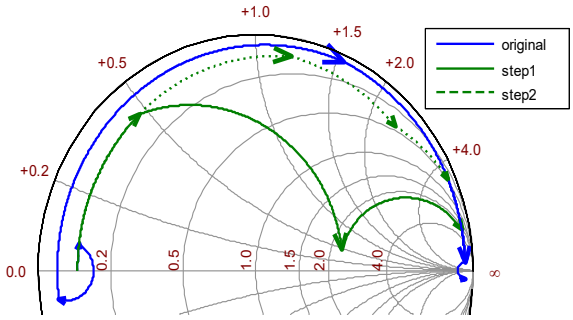
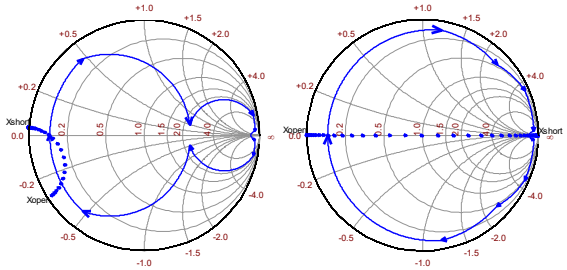


Fig. 20. Steps of the path correction on Smith chart.



(a) step 1 (b) step 2

Fig. 21. The correction result of each step.

TABLE VII
PARAMETERS OF THE CORRECTED DESIGN

Parameter	Value	Parameter	Value
f	1MHz	L_{f1}, L_{f2}	50.8μH
U_{src}	265V	r_{f1}, r_{f2}	532mΩ
R_L	26.78Ω	C_{f1}, C_{f2}	259.2pF
C_s	11.3pF	L_1, L_2	97.75μH
Q_L	600	r_1, r_2	1024mΩ
		C_1, C_2	113.2pF

TABLE VIII
SIMULATION RESULTS

Original		Corrected	
P_{in}	2.14kW	P_{in}	2.13kW
P_{out}	1.89kW	P_{out}	2.00kW
η	88.3%	η	95.8%
U_{plate}	5.424kV	U_{plate}	5.423kV
$\frac{U_{plate}^2}{P_{out}}$	3.788 15.6 kV²/kW	$\frac{U_{plate}^2}{P_{out}}$	5.272 14.7 kV²/kW

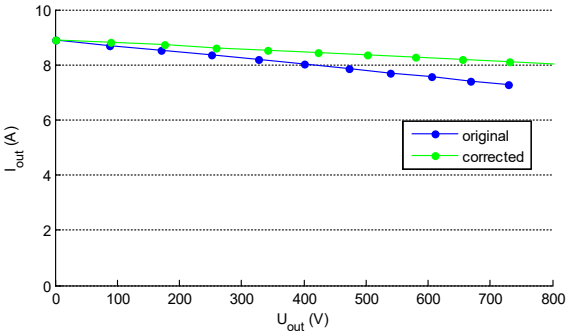


Fig. 22. Comparison of the output characteristics.

It is shown that the voltage on the coupling plates is 5.423kV which remains the same as the original design, the efficiency of the system is improved from 88.3% to 95.8% and the output remains a current source characteristics.

VII. CONCLUSION

This paper proposes a graphical method on analysis of the compensation designs for large-gap CPT systems. Based on the investigation in the graphical features of the path of CPT system on Smith chart, the voltage on capacitive plates, the loss on compensation network and the output characteristic and input characteristic can be read from the graph. Based on the graphical features, several design guidelines are proposed for qualitatively evaluate the compensation design of CPT systems. Finally, graphical design is used to improve the efficiency of a LCLC compensation design. It shows that the graphical analysis method and the design guidelines proposed can be used in multi-objective design for CPT systems. Future work will take robustness into consideration, such as the performance under gap variation, to make more practical designs.

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