Multi-Dimensional Models of SiC Power MOSFET for Accurately Predicting the Characteristics

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(Invited)

***Abstract*—The paper presents a compact simulation program with integrated circuit emphasis (SPICE) model for a 1200V/19A Silicon Carbide power metallic oxide semiconductor field effect transistor (MOSFET). Based on an equivalent circuit topology, the model completely describes the static and dynamic device characteristics which include the MOSFET channel current, the nonlinear junction capacitance and the switching behavior. Especially the parasitic elements effect is also considered and studied during the modeling, testing and simulation. The model parameters are extracted based on the experimental measurement data. For convenience, the model is implemented by Verilog-A description language and embedded in the simulation software – Advanced Design System (ADS). The validity and accuracy of the model are validated by the double pulse test under inductor load. The Verification result shows that the modeling job is correct and available for prediction of the switching performance under different conditions.**

***Index Terms*—Dynamic, model, SiC MOSFET, verilog-A.**

I. Introduction

DURING the last decade, the research on Silicon Carbide (SiC) power MOSFET had been greatly developed because of superior material features comparing to silicon, such as the wider band gap, higher breakdown voltage, higher switching speed and lower switching losses[1]-[2].

To fully study the SiC power MOSFET, it is truly critical to model the elements. Several published literatures show different compact model. Jun Wang et al. proposed a PSpice model of DiMOSFET with the nonlinear junction capacitor expressed by a sub-circuit of SIEMENS which made it more complex with various elements[3]. Mudholkar et al. presented a model with precise simulation of the MOSFET channel current[4]. Additionally, the literature proposed by Xueyu Hou[5] and Kainan Chen et al. paid attention to the body diode and drain to source capacitor respectively[6]. With these early and partly research, the model of the SiC power MOSFET is basically accomplished. However, most of the models are validated by switching behavior without the package and circuit parasitic elements. The purpose of this paper is to model the SiC power MOSFET with static and dynamic characteristics and verify it under the double pulse test with consideration of the stray inductor.

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II. Guidelines For Manuscript Preparation

In this paper, the exploration of modeling the SiC power MOSFET with hardware describe language Verilog-A[7] and Advanced Design System (ADS) is presented. The three major steps of modeling are determining the circuit, modeling the static characteristics and dynamic characteristics.

A. Structure and Circuit

Fig 1. Shows the typical structure of the SiC power MOSFET with the topology circuit. For the prototypes structure of the MOSFET, the model has three external nodes for gate, drain and source. The main MOSFET channel current is given by the current source I_{total}. And the series resistors are combined in one as R_{total} shows in the structure. The MOSFET used in this paper is C2M0120160D released by CREE INC.

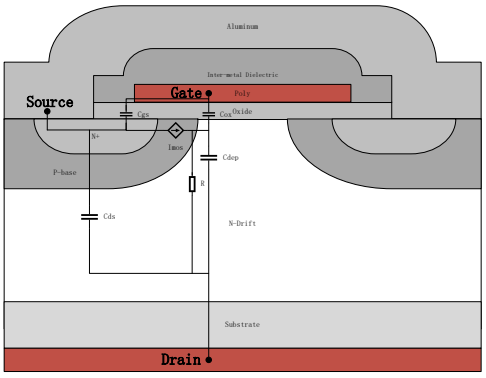


Fig. 1. Cell structure for a 1200V/19A SiC power MOSFET with compact model.

B. MOSFET Channel Current

For SiC power MOSFET the main conduction current is the current flow through the channel under the gate to the N-drift region as shown in the structure. The expression for channel current is based on McNutt's model [8]. Comparing SiC power MOSFET with Si MOSFET, the transition from linear region to saturation region needs for more attention. Thus, the channel current I_{total} has been divided into low-current-mode and high-current-mode with the values of V_{gs} and V_{ds} as separate conditions. The expression of the I_{total} is given as:

$$I_{total} = I_{low} + I_{high} \tag{1}$$

$$I_{low} = \begin{cases} K_{fl}K_f\left[(V_{gs}-V_{thl})V_{ds} - \frac{P_{vf}^{y-1}V_{ds}^{y}(V_{gs}-V_{thl})^{2-y}}{y}\right], & V_{ds} < \frac{V_{gs}-V_{thl}}{P_{vf}} \\ \frac{K_{fl}(V_{gs}-V_{thl})^2}{2}, & V_{ds} \geq \frac{V_{gs}-V_{thl}}{P_{vf}} \end{cases} \tag{2}$$

$$I_{high} = \begin{cases} (1-K_{fl})K_f\left[(V_{gs}-V_{thh})V_{ds} - \frac{P_{vf}^{y-1}V_{ds}^{y}(V_{gs}-V_{thh})^{2-y}}{y}\right], & V_{ds} < \frac{V_{gs}-V_{thh}}{P_{vf}} \\ \frac{(1-K_{fl})(V_{gs}-V_{thh})^2}{2}, & V_{ds} \geq \frac{V_{gs}-V_{thh}}{P_{vf}} \end{cases} \tag{3}$$

$$y = \frac{K_f}{K_f - \frac{P_{vf}}{2}} \tag{4}$$

K_{fl} and K_f are the transconductance factors and the P_{vf} is the pinch-off voltage factor which defines the slope of the transition region. In order to distinguish the linear and saturation region, two different threshold voltages, V_{thl} and V_{thh} are applied in the equations. The parameter extraction of the static characteristics is based on the transfer and output characteristics as Fig.2 and Fig.3 and the parameters are listed in Table. I.

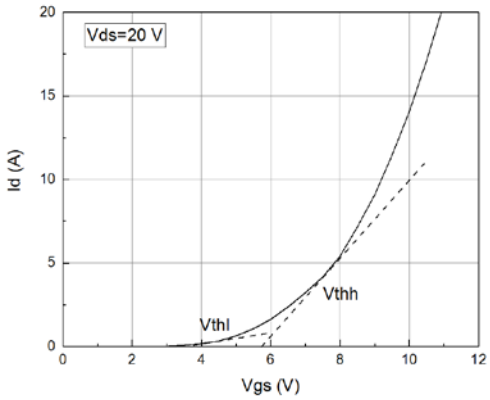


Fig. 2. Extraction procedure for transfer characteristic parameter.

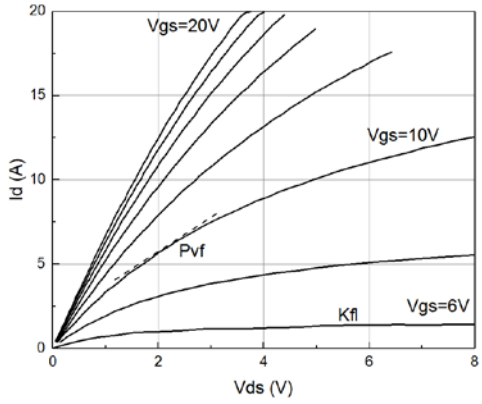


Fig. 3. Extraction procedure for output characteristics parameters.

TABLE I
UNITS FOR MAGNETIC PROPERTIES

Symbol	Description	Value
K_{fl}	Low current factor	0.35
K_f	Transconductance factor	1.5
P_{vf}	Pinch-off voltage	0.8
V_{thl}	Low current threshold voltage (V)	4.5
V_{thh}	High current threshold voltage (V)	5.4
C_{gs}	Gate to source capacitance (pF)	500
C_{ox}	Oxide capacitance (pF)	247
ε_{semi}	Semiconductor dielectric constant (F/cm)	85e-12
K	Boltzmann's constant (J/K)	1.3e-23
T	Chip surface temperature (K)	300
q	Fundamental electronic charge (C)	1.6e-19

The description of the output characteristics is based on the parameters above and the simulation result is shown in Fig.4. As for V_{gs} from 10V to 20V in the operation range, the simulation result fits the measurement curve perfectly.

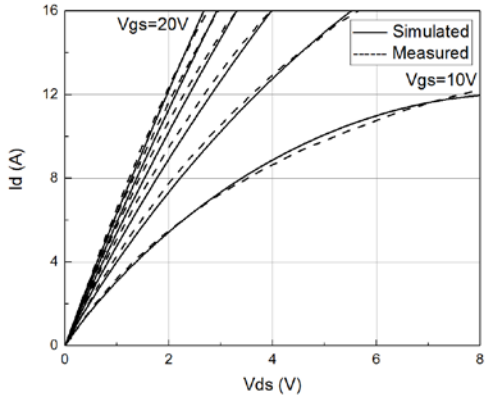


Fig. 4. Measured (dash) and simulated (solid) output characteristics at room temperature.

C. Nonlinear Junction Capacitance

As for a unipolar device, the separate capacitors connect to each other play the important roles during the dynamic behavior. Thus, the accurate extraction of the capacitances is important. Using the typical measurement, the values for input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer capacitance C_{rss} with different drain bias voltage are extracted. They are related to three major internal capacitances between nodes: gate to source capacitance C_{gs}, gate to drain capacitance C_{gd} and drain to source capacitance C_{ds}.

$$C_{iss} = C_{gs} + C_{gd} \tag{5}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{6}$$

$$C_{rss} = C_{gd} \tag{7}$$

C_{gs} is capacitance due to the overlap of polysilicon gate with the channel region and the source metallization over the isolation oxide. However, it is not a strong function of applied voltage and considered as a constant capacitance which equals the C_{iss} bias at zero drain voltage.

The others like the build-in potential V_{bi} and typical equations of parallel board capacitor C_{ds} are given as follows and the parameters are listed in Table. I.

$$V_{bi} = \frac{kT}{q} ln \frac{1*10^3 N_b}{ni^2} \quad (8)$$

$$W_{ds} = \sqrt{\frac{2\varepsilon_{semi}(V_{ds}+V_{bi})}{qN_b}} \quad (9)$$

$$C_{ds} = \frac{A_{ds}\varepsilon_{semi}}{W_{ds}} \quad (10)$$

The particular and major capacitor is C_{gd} which is formed by a combination of C_{ox} and the depletion region capacitor C_{dep} between gate oxide region and N-drift region. C_{ox} equals the maximum of the C_{rss} and is extracted from the measurement directly. And the C_{gd} is calculated as given:

$$W_{dep} = \sqrt{\frac{2\varepsilon_{semi}V_{ds}}{qN_b}} \quad (11)$$

$$C_{dep} = \frac{A_{dep}\varepsilon_{semi}}{W_{dep}} \quad (12)$$

$$C_{gd} = \begin{cases} C_{ox} & , V_{ds} \le V_{gs} \\ C_{ox}C_{dep} \Big/ C_{ox} + C_{dep} & , V_{ds} > V_{gs} \end{cases} \quad (13)$$

Fig.5. shows the curve comparison between simulation and the measurement. It is shown clearly that all of the simulation result of the capacitance fit the test result excellent in entire voltage range.

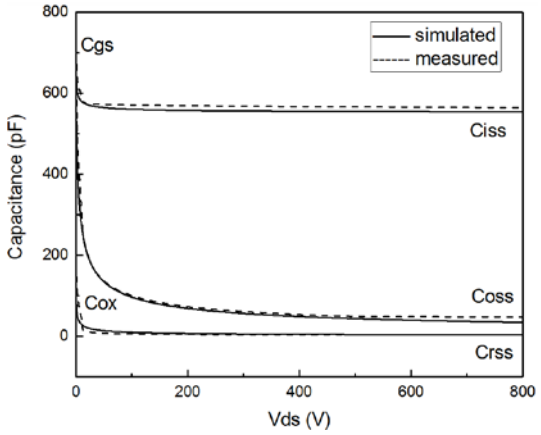


Fig. 5. Measured (solid) and simulated (dash) terminal capacitances.

III. Model Validation and Application

With the parameter extracted from the static characteristics, the model for the SiC power MOSFET has been settled. Then, the dynamic experimental measurement is applied to verify the entire accuracy of the model.

A. Double Pulse Test

Fig.6 shows the standard circuit for double pulse test and the parasitic elements from the package and measure circuit have also been considered in the simulation. And the test curve is shown in Fig.7.

As shown in Fig.6, the elements for double pulse test by TESEC 3430 are listed include the DC power apply $V_{cc} = 600\,V$, the test load inductor $L_{load} = 500\,\mu H$, the input gate step voltage source V_{gs} from -5V to 20V, the external gate resistor $R_g = 10\,\Omega$, the freewheeling diode (FWD) and the D.U.T. model. The values of the elements above are determined by the measurement conditions. And the L_g、R_g、L_d、R_d、L_s、R_s and L_{stray} refer to the parasitic elements in the package and circuit which are critical to the dynamic simulation as these influence the oscillations[9].

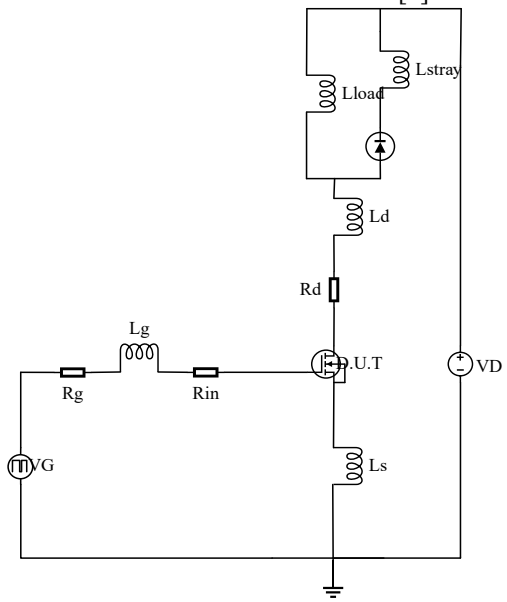


Fig. 6. Schematic circuit diagram for a inductor load test circuit with parasitic elements.

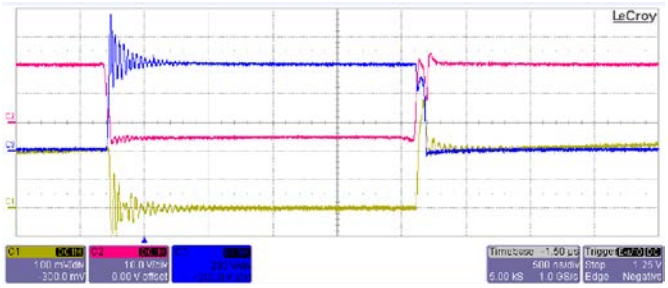
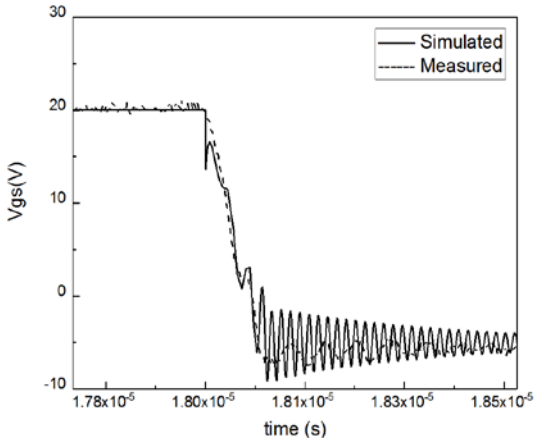


Fig. 7. Waveforms for double pulse test with inductor load.

B. Simulation Result

The dynamic validation of the model is verified by comparison between simulation and measurement at room temperature. As for the transient behavior, it is divided into two parts as turn-on and turn-off process.

As for the turn off process, the critical spike for V_{ds} shows the stress for the MOSFET breakdown voltage. And consideration of the oscillation of V_{gs}, it is necessary to operate the minimum voltage much lower than the threshold voltage to avoid switching on by mistake.



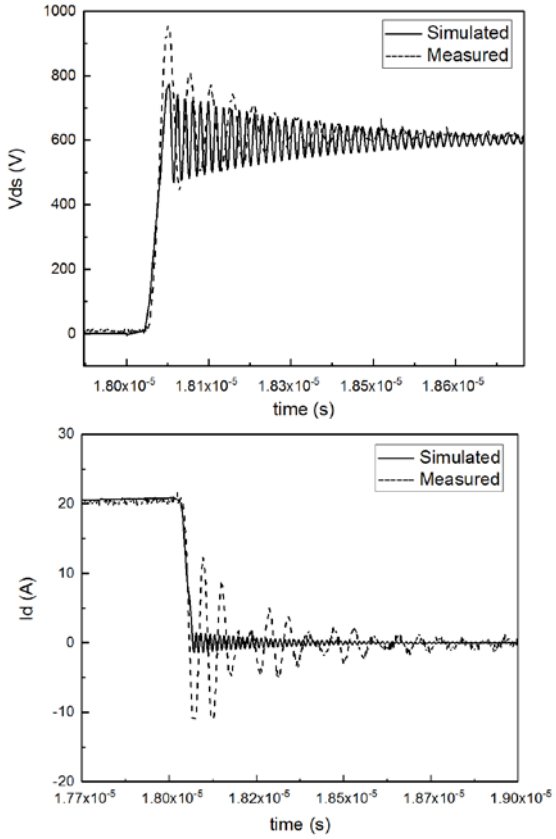
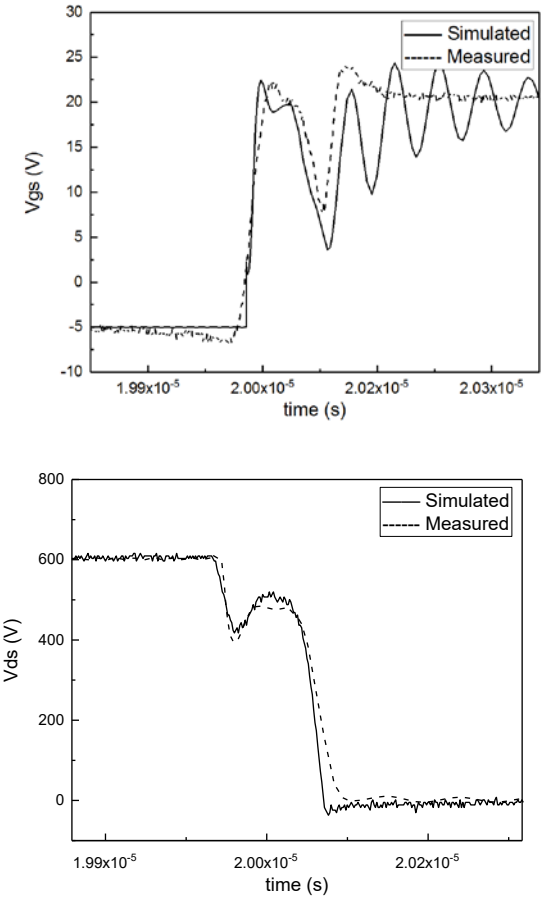


Fig. 8. Simulation and measurement of the turn off process of V_{gs}、V_{ds}、I_d.



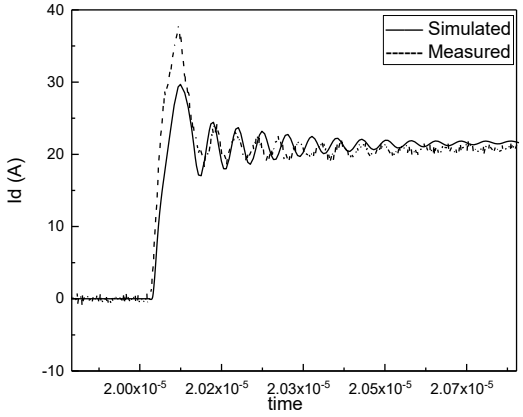


Fig. 9. Simulation and measurement of the turn on process of V_{gs}、V_{ds}、I_d.

The simulation result of the turn on transient shows the overshoot of the drain current is twice as the standard which is caused by the current stored in the diode and parasitic inductors.

C. *Model Application*

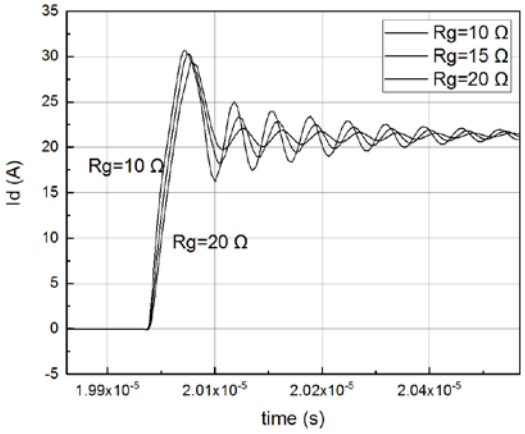
The major purpose for modeling the power MOSFET with electric elements is researching the MOSFET in the convenient simulation platform because not all of the circuit conditions are suitable and safe for measurement. In order to avoid the damage to the MOSFET because of the oscillations occurred by the undesirable circuit, the prediction of the dynamic behavior should be done before test. With the model has been verified above, the influences of the circuit parasitic elements are given as Fig.10 and Fig.11.

In the double pulse test, the gate-to-source voltage V_{gs} and drain-to-source voltage V_{ds} are calculated as given:

$$V_{gs} = V_G - I_g\left(R_g + R_{in}\right) - L_g\frac{dI_g}{dt} - L_s\frac{d(I_g+I_d)}{dt} \tag{14}$$

$$V_{ds} = V_D - V_{diode} - I_d R_d - L_d\frac{dI_d}{dt} - L_s\frac{d(I_g+I_d)}{dt} \tag{15}$$

The priority of the parasitic inductors and resistors are different, though the equations include every element in the circuit loops. With the measurement experience, the most important parts include the gate load resistor R_g and the parasitic inductor L_{stray}.



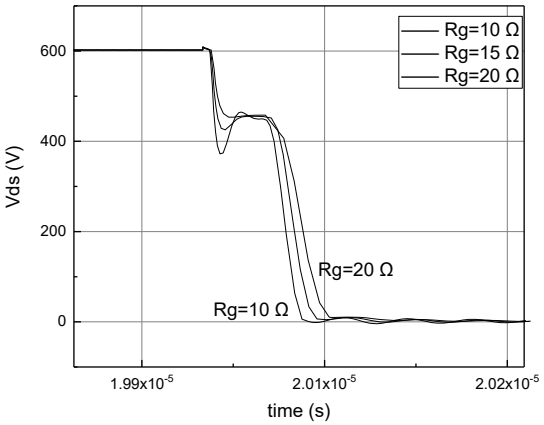


Fig. 10. Simulation result of turn off process under different R_g.

As shown in Fig.10, the lower R_g do increase the switching speed. However, it increases the spike of I_d and V_{ds} in trade.

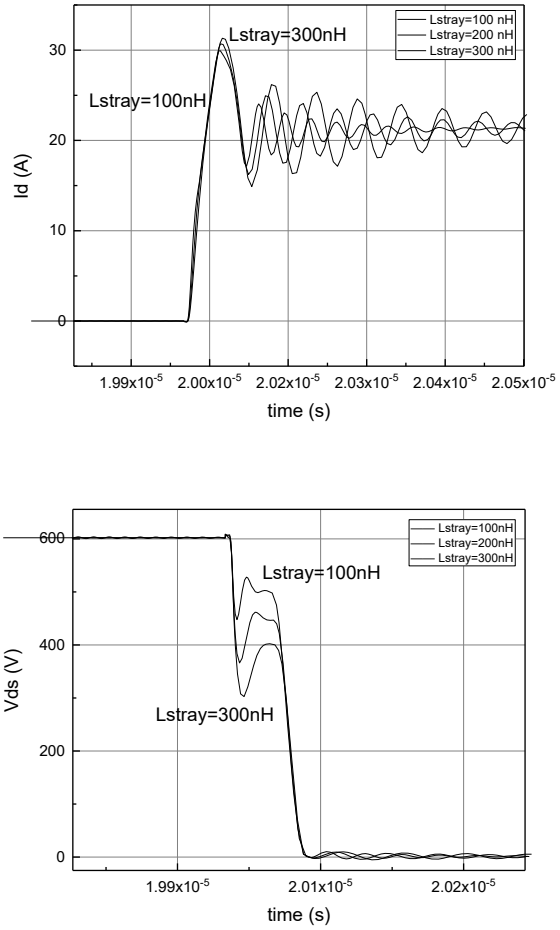


Fig. 11. Simulation result of turn off process under different L_{stray}.

With the increase of the L_{stray}, only the oscillations by the end of I_d and the medium of V_{ds} have changed. However, the switching time does not change as expected.

According to the simulation result above, the parasitic elements in the circuit influence the switching performance. Thus, the attention should be paid on the values of the inductors in realistic experiment to avoid undesirable performance.

IV. Conclusion

The model of 1200V/19A Silicon Carbide power MOSFET has been presented in this paper. Because of the accurate data captured by measurement, the dynamic behavior validation is much more convinced. And the comparison shows great agreement between the simulation and the measurement results in both static characteristics and switching behavior. The prediction of the gate resistance and parasitic inductor influence on the switching speed and the overshoot of the current and voltage is shown directly. All of the measurements are under room temperature and the effect of thermal heating should be considered in the further research. Generally speaking, the modeling of the SiC power MOSFET and prediction of the behavior under different conditions are meaningful in the development of the SiC power MOSFET.

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