Technical Approaches Towards Ultra-High Power Density SiC Inverter in Electric Vehicle Applications

Xuhui Wen, *Senior Member*, *IEEE*, Tao Fan, *Senior Member*, *IEEE*
Puqi Ning, *Senior Member*, *IEEE*, and Qing Guo, *Senior Member*, *IEEE*
(Invited)

***Abstract*—Along with the rapid growth in electric vehicle (EV) market, higher power density and more efficient motor drive inverters are required. It is well known that silicon carbide (SiC) has advantages of high temperature, high efficiency and high switching frequency. It is believed that the appropriate utilization of these merits can pave the way to ultra-high power density inverters. This paper presents issues about SiC chip's current-carrying capability enhancement which is crucial for a compact inverter of tens and hundreds of kilowatts. Technical approaches towards ultra-high power density EV inverter including SiC module packaging, dc-link capacitor function analysis and system level integration are discussed. Different PWM algorithms which may improve efficiency and help to reduce the inverter volume are also studied.**

***Index Terms*—DC-link capacitor, electrical motor, electric vehicle, inverter, silicon carbide.**

I. INTRODUCTION

TO enable the rapidly emerging and imminent energy economy, electric vehicles (EV) are needed at low cost. According to France's famous consulting firm Yole, the annual production and sales of world's electric vehicle will reach 20 million by 2020 [1]. Therefore, dramatic improvements in EV motor drive inverter have to be achieved in terms of energy efficiency, cost, and reliability.

In the late 90s, GM launched its electric car EV1, Toyota demonstrated its hybrid car Prius, and Daimler Chrysler launched fuel cell EV NuCar. In the past two decades, medium power rating inverters for EV drive are dominated by the mature and well established silicon IGBT technology. AC asynchronous motors and permanent magnet motors competed with other types of motors, and finally shares the EV marketplace[2]. With state-of-the-art IGBT module packaging and inverter system level integration technology, Toyota Corporation in Japan produced a high power density inverter with 17.2 kW/L (at 65° C). In ref [3], a research level prototype reached 36 kW/L, which is extremely high for a Si based inverter.

In recent years, the silicon carbide (SiC) power semiconductor has emerged as an attractive alternative that pushes the limitations of band-gap width, breakdown voltage, saturation drift rate and thermal conductivity of silicon (Si) devices [2][4]. Research organizations and EV vendors have successfully developed a high temperature and high frequency SiC inverter, which demonstrated advantages as high power density, high efficiency and low cost. In ref [5], Fuji Electric developed 10kW air-cooled SiC EV inverter with 190°C chip junction temperature, 50 kHz switching frequency, and about 40kW / L power density. In ref [6], Toyota increased vehicle fuel efficiency by 5%, which proofed their leadership in EV area with novel SiC device and its application. In the past 5 years, there are closed to 6700 patents related to inverters for electric vehicles. Among them, about 37.1% patents presented the utilization of SiC devices with its high temperature and high frequency advantages. SiC technology will assure future compact power electronics systems which target deployment in the emerging energy economy.

This article provides a status report on SiC devices and presents the key challenges that must be addressed when developing future compact SiC converter at high junction temperature. Issues regarding high temperature low parasitic parameters module packaging, dc-link capacitor functional analysis with associated PWM algorithm and system-level inverter integration methods have been discussed. In conclusion, with continually improved SiC chip technology, high frequency/ high temperature passive component and inverter technology, SiC devices are thus expected to drive the growth of EV motor drive inverter as they are the key components of a power system.

II. CHALLENGES OF ENHANCING SIC CHIP'S HIGH TEMPERATURE CURRENT-CARRYING CAPABILITY

SiC has a 3-time-higher band-gap, 3-time-higher thermal conductivity, 10-time-higher critical breakdown electric field than Si [7], as shown in Table I. Therefore, SiC power devices

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Xuhui Wen, Tao Fan and Puqi Ning are with Key Laboratory of Power Electronics and Electric Drive, Institute of Electrical Engineering, Chinese Academy of Sciences; Collaborative Innovation Center of Electric Vehicles in Beijing. (e-mai: wxh@mail.iee.ac.cn; fantao@mail.iee.ac.cn; npq@mail.iee.ac.cn).

Qing Guo is with Zhejiang University, National Engineering Center for Applied Power Electronics).

can work under high temperature and high frequency conditions with high efficiency. The above characteristics have built a solid foundation for the realization of high-power-density automotive motor drive inverter.

TABLE I
CHARACTERISTICS ANALYSIS OF SI, GAN AND SIC

	Si	SiC	Analysis
Bandgap（eV）	1.12	3.2	Wider band-gap can improve the working temperature, thus simplifying the cooling system.
Critical breakdown electric field（MV/cm,x10^5）	3	30	Higher critical breakdown electric field leads to lower power losses, thus improving the inverter's efficiency.
Electron/hole mobility（cm^2/V.s）	1450/450	950/115	Higher mobility and saturation velocity can reduce switching loss and improve switching frequency.
Electron saturation velocity（cm/s, x10^7）	1	2	
Thermal conductivity（W/cm.k）	1.3	5	Higher thermal conductivity is beneficial for inverter heat dissipation.

The voltage levels of electric vehicle motor drive systems span from 48V to 900V with power ratings of 3~300kW. The motor drive inverter utilizes SiC MOSFETs with body-diode or with anti-parallel SBD as switches, as shown in Fig. 1. Until 2016, the highest current-carrying capability of 1200V SiC MOSFET commercial chip is 63A at 25ºC and reduces to 46A at 100°C. Besides, SiC MOSFET R_{dson} at 200ºC increases rapidly to 2.5 times higher than its room temperature value, leading to sharp loss growth [8].

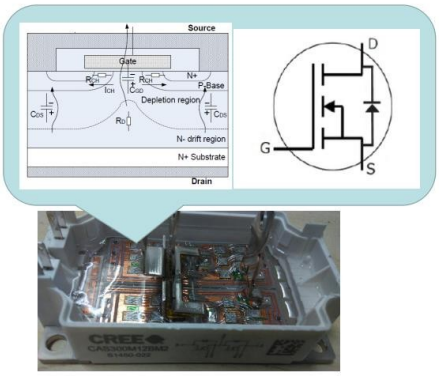

Fig. 1. Diagram of SiC MOSFET chip and module.

Compared with SiC IGBT modules for EV motor drive inverter, current SiC MOSFET chips show obvious problems such as low single-chip current-carrying capability and its deterioration at higher temperature. For example, in a compact battery powered electric car, the 77kVA motor drive inverter adopts a 650V/450A IGBT module comprised of 3 150A IGBTs and 3 anti-parallel diodes. If SiC chips were utilized, at least 9 MOSFETs and 9 diodes were needed to be parallel-connected, thus greatly increasing the module complexity and stray inductance. The increased module stray inductance will result in high electric stress of SiC MOSFETs, switching oscillations and EMI problems. Therefore, improving the high temperature current-carrying capability of SiC chips, especially SiC MOSFETs, is of paramount importance.

The carrier transport mechanisms and behaviors under high temperature and high electric field of SiC chips determine SiC chip's high temperature electrical characteristics and reliability:

1) Carrier scattering at high temperature deceases its mobility, and leading to higher SiC chip resistance and lower current-carrying capability. When the temperature increases, this scattering mechanisms will lead to mobility lowering, mobility saturation in MOS channel at high electric field etc., hindering the current-carrying capability improvement and increase on resistance of SiC chips. One research has reported that, the carrier mobility of MOSFETs annealed in phosphorous ambient is 130 $cm^2/V{\cdot}s$ at room temperature. It will reduce to 80 $cm^2/V{\cdot}s$ at 150ºC and 50 $cm^2/V{\cdot}s$ at 300ºC. New MOS structures are needed to improve the carrier mobility at high temperature.
2) Under high temperature and high electric field, more electron-hole pairs in PN junction barrier depletion region are produced resulting in larger leakage current. This leakage current at high temperature may be reduced by suppressing the parasitic parameters of the device.
3) For SiC MSOFET, the carrier capture and release at high temperature gate interface will affect the device stability and reliability. At high temperature, the electrons are accelerated to create large number of holes. These holes may be captured by oxide layer. This increases the electric field strength at local oxide defects and leads to tunneling current, which may cause oxide layer breakdown. It is necessary to develop a new gate dielectric layer growth method to improve the reliability of SiC MOS oxide layer.

Therefore, theories about the carrier transport mechanisms at high temperature, MOS gate dielectric interface degradation mechanisms and device failure mechanisms of SiC material are essential to SiC device design and fabrication. Under the theoretical guidance, the processes such as trench structure, p+ implantation, wafer thinning and low-interface high-reliability gate dielectric growth is the key for improving high temperature current-carrying capability of SiC chips.

III. TECHNICAL APPROACHES TOWARDS ULTRA-HIGH POWER DENSITY ON-BOARD INVERTER

When vehicles vary from mild-hybrid cars to full electric buses, the power rating of motor drive system increase from 3 ~ 5kW to 200 ~ 300kW, and the battery voltage raises from VIV to around 540V. If classified by power and voltage, EV motor drive inverter is a typical medium/low power, low voltage converter system.

In the past 20 years or so, current-type inverter [9], Z-source converter [10] and multi-phase inverter [11] were invented and researched in the development of EV. However, the main topology of EV motor drive power stage is still taken by two-level three-phase voltage source inverter (VSI). In the recent research and development of VSI for EV application, in order to increase the power density, the utilizations of new

components, including double sided cooling IGBT and different kinds of capacitors, and multi-physical field analysis based system level integration method have been studied. In SiC inverter research, the core is how to use the promising benefits of SiC device.

A. High temperature approach focusing on developing power module planar packaging technology

Since SiC chip cannot be directly applied to the motor drive inverter, the module packaging technology plays an important role to take the full advantages of SiC chips.

The first problem about SiC packaging is high temperature. High temperature causes module thermal stress and thus packaging material degradation. Although the loss of a SiC chip is smaller than that of a Si chip, heat flux density becomes larger because of reduction of the chip area. For example, the maximum current of Cree's 1200V/40mΩ MOSFET chip can reach 63A, and the operative area is 0.183cm^2. When working at 50 kHz and 50A$_{rms}$, the heat flux of the SiC chip reaches 623 W/cm^2, which is 2.5 times of state-of-the-art IGBT chip [13]. Therefore, high temperature packaging material and method are needed.

In power module, SiC or Si chips are soldered or sintered on the direct bonded copper (DBC) substrate. The melting points of conventional solder alloys used in Si IGBT packaging, such as SAC305 etc, are commonly below 300 °C, and the operation temperature cannot exceed 175°C. High temperature solders, such as Au80Sn20 and Au88Ge12 are too hard and do not meet the requirement of high temperature operation (200°C above). Although the micrometer scale silver paste can be sintered at 250°C and the operation temperature is over 500°C, the sintering process requires a pressure over 15 MPa, which may easily damage SiC chips [13]. In ref [14], Nano silver paste can achieve a pressure free low temperature sintering process, and also allows over 600°C operation temperature. After the sintering, the formed micro-pore structure can absorb thermal stresses, which meet the high temperature and high reliability requirements of SiC chip.

With high temperature cycling and large temperature excursion, especially during transient switching conditions when the semiconductor chips are commonly lack of thermal balance, the packaging materials will degrade fast. Under these stresses, layer in the module will form pre-defects, the residual stress will be intensified, and potting materials evaporate fast, all of those lead to module failure. Therefore, the calculation methods for electrical unbalance and temperature unbalance between key packaging components need to be carefully studied. For SiC power module designs, it is extremely important to learn the fatigue failure and acceleration mode of packaging material under electrical stress, thermal stress and mechanical stress.

The second problem is how to insure fast switching and high frequency operations. The switching speed of SiC MOSFET is 3 to 5 times higher than Si IGBT while its frequency can reach up to 1 MHz for a power converter. Fast switching and high frequency require extreme low stray impedance in SiC module. Package parasitic reduction methods such as copper ribbon bonding and optimal chip distribution method need to be studied. As the converter switching frequency is increased for module miniaturization, electromagnetic interference will become another important issue to tackle. In the end, the current rating of a single SiC MOSFET die is 1/4 ~ 1/6 of Si IGBT. It means that a 450A SiC MOSFET module need to parallel 9 dies, while a 450 Si IGBT module only needs to parallel 3 IGBT dies. As a result, a large number of dies raises many difficulties in module layout design.

In the new generation of automotive modules, planar package is preferred, because that the planar package can reduce stray inductance by 70%. With double-sided cooling structure, the planar package can also reduce the thermal resistance by 35% [15]. Most of planar package researches are focused on the top die surface interconnection and the package layout design. Among the top die surface interconnection methods, the main approaches include, molybdenum buffer layer inter-connection [16], soldering bump implantation over passivation layer [17], embedded direct bonded copper (DBC) structure[18], multi-layer sputtering and curing method [19]. For double-sided structure design, scholars are exploring genetic algorithm based multi-objective optimization methods. The novel optimization method can break through the design limits of experience based engineering method, and it can prove high temperature and high frequency advantages of SiC chips [20].

In summary, the planar package and Nano silver paste interconnect technology will assist SiC from a promising future technology to a potent alternative to Si in high reliability, high temperature and high frequency applications.

B. High switching frequency approach focusing on raising dc-link capacitor's current-carrying capability and inverter switch frequency

The power circuit of electric vehicles can be described by a battery pack, a two-level three-phase inverter and a motor. The battery pack is equivalent to an ideal voltage source in series with a small resistance of hundreds of nano-ohms, a very large capacitor of several hundreds of Farads paralleled with its internal resistance. A dc-link capacitor is required to supply ripple current to switches and balance DC voltage fluctuation, as Fig. 2 shows.

Usually in IGBT inverter, the dc-link capacitor accounts for 35% of the total volume and 25% of the total mass. It is well known that the capacitor in EMI filter can be reduced by increasing frequency. Therefore, the beginning idea of utilizing the high frequency capability of SiC device starts with the dc-link capacitor function research in order to increase power density of SiC inverter.

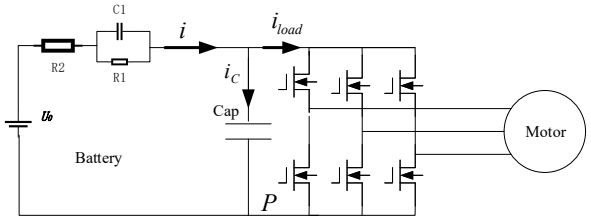

Fig. 2. Schematic Diagram of EV's power circuit.

Contrast to the capacitor in EMI filter, the first role of the dc-link capacitor in the EV power circuit is to supply ripple current to the inverter switches during switching period. By using the law of power equilibrium, under the condition of balanced sinusoidal three phase AC current, Kolar [21] derived the relationship between the DC and AC currents on both sides of switches during one single switching period as equation (1) and (2) shown. From the equations, it is clear that the inverter ripple current I_{rms} and the capacitor ripple current $I_{C,rms}$ can be described by the motor phase current $I_{\varphi,rms}$, power factor $cos\varphi$ and the voltage modulation index M . Because the impedance of dc-link capacitor branch is much lower than that of the battery branch, the high order harmonics of I_{rms} has to be extracted from the dc-link capacitor.

$$I_{rms} = I_{\varphi,rms}\sqrt{\frac{2\sqrt{3}}{\pi}M(\frac{1}{4}+\cos^2\varphi)} \tag{1}$$

$$I_{C,rms} = I_{\varphi,rms}\sqrt{2M\left[\frac{\sqrt{3}}{4\pi}+\cos^2\varphi(\frac{\sqrt{3}}{\pi}-\frac{9M}{16})\right]} \tag{2}$$

The second role of the dc-link capacitor in the circuit is to smooth the dc voltage fluctuations caused by the load P_{max}. This function is expressed by the right term of Eq. (3):

$$P_{\max} = i_c\left(U_{dc0}-\frac{1}{2Cf_s}i_c\right) = i_c\left(U_{dc0}-\frac{1}{2}\Delta U\right) \tag{3}$$

Where, U_{dc0} is the steady state of DC voltage, f_s is the switching frequency, C and i_c are the capacitance and the ripple current of the capacitor respectively. From equation (3), it is apparent:

1) The low impedance dc-link capacitor is a better source for the inverter ripple current, especially for its current harmonics near the switching frequency. It is even more important for EV, since tens of kilohertz and hundred amperes of ripple current will inevitably reduce battery lifetime.
2) The dc-link voltage fluctuation ΔU caused by load needs to be suppressed, which is expressed as:

$$\Delta U = \frac{i_c\Delta t}{C} = \frac{i_c}{Cf_s} \tag{4}$$

For a three phase AC motor, Eq. (4) can be rewritten as:

$$C(n,T) = \frac{\sqrt{3}\left(1-M(n,T)\right)M(n,T)I_{\varphi,rms}(n,T)}{2\Delta Uf_s} \tag{5}$$

M and $I_{\varphi,rms}$ are functions of motor speed n and torque T.

The capacitance of the dc-link capacitor is determined by the modulation index as well as the power factor [24], can be obtained from (5). From Eq. (4) and (5), assuming the dc-link capacitor supplies adequate inverter ripple current, it is known that the increase of switch frequency in SiC inverter is much more appropriate than the way of the capacitor value augment, because of the SiC device's high frequency advantage.

Take a 77KVA inverter for example again. Its voltage is 320V, peak current is 282A. In a Si based IGBT motor drive inverter, 10 kHz switch frequency is commonly used. After evaluating the capacitor ripple current-carrying capability and the DC voltage fluctuation limit (5% ~ 10%), the dc-link film capacitor used in domestic inverter is usually 600 off, which is 500 mL based on the state-of-art film capacitor technology (1.2μF/mL).

TABLE II
IMPACT OF SWITCH FREQUENCY TO CAPACITOR

	Si_inverter	SiC_ inverter
$U_0(V)$	320	320
$I_{rms}(A)$	200	200
$I_{peak}(A)$	282.8	282.8
$C(\mu F)$	600	120
$V^*_C(mL)$	500	100
$f_s(kHz)$	10	50
$\Delta U(V)$	23.57	23.57
$\Delta U/U_0(\%)$	7.36	7.36

But, in a SiC inverter, assuming the switch frequency being arisen by 5 times, the capacitance can be decreased to 120μF and volume to 100mL. The same DC voltage fluctuation limitation is also guaranteed, as Table II shown. It should be pointed out that this 120 μF film capacitor has to provide the ripple current of 50 kHz and its harmonics corresponding to 282.8 A! Therefore, research objectives of the film capacitor in SiC inverter should include not only capacitance per volume (C/mL) but also the current-carrying capability at high temperature. The latter one is even more important.

The research of film capacitors used in automobile spans from material level to component level. At the material level, GE has developed polyetherimide (PEI) film materials, allowing the ambient temperature up to 180℃, 4% higher than that of the polypropylene (PP) film which is most widely used currently. In terms of component level, the SBE from US has reduced the equivalent thermal resistance of the capacitor through the integration of capacitor and its cooling components. The capacitor rated ripple current is directly enhanced [22].

In conclusion, making full use of high frequency feature of SiC devices is embodied in developing the film capacitor with high current-carrying ability at high temperature and large C/mL value. Based on the planar SiC packaging technology and high density film capacitor technology, the multi-physical field analysis methods and system-level power electronics integration technology can make SiC inverter even better:

1) DC bus bar optimization: the DC bus bar connects capacitor cells and SiC power module together. The electromagnetic field analysis such as ANSYS Q3D can help to optimize the bus bar current distribution and reduce the inverter loop stray inductance which may result in reduction of SiC power rating and increase of inverter power density.
2) Inverter layout optimization: after the losses and heat distribution in the inverter are obtained by circuit calculation and 3D thermal simulation, the high efficient heat transmission methods including phase transformation and specific heat by-pass design can help to decrease the thermal resistance between each heat source and heat sink [23]. Sometime the heat insulation technology need be included to reduce the thermal coupling between the heat

source and heat sensitive components in SiC inverters.

C. High efficient approach focusing on SiC inverter PWM algorithms

The losses of an EV electrical drive system are divided into the motor losses and the inverter losses. The loss arising from the power switch is the dominant part in an inverter. The innovative pulse modulation methods are effective to increase SiC inverter efficiency and thus power density.

a) High efficiency pulse width modulation algorithm for SiC inverter

The power loss of the SiC devices can be expressed by (6) assuming the loss from the FRDs is ignored. $E_{on}(k)$ and $E_{off}(k)$ are the power loss from the *kth* power switch in an inverter. $N_s(k)$ is the number of switching on-and-off in a unit time, D_s is a constant. For the three-phase half bridge, the upper limit of k is 6.

$$P_s = D_s \sum_{k=1}^{6} \left(E_{on}(k) + E_{off}(k) \right) N_s(k) \tag{6}$$

In the EV's AC motor drive application, the space vector modulation method is commonly used. Optimization of the operation sequence for the resulting space vector is an efficient way to decrease k in (6). The so-called 7-segment method is drawn on the left of Fig 3. In this pattern, the numbers of switching is 6 in a carrier wave period. If combining the zero vectors in the middle and the ends together, namely, the zero vector 111 is not used, a different switching pattern is obtained, which is shown on the right in Fig 3. It can be seen that, the numbers of switching are reduced by 1/3.

A dilemma is found when reviewing section III-B: on the one hand, the switching frequency rise can decrease the required dc-link capacitance and thus the inverter volume. On the other hand, the switching frequency decrease can rise the inverter efficiency and cut down the loss which is also helpful for higher power density. Therefore, an optimal switching frequency is needed to balance the efficiency and the power density of an inverter.

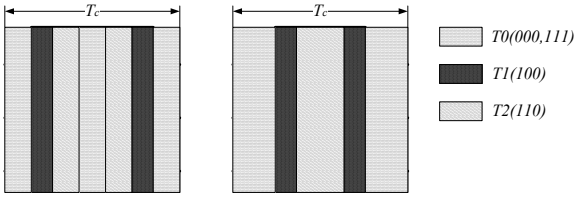

Fig. 3. Different switching pattern

b) Pulse width modulation algorithm considering working condition

According to the discussion in the section III-B, it is known that the capacitance is inversely proportional to the switching frequency for a certain DC voltage fluctuation limit. Choosing a typical 60kW electrical motor as an example, the relationship corresponding to (5) is given in Fig 4 (the switching frequency is kept constant). It is shown that the required capacitance is changing with the working condition within a predefined voltage fluctuation limit (ΔU). The maximum capacitance is found at the mid-range speed with peak torque (1800rpm@190Nm). Therefore, this maximum capacitance is used in inverter design. From another point of view, because the voltage fluctuation is well below the voltage fluctuation limit ΔU at other working points rather than the above-mentioned one, lower switching frequencies are thus allowed to obtain reduced switching losses in those working conditions.

The relationship behind the Fig 4 means that, the minimal allowed switching frequency with a defined ΔU is a function of both speed and torque when capacitor is chosen, and this makes PWM algorithm more effective but rather complex in implementation. A simplified method is given in Fig 5. It is essentially an improved subsection synchronization modulation. The Upper Limit in Fig 5 is calculated by the maximum allowed switching losses, and the Lower Limit is a function of speed, and can be calculated by (7). C_0 is the maximum capacitance, and f_{sw0} is the frequency corresponding to C_0 and ΔU. *M*ax $(C(n, T))$ means the maximum capacitance for a given speed with all torque.

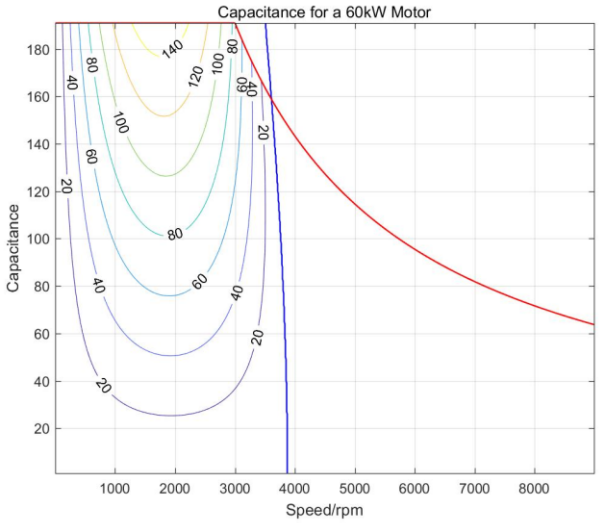

Fig. 4. the relationship between the capacitance and the working condition.

Using this approach, an optimized switching frequency can be obtained. As a result, the switching loss is reduced and the power density of the inverter is increased.

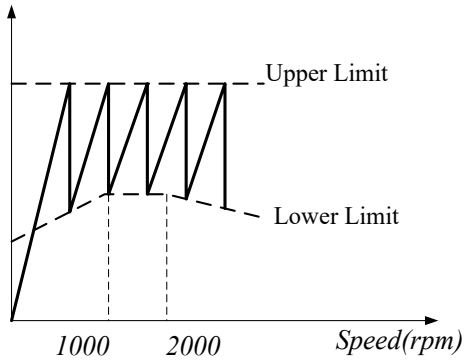

Fig. 5. Improved subsection synchronization modulation.

$$f_{\text{lower\_limit}}(n) = \frac{C_0}{\text{Max}\left(C(n,T)\right)} f_{sw0} \tag{7}$$

IV. CONCLUSION

Because of its excellent characteristics in high temperature, high efficiency and high switching frequency, SiC device has been used to develop ultra-high power density inverter for EV applications. Issues including SiC chip's current-carrying capability and reliability at high temperature are addressed in this paper. Several technology approaches towards ultra-high power density SiC inverter are discussed. Among all these technology approaches, development of power module planar packaging and double side cooling technology is mainly aiming at the purpose of high temperature; raising dc-link capacitor current-carrying capability and inverter switching frequency is mainly aiming at the purpose of high frequency; while SiC inverter control strategies are mainly aiming at the purpose of high efficiency. With all the innovations in active and passive components, the inverter system level integration technologies, especially the thermal management technology, will largely increase the power density of inverters.

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Xuhui Wen (D'93) was born in Chengdu, China. She received her B.S, M.S and PhD degree in electrical engineering from Tsinghua University in 1984, 1989, 1993 respectively. She is full professor in Institute of Electrical Engineering, Chinese Academy of Sciences. Dr. Wen has been involved in high power density electrical drive and generation especially for electric vehicle application for more than 20 years.

Tao Fan (D'09) received his B.S degree in electrical engineering from Tsinghua University in 2004, and his M.S and PhD degrees in electrical engineering from the Graduate University of the Chinese Academy of Sciences in 2006 and 2009 respectively. He became an IEEE member in 2012. From 2009 to 2011 he worked as an assistant professor in the Institute of Electrical Engineering of Chinese Academy of Sciences, and became an associate professor in 2011. His research direction are design and analysis of special electrical machine and large power generation and high power electrical propulsion system.

Puqi Ning (D'10) was born in Tianjin, China. She received the Ph.D. degree in electrical engineering from Virginia Tech, Blacksburg, US in 2010.

He is full professor in Institute of Electrical Engineering, Chinese Academy of Sciences. Dr. Ning has been involved in high temperature packaging and high density converter design for more than 10 years.

Qing Guo was born in Tai'an, China. He received the Ph.D. degree in Microelectronics from Zhejiang University, Hangzhou, China.

He is associate professor in electric engineering, Zhejiang University. Dr. Guo has been involved in power devices for about 10 years