Precise Electro-thermal Power Loss Model of a Three-level ANPC Inverter with Hybrid Si/SiC Switches

*Dereje Woldegiorgis** *and H. Alan Mantooth*

(Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701, USA)

Abstract: Hybrid Si/SiC switches constituting a parallel connection of a lower current rated SiC MOSFET and a higher current rated Si IGBT are becoming very attractive solution for designing high frequency and high-power density power electronic converters. Due to the complementary nature of Si IGBT devices (smaller inverter cost and smaller conduction loss) and SiC devices (smaller switching loss and higher junction temperature capability), these novel switch device configurations enable a good tradeoff between cost and efficiency for high power converter applications. One such recent application of hybrid Si/SiC switches for efficiency-cost optimization is an Si/SiC hybrid switch based ANPC inverter proposed in Ref. [30]. In Ref. [30] the topology structure, modulation strategy and the efficiency-cost benefits of the proposed ANPC inverter is presented. In this paper a precise electro-thermal power loss model for this ANPC inverter topology will be presented based on the modulation strategy of the inverter and the operating characteristics of the Si/SiC hybrid switches. The power loss model development takes into account how the current sharing between the two internal devices of the Si/SiC hybrid switches and their corresponding gate control method affects their power loss. A brief introduction to the topology structure and operation principle of the Si/SiC based ANPC inverter is first highlighted to provide context for readers and then a detailed description of the proposed electro-thermal power loss model is presented. The precision of the electro-thermal power loss model introduced in this paper is then validated using experimentally measured energy loss, device temperature and inverter efficiency data.

Keywords: Cost reduction, power loss model, efficiency improvement, ANPC inverter

1 Introduction

With the increase in population and industrialization, the annual world energy consumption is also increasing constantly. The increasing energy consumption however brought a significant challenge to the world. The annual CO_2 emission from industries and manufacturing plants into the atmospheric air is parallelly increasing. This causes depletion of the ozone layer which protects the earth from harmful ultraviolent radiations [1]. With the depleted ozone layer, the increased concentration of CO_2 and other greenhouse gases such as methane and Nitrous Oxide increases the absorption and emission of radiant energy from the environment causing an annual mean temperature increase to the world, a phenomenon called global warming. This phenomenon causes changing weather patterns such as extreme weather events, melting icebergs and sea level rise affecting the polar and marine ecosystems [2]. To mitigate the harmful effect of CO_2 and other greenhouse gases, several actions have been taken by many stakeholders to reduce the emission of these harmful gases into the atmosphere. Following the Paris climate agreement in 2015, several nations pledged to reduce their CO_2 emission into the atmosphere by fostering the use of alternative clean and renewable energy resources such as Photovoltaic (PV), wind, geothermal and hydropower through government incentives such as investment tax credits and lower tax rates [3-4]. This brought a new era in the energy sector where renewable energy resources are increasingly being used.

Nowadays, the renewable energy market is promptly

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* Corresponding Author, E-mail: dlwoldeg@uark.edu

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growing especially in wind and solar energy. Not only the annual energy harvest from these renewable energy resources is exponentially increasing but also the generation capacity of these energy generation sites is increasing – Megawatt scale wind energy and PV energy generation sites are now common [5]. Parallel to the rapid growth of the renewable energy market, there is also a rapid growth in the electrification of the transportation sector [6]. Starting from passenger commuter vehicles to heavy duty trucks and big aircrafts, the electric transportation sector is now generating multi-billion dollars revenue annually. However, this rapid increase in renewable energy and electric transportation market poses a major challenge in the design of energy conversion systems. There is a parallelly increasing demand for increasing the conversion efficiency as well as the power density of energy conversion systems in renewable generation and electric transportation to maintain the economic viability of these market sectors [7-8].

The advent of wide bandgap power devices such as Gallium Nitride (GaN) and Silicon Carbide (SiC) is one of the enablers of designing a high efficiency and high power density energy conversion systems for renewable energy conversion and motor drive applications. These switching devices have higher switching frequency operation capability (enabling significant passive component size reduction and hence increasing converter power density), lower switching energy loss (enabling higher converter efficiency) and higher thermal conductivity and junction temperature capability (reduced thermal management requirement) compared to Silicon (Si) IGBT devices [9-11]. However, the widescale deployment of Silicon Carbide (SiC) devices is currently hampered by their relatively higher cost compared to their silicon counterpart. In order to mitigate this problem and fully utilize the benefits of SiC devices, a novel switching device configuration termed as hybrid Si/SiC switch by many researchers is recently proposed by connecting Si IGBT device in parallel with SiC MOSFET device [12-15]. This switching device configuration provides a good tradeoff between cost and efficiency due to the complementary nature of Si IGBT and SiC MOSFET devices. The Si IGBT enables lower cost and lower conduction power loss [16] while the SiC MOSFET enables lower switching power loss and higher switching frequency operation capability in hybrid Si/SiC switch configuration [9, 11]. In addition, several gate control methods for the internal Si/SiC hybrid switches [17-20] have also been proposed to optimize the Si/SiC hybrid switches loss and increase the efficiency of converters utilizing these switching device configurations.

Another enabler for the design of high power density and high efficiency energy conversion systems is the use of multilevel converter topologies especially three-level voltage source converter topologies. These converter topologies offer lower dv/dt (lower electromagnetic interference), lower semiconductor device blocking voltage requirement and lower output filter requirement compared to two-level voltage source converter topologies [21-23]. Therefore, they provide higher efficiency and higher power density especially for energy conversion applications with high voltage and current requirement compared to two-level converter topologies. Amongst the multilevel converter topologies, the three-level converter topologies especially the three-level active neutral point clamp (ANPC) converter topology is usually preferred for different applications because of its benefits over other three-level inverter topologies. Some of these benefits are the semiconductor devices have balanced power loss and it can handle high output voltage levels with semiconductor devices of low voltage rating - the semiconductor device blocking voltage requirement is 50 percent of the magnitude of the dc voltage [24-25]. In addition, ANPC inverter has flexible control and modulation capabilities because of its redundant neutral switching states. Different modulation and control strategies can be developed to serve various objectives such as power loss minimization (efficiency improvement), reducing common mode voltage [26-28].

An ANPC converter constituting Si/SiC hybrid devices, as shown in Fig. 1, is recently introduced in Refs. [29-31]. This converter adopts the control method introduced in Ref. [32]. This control method is especially attractive due to its features of lower number of switches operating at carrier frequency (high frequency switches). Therefore, it offers a good

tradeoff between cost and efficiency. In order to enable a good cost-efficiency tradeoff, the high frequency switches are implemented with Si/SiC hybrid devices while Si IGBTs are chosen for the low frequency switches. Due to their lower cost and lower conduction loss especially for high load current, Si IGBTs in particular are very ideal choice for low frequency switches [16]. SiC MOSFETs would have been the best choice for the high frequency switches to achieve high converter efficiency and high power density [9-11] but their high cost is a major issue. Therefore, a hybrid Si/SiC switch comprising of SiC MOSFET of smaller current rating and Si IGBT of larger current rating is chosen for the high frequency switches to minimize the converter cost and power loss. However, the efficiency-cost tradeoff and reliability of the converter depends on the static and dynamic current sharing among the internal devices of the Si/SiC hybrid switches——the SiC MOSFET and the Si IGBT [15, 33]. Smaller current rated SiC MOSFET would reduce the cost of the inverter however the current rating of the SiC MOSFET is too small, the transient peak temperature of the SiC MOSFET may go beyond the maximum allowable junction temperature of the SiC MOSFET. This may in turn cause reliability issue such as thermal run away. Therefore, to forecast the SiC MOSFET's peak junction temperature at the initial stage of design a precise electro-thermal power loss model of the inverter accounting the operating characteristics of the Si/SiC hybrid switches is required.

There has been significant research already to develop an analytical electro-thermal power loss model for an active neutral point clamped converter. These electro-thermal power loss models can be broadly classified as methods based on device datasheet extracted parameters [34-36] and methods based on analytical expression of the converter operation and modulation strategy [37-38]. In the first method the electro-thermal power loss model is based on the high-level parameters of semiconductor devices such as on-state resistance and input/output capacitance which are the determining factors of semiconductor devices power losses. These parameters are extracted from the device datasheets using linear approximation. The second method is based on the operation and control of the inverter. An analytical expression of the power loss of the inverter is derived based on the modulation strategy and the inverter operating conditions such as power factor and modulation index. However, none of these existing electro-thermal power loss models are directly applicable for Si/SiC hybrid switches. These switching devices have distinct operation profile in terms of switching and conduction dynamics compared to the single SiC MOSFET and Si IGBT devices [39].

In this paper, a precise electro-thermal power loss model is proposed for a three-level ANPC inverter consisting of Si/SiC hybrid switches [29]. The power loss model is derived considering the current and voltage characteristics of the hybrid switches. In addition to the operating characteristics of the Si/SiC hybrid devices, the proposed power loss model also takes into account the modulation strategy of the inverter. The current sharing among the internal devices of the Si/SiC hybrid switches and their corresponding gate control strategy (the turn-off and turn-on delay times between the gates of the two internal devices) are also considered during derivation of the analytical electro-thermal power loss model introduced in this paper. The detailed derivation and experimental validation of this model is presented in the following sections.

2 Brief introduction to topology structure and important features

The structure (switch configuration) of the ANPC inverter consisting of Si/SiC hybrid devices is shown in Fig. 1 [30]. This semiconductor device configuration is motivated by the modulation method proposed in Ref. [31] and shown in Fig. 2. It creates two types of switches in the ANPC inverter: a low frequency switches group functioning at 60 Hz line frequency (S_1-S_4) and a high frequency switch group functioning at the carrier (switching) frequency (S_5-S_6). Conduction power loss is predominant for the switches operating at fundamental frequency; the switching power loss of the switches is minor since the switch just twice per fundamental line period. Therefore, Si IGBTs are used for these switching positions since they have lower conduction power loss and lower cost

than SiC MOSFETs especially at higher load currents [16]. For the switches operating at the converter's switching frequency, Si/SiC hybrid switches constituting a smaller current rated SiC device and a larger current rated Si device are utilized. Therefore, they have much lower cost than using SiC MOSFETs for these switching positions [15]. In addition, the Si/SiC hybrid switches have lower power loss in comparison to SiC MOSFETs [12, 15, 20]. Therefore, this ANPC semiconductor device configuration for offers much better tradeoff with regard to the inverter cost and efficiency as demonstrated in Ref. [30].

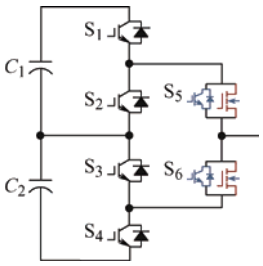

Fig. 1 Topology of the Si/SiC hybrid ANPC inverter

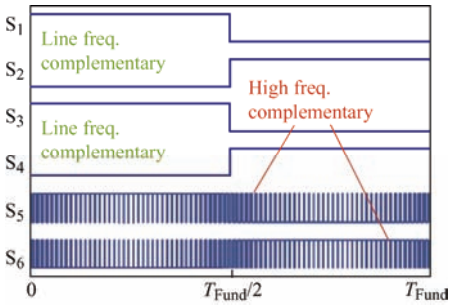

Fig. 2 PWM signals of the Si/SiC hybrid switch ANPC inverter

To maximize the advantages of the Si/SiC hybrid devices (achieve lower inverter cost and reduce the inverter power loss), a smaller current rated SiC device and a larger current rated Si device are commonly chosen to form the hybrid cross switches. However, if the current rating of the internal SiC MOSFET is too small, the SiC MOSFET will experience a large power loss and the junction temperature of the SiC MOSFET may go beyond the maximum allowable device temperature value. If this happens frequently, it may cause reliability issue for the SiC MOSFET such as thermal runaway consecutively for the hybrid switch. This is indeed one of the main research topics for Si/SiC hybrid switches and several researchers have tried to develop current ratio optimization method for Si/SiC hybrid devices to enable determine the tradeoff between power loss, cost, and reliability of these types of switches. Fig. 3 shows the diagram of the current ratio optimization for the Si/SiC hybrid switches proposed in Ref. [15]. As can be seen from the diagram, the performance of the optimization algorithm depends on the accuracy of the device junction temperature and power loss calculation method. The researchers in Ref. [15] utilized simple DC/DC converter circuit to demonstrate the applicability of the proposed hybrid switches using physics-based circuit simulations.

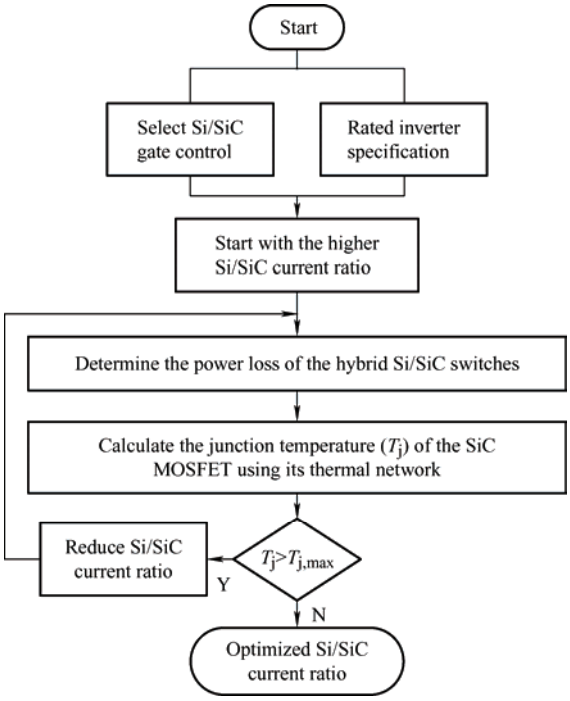

Fig. 3 Optimization algorithm for Si/SiC hybrid device current rating determination

Despite its good accuracy, physics-based circuit simulation takes very long time to run and is sometimes difficult to implement for complicated circuits such as three-level inverter topologies. In addition, the Si/SiC hybrid devices power loss is also reliant on the method for the internal devices gate control (shown in Fig. 4). Therefore, it is important to have a precise analytical power loss model accounting the operating characteristics of the Si/SiC hybrid switches and the internal devices gate control method to facilitate the inverter design optimization in terms the internal devices current ratio optimization and turn-on/turn-off gate delay optimization to attain a good inverter performance tradeoff.

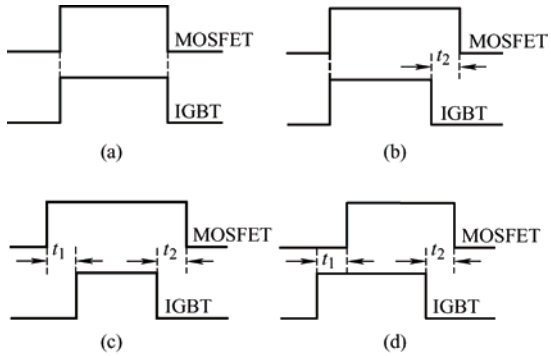

Fig. 4 Gate control methods for Si/SiC hybrid switches

3 The proposed electro-thermal power loss model

To develop an analytical model to estimate the power loss the Si/SiC hybrid switches, it is first important to revise the output characteristics of such kind of switches. The Si/SiC switches output characteristics determines their conduction power loss. Fig. 5 [20] shows the output (*I-V*) characteristics of the Si/SiC hybrid switches and the two internal devices (the Si IGBT and the SiC MOSFET) [16]. As can be seen from the figure, the output characteristics curve of the SiC MOSFET and the Si IGBT have a common intersection (cross-point) which is about 1.15 V and 10 A. This shows the majority of the load current goes via the SiC MOSFET when the load current is below the output characteristics intersection current value and the Si IGBT carries the majority of the load current when the load current is greater than the output characteristics intersection current value.

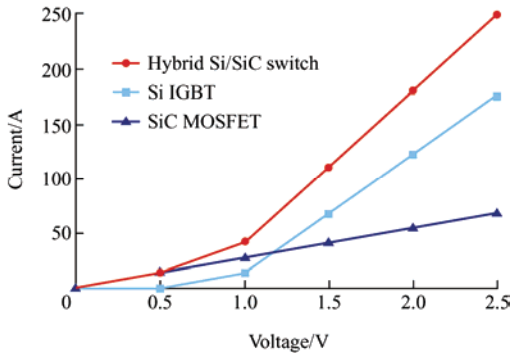

Fig. 5 Typical *I-V* curve of 150 A Si IGBT, 25-mΩ SiC MOSFET and hybrid Si/SiC switch at 125 ℃

The current conduction features of the Si/SiC hybrid devices is also dependent on their gate control method and the corresponding current sharing among them. Fig. 6 shows the nominal operating (conduction and switching) features of Si/SiC hybrid devices [39]. In the output voltage positive half cycle, the two internal devices divide the load current in accordance with their on-state resistance (device current rating) if the voltage across the hybrid devices is greater than the Si IGBT's knee voltage (the Si IGBT forward voltage at which the output current suddenly increases). On the other hand, the SiC device single-handedly carries the output load current if the voltage across the internal devices is smaller than the Si IGBT's knee voltage.

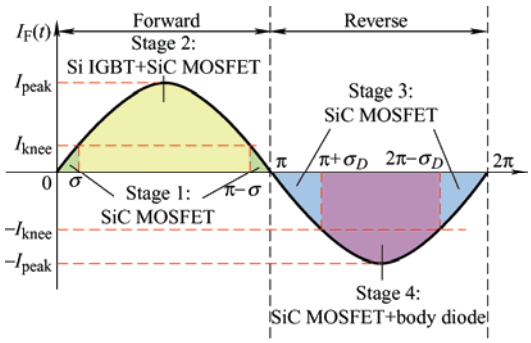

Fig. 6 Operating characteristics of Si/SiC hybrid switches

Likewise, in the output voltage negative half cycle, the output current is handled by the SiC MOSFET and its body diode. If the voltage across the SiC MOSFET is smaller than the SiC MOSFET body diode knee voltage (the body diode forward voltage at which its output current suddenly increases), the output current shall be conducted by the SiC MOSFET channel but both the body diode and the SiC MOSFET channel itself will conduct the load current if the voltage across the Si/SiC hybrid switches larger than the SiC MOSFET body diode knee voltage. This however holds valid when the SiC MOSFET channel is not made to conduct current in third-quadrant (synchronous rectification is not enabled). The SiC MOSFET body diode has very high forward voltage drop (about 4 V [14]) hence it causes higher conduction power loss for power converters if it is used in third-quadrant operation. To eliminate this drawback and achieve lower conduction power loss, synchronous rectification is commonly enabled for silicon carbide devices where the main device channel is made to conduct during its third quadrant operation.

In the output voltage positive half cycle if the voltage across the Si/SiC hybrid switches is smaller than the Si IGBT's knee voltage, only the SiC MOSFET carries the output (load) current of the inverter. On the other hand, if the voltage across the

Si/SiC hybrid devices is larger than the Si IGBT's knee voltage, both the SiC MOSFET and the Si IGBT conduct the load current of the inverter. The current sharing between the two internal devices depends on their equivalent on-state resistance values. Considering their on-state resistances and the Si IGBT knee voltage, the current that flows via the Si IGBT and the SiC MOSFET can be given as in Eqs. (1) and (2).

$$I_{\mathrm{MOS}} = \frac{R_{\mathrm{ce}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} I_{\mathrm{F}} + \frac{V_{\mathrm{knee}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} \tag{1}$$

$$I_{\mathrm{IGBT}} = \frac{R_{\mathrm{ds}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} I_{\mathrm{F}} - \frac{V_{\mathrm{knee}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} \tag{2}$$

where R_{ds} is the SiC MOSFET's device on-state resistance, R_{ce} is the Si IGBT's equivalent on-state resistance that can be determined from the Si IGBT *I-V* curve slope using straight line approximation (piece wise linear approximation) and I_{F} is the Si/SiC hybrid switches total output load current and V_{knee} is the Si IGBT's knee voltage (the forward voltage of the Si IGBT at which the output current suddenly increases). The internal devices (the SiC MOSFET and Si IGBT) equivalent on-state resistance knee voltage values can be obtained from the datasheet of these devices. However, the equivalent on resistance and the voltage across the semiconductor devices during on state (conduction) are dependent on the device's junction temperature.

The drain-to-source on-state resistance ($R_{\mathrm{ds(on)}}$) of SiC MOSFETs increases when their junction temperature increases since they are an enhancement mode devices like Si MOSFETs [9, 12]. Like with the threshold voltage of SiC MOSFET devices also decreases as their operating junction temperature rises. For example, Microsemi SiC MOSFET devices have a minimum threshold voltage of 1.7 V at room temperature, but this reduces to about 0.8 V at their typical maximum operating junction temperature (175 ℃) [37]. Another effect of temperature on SiC MOSFET characteristics is the effect on the forward voltage of the body diode of the SiC MOSFET. The forward voltage of the body diode of an SiC MOSFET also increases with higher junction temperature values [17]. Junction temperature also has similar effect on silicon devices. The collector-to-emitter equivalent on-state resistance and on-state voltage of Si IGBTs also increases with higher junction temperature values [17, 29].

To properly account the dependency of the devices on-state resistance and forward voltage on their junction temperature, they need to be scaled according to Eqs. (3)-(5). This parameter scaling for accounting the junction temperature dependency of the semiconductor device parameters is commonly used and proved to have good accuracy in several literatures [17-18, 39].

$$R(T_{\mathrm{j}}) = R(T_1) + \sigma_{\mathrm{T}}(T_{\mathrm{j}} - T_1) \tag{3}$$

$$V_{\mathrm{knee}}(T_{\mathrm{j}}) = V_{\mathrm{knee}}(T_1) + \sigma_{\mathrm{T}}(T_{\mathrm{j}} - T_1) \tag{4}$$

$$\sigma_{\mathrm{T}} = \frac{R(T_2) - R(T_1)}{T_2 - T_1} \tag{5}$$

where R denotes R_{ce} and R_{ds}, T_{j} denotes the internal devices junction temperature, T_1 and T_2 denote the internal devices junction temperatures provided in their corresponding output (*I-V*) characteristics. The semiconductor device datasheet usually provides the devices characteristics for two operating temperatures commonly 25 ℃, 150 ℃; but this depends on the device manufacture and the device type.

Using the well-established semiconductor devices conduction power loss analytical equation ($P_{\mathrm{cond}} = r_{\mathrm{on}} \cdot I_{\mathrm{rms}}^2$ [40-42]), the conduction power loss of the Si/SiC hybrid switches then determined as in Eqs. (6) and (7) using the relationship of the two internal devices current sharing.

$$P_{\mathrm{Cond\_MOS}} = \begin{cases} R_{\mathrm{ds}} \cdot I_{\mathrm{F}}^2 & I_{\mathrm{F}} < I_{\mathrm{knee}} \\ R_{\mathrm{ds}} \cdot \left(\dfrac{R_{\mathrm{ce}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} I_{\mathrm{F}} + \dfrac{V_{\mathrm{knee}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} \right)^2 & I_{\mathrm{F}} \geqslant I_{\mathrm{knee}} \end{cases} \tag{6}$$

$$P_{\mathrm{Cond\_IGBT}} = \begin{cases} 0 & I_{\mathrm{F}} < I_{\mathrm{knee}} \\ \left(\dfrac{R_{\mathrm{ds}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} I_{\mathrm{F}} - \dfrac{V_{\mathrm{knee}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} \right) \times \left[V_{\mathrm{knee}} + \left(\dfrac{R_{\mathrm{ds}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} I_{\mathrm{F}} - \dfrac{V_{\mathrm{knee}}}{R_{\mathrm{ce}} + R_{\mathrm{ds}}} \right) \cdot R_{\mathrm{ce}} \right] & I_{\mathrm{F}} \geqslant I_{\mathrm{knee}} \end{cases} \tag{7}$$

For reverse current (the forward voltage's negative half cycle), the output current of the Si/SiC hybrid switches will be carried by the SiC MOSFET channel and the body diode of the SiC MOSFET device. The two devices share this current in accordance with Eqs.

(8) and (9) when the output voltage across the hybrid devices is larger than the SiC MOSFET body diode knee voltage when the SiC MOSFET channel is not made to conduct in third quadrant (synchronous rectification is not enabled).

$$I_{\text{rev\_MOS}} = \frac{R_{\text{D}}}{R_{\text{D}} + R_{\text{ds}}} I_{\text{rev}} + \frac{V_{\text{D}}}{R_{\text{D}} + R_{\text{ds}}} \tag{8}$$

$$I_{\text{rev\_diode}} = \frac{R_{\text{ds}}}{R_{\text{D}} + R_{\text{ds}}} I_{\text{rev}} - \frac{V_{\text{D}}}{R_{\text{D}} + R_{\text{ds}}} \tag{9}$$

where R_{D} is the resistance of the body diode of the SiC MOSFET and V_{D} is the tun-on voltage of the SiC MOSFET body diode. For this application, the SiC MOSFET is made to conduct the load current in third quadrant (synchronous rectification is enabled) as can be the case in many applications to reduce conduction power loss hence the conduction power loss of the SiC MOSFET in third quadrant is calculated as in Eq. (10).

$$P_{\text{cond}} = R_{\text{ds}} I_{\text{rms}}^2 \tag{10}$$

The switching losses of the hybrid devices can be determined using parameters extracted their datasheet. One of the parameters manufacturers provided in their device datasheet is the energy losses of semiconductor devices. These switching energy loss values are normally given at a test condition that may be different for the specific application at hand. But they can be scaled according to Eqs. (11) and (12) [17, 40, 43] assuming linear relationship between the semiconductor devices switching energy losses and their corresponding operating voltage and current. The switching energy losses of semiconductor devices do not heavily depend on their junction temperature [9]. Thus, the semiconductor devices switching energy losses can be approximated from the datasheet losses provided at 25 ℃.

$$E_{\text{on\_hard}}(I_{\text{F}}, T_{\text{j}}) = E_{\text{on\_ref}} \left(\frac{I_{\text{F}}}{I_{\text{ref}}} \right)^{\alpha_1} \times \left(\frac{V_{\text{dc}}}{V_{\text{ref}}} \right)^{\alpha_2} \tag{11}$$

$$E_{\text{off\_hard}}(I_{\text{F}}, T_{\text{j}}) = E_{\text{off\_ref}} \left(\frac{I_{\text{F}}}{I_{\text{ref}}} \right)^{\beta_1} \times \left(\frac{V_{\text{dc}}}{V_{\text{ref}}} \right)^{\beta_2} \tag{12}$$

where V_{dc} and V_{ref} are the input dc bus voltage and the dc bus voltage used in the device's datasheet, I_{F} and I_{ref} are the forward current of the application and the forward current stated in the device's datasheet, α_1, α_2, β_1 and β_2 are the coefficients of the nonlinear empirical approximation. Nonlinear empirical approximation is applied for the hybrid devices switching energy loss scaling to transform the energy losses from the datasheet voltage and current values to the actual inverter operating voltage and current values.

The Si/SiC hybrid switches gate control method also affects the internal devices losses. If the two internal devices operate simultaneously, both devices share the loss incurred on them according to their on-state resistance and their switching speed (switching time). However, if there is a delay time between the gates of the Si IGBT and the SiC MOSFET during switching instant, the device which turns on first and turns off later experiences larger switching energy loss than the device which turns off first and turns on later. In addition, if the gate delay time is too large, the device which is conducting during the delay time will carry the full load current hence will experience additional conduction power loss. Therefore, the effect of the turn on and turn off gate delay times on the switching and conduction power losses of the hybrid Si/SiC switches must be properly modeled.

Since the SiC MOSFET has much higher switching speed than the Si IGBT, it turns on very quickly and handles the majority of the turn on energy loss [11, 13]. Hence no turn on gate delay time is usually necessary and the Si IGBT and the SiC MOSFET are made to turn on simultaneously. However, the turn off gate delay time is critical for optimizing the switching energy loss of the hybrid devices. Due to the slower switching speed of the IGBT and its tail current, the Si IGBT has large turn off energy loss. Hence to eliminate the large turn off energy loss of the Si IGBT, a turn off gate delay time ($T_{\text{off\_delay}}$) is commonly used between the gates of the two devices. Accounting the turn off gate delay time between the gates of the SiC MOSFET and the Si IGBT, the two internal devices power losses can be given as in Eqs. (13) and (14) [17, 43].

$$P_{\text{loss\_MOS}} = \left(D_{\text{eff}} + f_{\text{sw}} \cdot T_{\text{off\_delay}} \right) E_{\text{cond\_MOS}} + f_{\text{sw}} \left(E_{\text{on\_MOS}} + E_{\text{off\_MOS}} \right) \cdot \exp(\delta \cdot T_{\text{off\_delay}}) \tag{13}$$

$$P_{\text{loss\_IGBT}} = \left(D_{\text{eff}} - f_{\text{sw}} \cdot T_{\text{off\_delay}} \right) E_{\text{cond\_IGBT}} + f_{\text{sw}} \left(E_{\text{on\_IGBT}} + E_{\text{off\_IGBT}} \right) \cdot \exp(-\delta \cdot T_{\text{off\_delay}}) \tag{14}$$

where f_{sw} is inverter's switching frequency, δ is exponential time constant of the dependency of the switching energy loss on gate turn off delay time and D_{eff} is the inverter's effective phase duty ratio given by Eq. (15) [44].

$$D_{\text{eff}} = \frac{1}{2\pi}\int_0^{\pi}\left(1+M\sin(\theta+\phi)\right)\mathrm{d}\theta \tag{15}$$

where ϕ is the load power factor angle and M is modulation index. From Eqs. (13) and (14), we can see that the hybrid devices switching energy losses are exponentially dependent on the gate turn off delay time. The switching energy loss of the SiC MOSFET increases exponentially while the switching energy loss of the Si IGBT decreases exponentially with the gate turn off delay time. During the gate turn of delay time, the SiC MOSFET carries the full load current hence it experiences an extra conduction power loss due to the gate turn off delay time as shown in the first term of Eq. (13). On the other hand, the gate turn off delay time shrinks the mean conduction period of the Si IGBT reducing its conduction power loss as can be seen from the first term of Eq. (14).

The conduction and switching power loss of the switches (S_1-S_4) are calculated similarly using Eqs. (10)-(12) except the R_{ds} in Eq. (10) will be replaced by the on-state resistance of the Si IGBTs (R_{ce}). Then the total power loss of these switches (P_{loss}) can be calculated as in Eq. (16) from their conduction power loss (P_{cond}), switching on energy loss (E_{sw_on}), switching off energy loss (E_{sw_off}) and switching frequency of the inverter (f_{sw}).

$$P_{\text{loss}} = P_{\text{cond}} + f_{\text{sw}}\cdot\left(E_{\text{sw\_on}} + E_{\text{sw\_off}}\right) \tag{16}$$

The total converter power loss then will be the sum of the power losses of the individual switches. The power loss of ANPC inverter is symmetrical [40-41] hence it is only enough to estimate the power losses of the upper switches (S_1, S_2 and S_5) and then multiply the sum by two to calculate the total power loss of the inverter phase leg.

Fig. 7 shows the flowchart of the proposed electro-thermal power loss model [29]. Since temperature does not heavily affect switching losses [9], the turn on and turn off energy losses of the internal devices are determined from the switching energy loss values specified in their corresponding datasheet for room temperature. Nonetheless, the junction temperature of semiconductor devices significantly affects their conduction power loss. Hence, the junction temperature and the conduction power loss of the internal devices are determined iteratively. To begin with, conduction loss is determined from the room temperature datasheet values. Next the junction temperature and the total power loss of the devices are determined iteratively using Eq. (17).

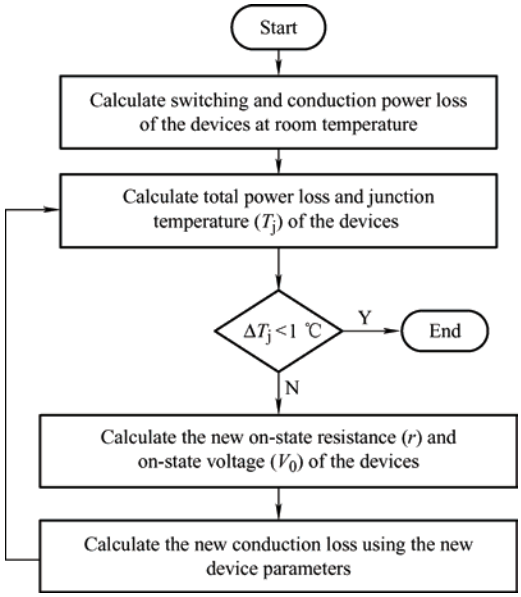

Fig. 7 Flowchart of the proposed device temperature and power loss estimation method

$$T_{\text{j}} = \left(P_{\text{cond}} + P_{\text{sw}}\right)\cdot Z_{\text{th,(j-c)}} + T_{\text{c}} \tag{17}$$

If the temperature difference among consecutive runs is significantly large (for example >1 ℃), the internal devices on-state voltage and resistance recomputed using the newly determined device junction temperature value and then the whole process will be repeated. When the temperature difference among consecutive calculation runs is acceptably small, the process will end, and it returns the devices estimated junction temperature power loss values.

4 The proposed electro-thermal power loss model

The precision of the electro-thermal power loss model introduced in this paper is validated using experimental test. The hybrid devices switching energy losses and their corresponding junction

temperature as well as the overall efficiency of the inverter are used for this purpose. Fig. 8 shows picture of the experimental inverter prototype that is built for the electro-thermal power loss accuracy validation. Tab. 1 shows the information of the semiconductor devices that are chosen for the inverter prototype. The semiconductor devices are chosen considering the required current and voltage rating of the application as well as the device availability.

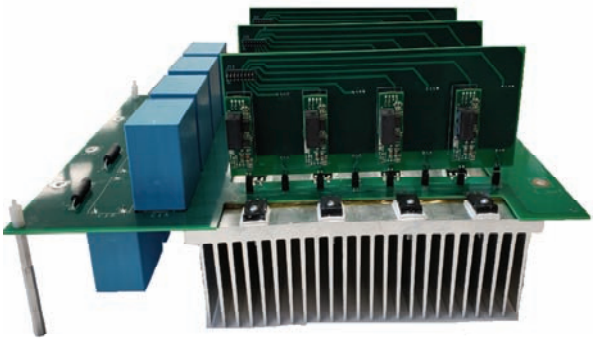

Fig. 8 Picture of the ANPC inverter experimental prototype

Tab. 1 The selected semiconductor devices

Parameter	Value
Full current Si IGBT	IRGP4069DPBF
Full current SiC MOSFET	SCT3030ALGC11
Hybrid Si/SiC switches	IRGPC40S(Si IGBT) SCT3080ALHRC(SiC)

First, DPT test is carried out to measure the switching energy loss of the Si/SiC hybrid devices for the purpose of validating the precision of the switching energy loss model. The internal devices switching (turn off and turn on) energy losses are measured and recorded. Since the semiconductor devices switching energy loss is not heavily dependent on their device junction temperature, the experimental test is performed at room temperature [9]. The operating characteristics of the hybrid devices is shown in Fig. 9. The internal devices switching energy loss is also estimated using the proposed electro-thermal power loss model. The comparison of the estimated and the actual losses for the internal devices of the Si/SiC hybrid switches is shown in Fig. 10 for different load operating conditions. Evident from the comparison that the theoretically calculated switching energy loss of the two internal devices have quite small difference with that of the corresponding measured losses and hence the proposed switching loss model has a very good accuracy.

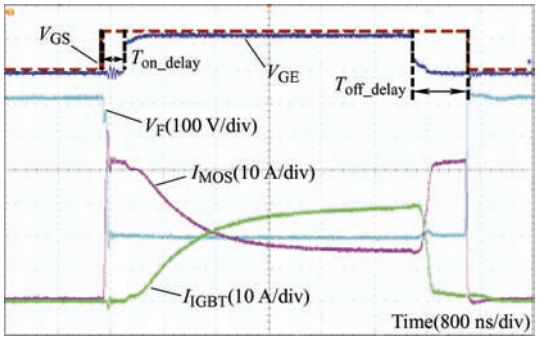

Fig. 9 The Si/SiC hybrid switch operating characteristics

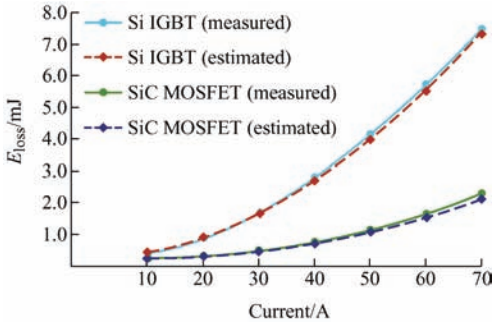

Fig. 10 Comparison of the Si/SiC switching energy losses

The accuracy of overall electro-thermal power loss model is also validated in the same manner using the measured experimental converter efficiency values. The efficiency test of the inverter is also performed for different load operating conditions (different loading percentage of the inverter). The comparison of the measured converter efficiency performance values and the analytically estimated converter efficiency performance values are shown in Fig. 11. This comparison result also validates the precision of the overall electro-thermal power loss model of the inverter proposed in this paper since the difference between the measured and the estimated inverter efficiency values is very small. This small difference is not actually because of the inaccuracy of the inverter electro-thermal power loss model; it is rather because of the power losses in the other inverter components such as the PCBs and cables. The electro-thermal power loss model proposed in this paper accounts only the power losses of the semiconductor devices since the aim of this electro-thermal loss model is to help the theoretical design and analysis of the inverter stage especially for the Si/SiC hybrid switches.

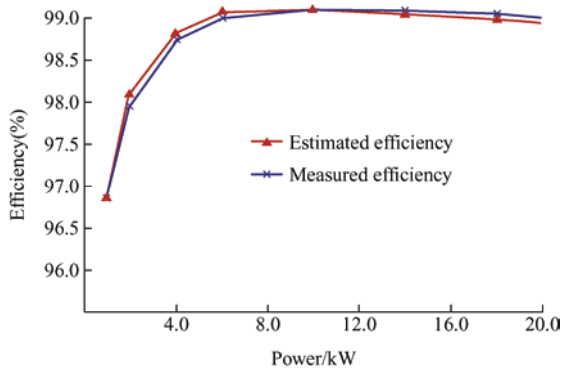

Fig. 11 Comparison of the inverter measured and estimated efficiency values

In addition to power loss and efficiency estimation for the inverter, another purpose of the proposed electro-thermal power loss model is junction temperature estimation for the Si/SiC hybrid switches. To validate this aspect of the proposed electro-thermal power loss model, the case temperature of the internal devices of the Si/SiC hybrid switches are measured and it is compared with their estimated junction temperature values as shown Fig. 12. Due to the inconvenience of getting the internal junction temperature of TO-247 semiconductor devices, their outer package case temperature is measured. The actual junction temperature of the internal devices of the Si/SiC hybrid switches is then calculated using the actual case temperature and the power losses of the internal devices using Eq. (17). As can be seen from Fig. 12, the difference between the actual case Si/SiC hybrid switches case temperature and that of their corresponding estimated junction temperature is very small. In fact, the case temperature of semiconductor devices and the junction temperature of semiconductor devices are supposed to be different because of the temperature drop in the junction-to-case thermal impedance of the devices.

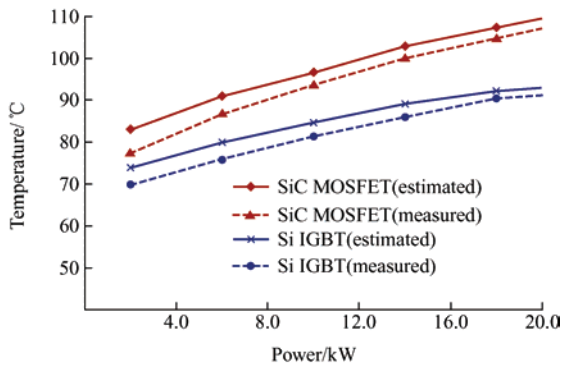

Fig. 12 Comparison of the hybrid devices temperature values

To demonstrate the applicability of the proposed electro-thermal power loss model for use in the design of Si/SiC hybrid switches and the overall optimization of the inverter in general, four different Si/SiC switch pairs (shown in Tab. 2) that can be used for a 20 kW inverter are selected, and their corresponding power loss and device temperature are investigated. Normally one likes to choose an Si/SiC switch with smaller current rated SiC MOSFET to reduce cost but choosing an SiC MOSFET device with a very small rated current causes reliability issue in terms of the device's junction temperature. The internal devices' junction temperature is one indicator of the reliability of the Si/SiC hybrid switches. To ensure reliable operation of the Si/SiC hybrid switches, the maximum device junction temperature of the internal devices should be lower than their maximum permissible junction temperature. To determine which of the four Si/SiC switch pairs in Tab. 2 will be reliable in terms of the maximum temperature of the internal devices, the internal devices junction temperatures are assessed using the proposed electro-thermal power loss model. Fig. 13 shows the internal devices theoretically calculated internal device temperature for different operating conditions and different current ratios of the two internal devices of the Si/SiC hybrid switches. Air cooled heatsink is used for this design as shown in

Tab. 2 Devices considered for the hybrid switches

Ratio	Si IGBT	SiC MOSFET
85:15	IRG4PC50SDPBF (600 V, 42.5 A)	SCT2450KEGC11 (650 V, 7.5 A)
80:20	RGCL80TS60GC11 (600 V, 40 A)	SCT3120AL (650 V, 10 A)
70:30	IXGR50N60B2 (600 V, 35 A)	C3M0120065D (650 V, 15 A)
60:40	IRGPC40S (600 V, 30 A)	SCT3080ALHRC11 (650 V, 20 A)

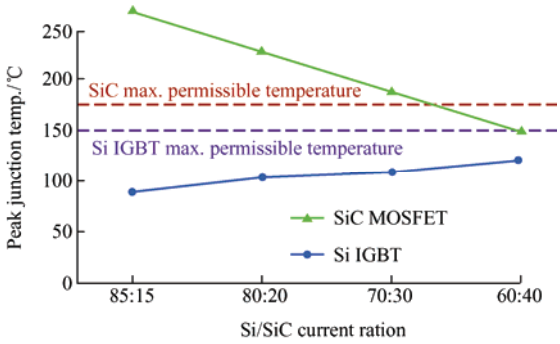

Fig. 13 Estimated peak temperature of the hybrid devices for various current ratios

Fig. 8 hence a case temperature of 65 ℃ is assumed for the internal devices case temperatures for their junction temperature power loss estimation. This case temperature value is the measured case temperature after the inverter is operated for an extended time. Despite the case temperature depends on the cooling approach and the power loss of the inverter, a same cooling approach and hence a similar case temperature is assumed for the different Si/SiC current ratio device pairs. As can be seen from the figure, the maximum junction temperature of the SiC MOSFET increases when the current rating of the SiC MOSFET decreases. For reliable operation, the SiC the SiC MOSFETs maximum junction temperature should be smaller than its maximum permissible value. Hence only the 60:40 hybrid Si/SiC current rating ratio is reliable for the given application. The maximum estimated SiC MOSFET junction temperature is smaller than that of the device allowable maximum temperature value only for this current ratio. It is also important to note that the Si IGBT's estimated peak junction temperature is smaller than the typical maximum allowable operating temperature for Si IGBTs for the different Si/SiC current ratios. Therefore, special care is needed only for the SiC device selection during design of hybrid devices.

To minimize the turn off energy loss of the hybrid Si/SiC switches, the Si IGBT is preferred to turn off before the SiC MOSFET. If the turn off gate delay time is increased, the turn off energy loss of the Si IGBT decreases (even can be fully eliminated if a large gate turn off delay time is used). However, if a very large delay time is used during turn off, the conduction power loss of the SiC device also rises since it is carrying the current during the delay time in the turn off transient. Therefore, there must be an optimal gate turn off delay time ($T_{\text{off\_delay\_opt}}$) for specific Si/SiC current ratio and application. Fig. 14 shows the Si/SiC hybrid switch internal devices switching energy losses for different gate turn off delay time values. The switching energy loss of the Si IGBT decreases and the switching energy loss of the SiC MOSFET increases with increasing gate turn off delay time resulting in a parabolic shaped total switching loss curve for the hybrid devices as can be seen from the figure. The optimal gate turn off delay time value is the value that results in minimum switching energy loss for the hybrid devices (in this case about 1.5 μs).

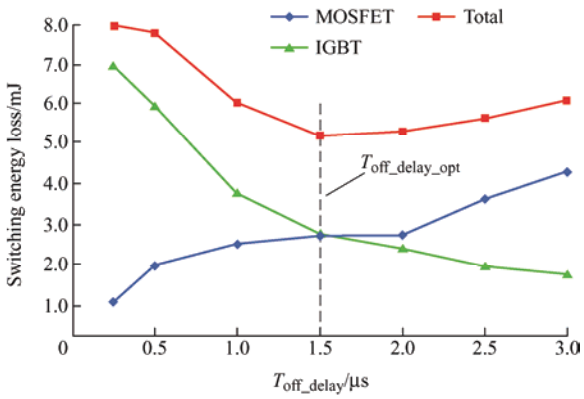

Fig. 14 The Si/SiC hybrid switches energy loss for different gate turn-off delay time values

The junction temperature of the semiconductor devices is estimated using the electro-thermal power loss model of the inverter developed in this paper. Since the power loss of ANPC inverter is symmetrical [40-41], only the junction temperature of the upper switches (S_1, S_2 and S_5) are shown here. The junction temperature of the upper switches is also estimated using PLECS electro-thermal simulation in order to verify the accuracy of the proposed electro-thermal power loss model. Fig. 15 shows the comparison of the estimated junction temperatures of the upper switches and the simulated junction temperature of the upper switches using PLECS. As can be seen from the figure, the estimated and the simulated junction temperature values of the switches have a good match with each other.

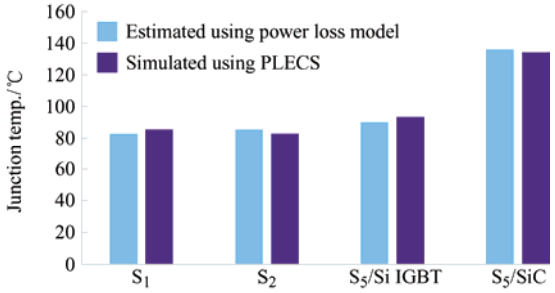

Fig. 15 Comparison of the estimated and PLECS simulated junction temperature values for the upper devices

5 Conclusions

In this paper, a precise electro-thermal power loss model is presented for an Si/SiC hybrid switches based three-level active neutral point clamp inverter. First,

the operating characteristics of Si/SiC hybrid switches is reviewed and the impact on the development of the electro-thermal power loss model is explained. Basically, the junction temperature and power loss of Si/SiC hybrid switches are dependent on the gate control method between the gates of the two internal devices and the sharing of the forward current among them. Therefore, the developed electro-thermal power loss model takes into consideration these two important factors. In addition, the control and modulation strategy of the inverter is also taken into account when developing the model.

The precision of the developed electro-thermal power loss model is validated with actual data gathered from experimental test. The Si/SiC hybrid switch switching losses and the overall efficiency of the inverter are used for the model validation. The measured inverter efficiency and switching energy loss of the internal switches of the Si/SiC hybrid switches have a very small difference in comparison to that of the theoretically calculated converter efficiency and switching energy losses of the internal Si/SiC hybrid switches verifying the accuracy of the developed electro-thermal power loss model. The developed electro-thermal power loss model enables designers to perform design and optimization of the internal devices of the Si/SiC hybrid switches and the overall inverter performance in terms of the cost and efficiency.

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Dereje Woldegiorgis (S'18) received BSc. degree in Electrical and Computer Engineering from Arba Minch University, Ethiopia in 2009 and an Erasmus Mundus joint M.Sc. degree from University of Nottingham, UK, University of Oviedo, Spain and Polytechnic Institute of Coimbra, Portugal in 2014. He is currently working towards his Ph.D. degree at the University of Arkansas, Fayetteville, AR, USA and doing summer internship as a Power Applications Engineer at Wolfspeed, Fayetteville, AR, USA. He was a recipient of the Outstanding Presentation Award for the 2021 IEEE Applied Power Electronics Conference (APEC).

His research interests include modulation and control of power electronic converters, multilevel converter topologies, and renewable energy integrations and embedded system programming.

H. Alan Mantooth (S'83-M'90-SM'97-F'09) received the B.S. and M.S. degrees in Electrical Engineering from the University of Arkansas in 1985 and 1986, respectively, and the Ph.D. degree from the Georgia Institute of Technology in 1990. He then joined Analogy, a startup company in Oregon, where he focused on semiconductor device modeling and the research and development of modeling tools and techniques. In 1998, he joined the Faculty of the Department of Electrical Engineering at the University of Arkansas, Fayetteville, where he currently holds the rank of Distinguished Professor. His research interests now include analog and mixed-signal IC design & CAD, semiconductor device modeling, power electronics, and power electronic packaging. Dr. Mantooth helped establish the National Center for Reliable Electric Power Transmission (NCREPT) at the UA in 2005. Professor Mantooth serves as the Executive Director for NCREPT as well as two of its centers of excellence: the NSF Industry/University Cooperative Research Center on Grid-connected Advanced Power Electronic Systems (GRAPES) and the Cybersecurity Center on Secure, Evolvable Energy Delivery Systems (SEEDS) funded by the U.S. Department of Energy. In 2015, he also helped to establish the UA's first NSF Engineering Research Center entitled Power Optimization for Electro-Thermal Systems (POETS) that focuses on high power density systems for transportation applications. Dr. Mantooth holds the 21st Century Research Leadership Chair in Engineering. He serves as Immediate Past-President for the IEEE Power Electronics Society in 2019-2020. Dr. Mantooth is a Fellow of IEEE, a member of Tau Beta Pi and Eta Kappa Nu, and registered professional engineer in Arkansas.