Modulation and Voltage Balancing Control of Dual Five-level ANPC Inverter for Ship Electric Propulsion Systems

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Abstract: Open-end winding motors are used extensively in ship electric propulsion systems, in which medium-voltage high-power inverters are a critical component. To increase the system voltage and power density, a dual five-level active neutral-point clamped (ANPC) inverter is proposed herein to drive medium-voltage open-end winding motors for ship electric propulsion. Each phase of this inverter comprises two five-level ANPC bridges and all the phases are powered by a common direct-current link. A hybrid modulation method is proposed to control this inverter. The series-connected switches in all the five-level ANPC bridges are operated at the fundamental frequency, and the other switches are controlled with a phase-shifted pulse-width modulation (PWM), which can achieve a natural balance between the neutral-point voltage and flying capacitor voltages in a carrier period. A closed-loop capacitor voltage balancing method based on adjusting the duty ratios of the PWM signals is proposed. The neutral-point voltage and flying capacitor voltages can be controlled independently and balanced without affecting the output phase voltage. Simulation and experimental results are presented to demonstrate the validity of this method.

Keywords: Multilevel inverter, active neutral-point clamped (ANPC), capacitor voltage balance, open-end winding motor drive

1 Introduction

All-electric ships are the future trend in modern ships owing to their advantages of high fuel efficiency, high power density, and high dynamic response [1-3]. Medium-voltage direct current (MVDC) systems offers many advantages over medium-voltage alternating current systems; therefore, the former are regarded as the next-generation ship integrated power system (IPS) [1-2]. High-power medium-voltage inverters are crucial as a critical component in MVDC electric propulsion systems. With the continuously increasing demand for power and grid voltage, conventional two-level dc-ac inverters are no longer suitable [4]. In fact, multilevel converters have received increasing attention in recent years owing to their merits of low voltage stresses, reduced common-mode voltage, high operating voltage, and high harmonic performance. Among multilevel topologies, neutral-point-clamped (NPC), flying-capacitor (FC), and cascaded H-bridge (CHB) multilevel converters are the earliest and most classic topologies in the industry [5-7].

Three-level NPC converters, which were first proposed in 1981 [8], are a competitive and extensively used topology for medium-voltage applications [8-9]. Compared with FC and CHB converters, it features the highest power density [10]. However, limited by the blocking voltages of the present semiconductors, it cannot be readily applied to high-voltage drives exceeding 6 kV [7]. When the number of voltage levels increases to four or more, NPC converters are affected by the neutral-point (NP) voltage imbalance problem, which impedes their application in the industry [11]. Although some new modulation and control techniques can be used to solve this problem, such

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as carrier-overlapped PWM [12-13], virtual-vector PWM [14], and model-predictive control [15], they present increased power losses and harmonics.

Compared with multilevel NPC inverters, FC multilevel converters use fewer switches and are not confronted by the NP voltage balance problem [10, 16]. The main drawback of this topology is the large number of FCs, which increases the system volume, weight, and control complexity significantly. CHB converters are extensively used in high-voltage applications [17]. The shortcoming of this topology is that numerous isolated DC sources are required; hence, it is not suitable for MVDC ship IPSs.

The modular multilevel converter is an emerging multilevel converter topology that has garnered increasing attention in recent years [18-20]. However, it is affected by low-frequency capacitor voltage fluctuations in medium-voltage drive applications [19-20], and it requires significant numbers of switches and capacitors; therefore, the power density of the entire system is decreased.

To further increase the voltage levels and reduce the number of devices, numerous new multilevel topologies are investigated based on combinations of present topologies, which are classified as hybrid multilevel topologies. The stacked multicell (SMC) converter is one of the earliest hybrid multilevel topologies [21-22]; it is configured as a two FC multilevel converters stacked together. The five-level active neutral-point clamped (5L-ANPC) converter is another hybrid multilevel topology that combines a three-level ANPC converter and a two-level cell [23]. Compared with a 5L-SMC converter, a 5L-ANPC converter uses fewer capacitors and hence the power density will be higher. Many other hybrid topologies have been investigated [24-29]. A four-level nested neutral-point clamped (NNPC) inverter is proposed in Ref. [24], which is an extension of the 3L-NPC converter that can operate at higher voltages. Furthermore, a five-level NNPC inverter is proposed in Ref. [25]. Subsequently, four- and five-level hybrid-clamped (HC) converters are proposed in Refs. [26-27], and they can be regarded as the variation of FC multilevel converters with reduced flying capacitors. However, both the NNPC and HC topologies require more flying capacitors than the 5L-ANPC converter.

To improve the DC-link voltage utilization, fault tolerance, and harmonic performance, one promising configuration is to use an open-end winding motor fed by two inverters at each end. Several power circuit configurations have been reported for open-end winding induction motor drive, such as the dual two-level inverter [28], dual three-level NPC inverter [29-30], and dual three-level ANPC inverter [31-32]. Similarly, to further extend the power and voltage range, the abovementioned SMC, ANPC, NNPC, and HC multilevel topologies can be configured into an H-bridge structure to drive the single phase of an open-end winding motor. As previous mentioned, the dual five-level ANPC structure offers the best cost performance and highest power density among all these solutions [33]. Additionally, a dual five-level inverter with reduced switch-count is proposed in Ref. [34]. For this inverter, only eight switches and two diodes are used per bridge and no FCs are required. However, its DC-link is powered by four separated DC sources to solve the NP voltage balance problem, which is the main drawback of this topology.

Another solution for open-end winding motor drive is to use multilevel DC-link (MLDCL) inverters [35], which can be regarded as an H-bridge with a multilevel DC-link voltage. An MLDCL can be a diode-clamped phase leg, a flying-capacitor phase leg, or cascaded half-bridge cells [35]. Based on this idea, a hybrid cascaded multilevel converter for electric vehicles is proposed in Ref. [36], and it can be extended to more levels owing to the modular structure. However, each submodule of this topology must be powered by a battery or an isolated DC source; hence, it is not suitable for a ship IPS with a single DC bus. Another MLDCL topology named "symmetrical hybrid multilevel inverter" is proposed in Ref. [37]. Its DC-link is a five-level DC/DC converter; as such, the output phase voltage comprises nine levels. The common shortcoming among all MLDCL topologies is that the H-bridge cell will bear the total DC-link voltage, and this necessitates the series connection of power devices.

The structure of the dual 5L-ANPC inverter is shown in Fig. 1. Each phase of this inverter is

composed of two 5L-ANPC bridges and drives an isolated load. Therefore, the phase voltage comprises a maximum of nine voltage levels. A key issue pertaining to this inverter is the voltage unbalance of the FCs and DC-link capacitors, which may worsen

the harmonic performance and result in the over-voltage of semiconductors and capacitors. This may arise from the dispersion of capacitor parameters, drive signal delay, dead-time effect, unbalanced load current, etc.
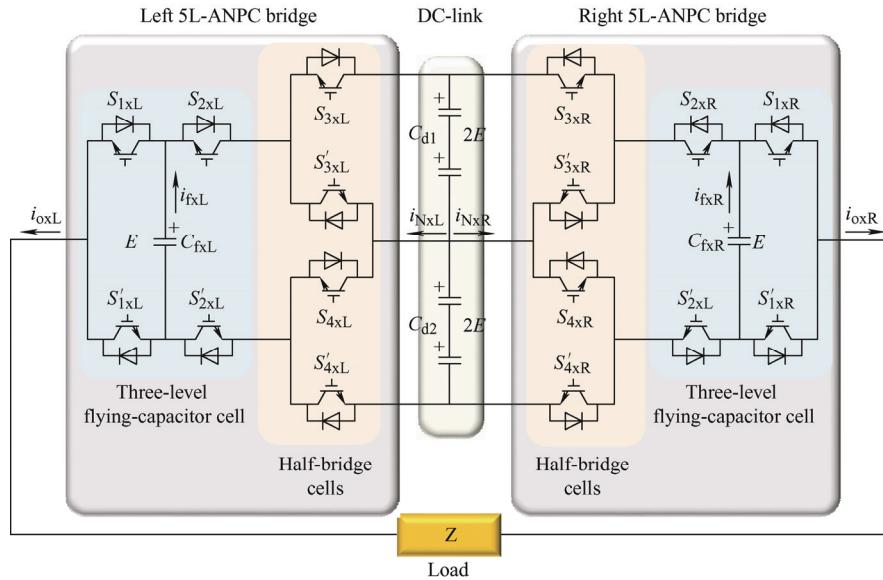

Fig. 1   A single phase of the dual 5L-ANPC inverter

Many modulation methods can be used to control this converter, such as selective harmonic elimination PWM [38-39], space vector PWM (SVPWM) [40-43], hybrid modulation [44], phase-disposition PWM (PDPWM) [45], and phase-shifted PWM (PSPWM) [46].

SVPWM affords good control performance in terms of NP voltage balance by selecting the appropriate redundant vectors and switching sequences. However, it is more complex for higher voltage levels owing to the rapid increase in voltage vectors and redundant switching states [40-44]. To alleviate this problem, a hybrid modulation method that combines the three-level SVPWM and PSPWM is proposed in Ref. [44]. The NP voltage is balanced with three-level SVPWM and the FC voltages are balanced with PSPWM. Hence, the modulation process is simplified significantly.

Compared with multilevel SVPWM schemes, carrier-based PWM schemes are simpler and more suitable for converters with high voltage levels. Both PDPWM and PSPWM can be used to control the 5L-ANPC converter [45-46]. The FC voltages can be balanced by selecting the appropriate redundant switching states when using PDPWM [45] or adjusting the dwell time of two redundant switching states when

using PSPWM [46]. However, the NP voltage is balanced by the same zero-sequence voltage injection method, which is only suited for star-connected loads without a neutral line.

This paper is a major revision of Ref. [33]. To solve the capacitor voltage balancing problem of the dual 5L-ANPC inverter, a hybrid modulation method based on PSPWM is proposed, which permits the fundamental frequency switching of series-connected switches and equal frequency switching of other switches. Moreover, mathematical models of the NP current and FC current based on this modulation method is derived, in which the average values of both the FC currents and NP current are zero in a carrier period. Furthermore, a closed-loop capacitor voltage balancing method is proposed, which does not require a zero-sequence voltage and only adjusts the four PWM signals slightly. Simulation and experimental results are presented to demonstrate this method.

2   Modulation method and natural voltage balance ability

As shown in Fig. 1, each 5L-ANPC bridge comprises two half-bridge cells and a three-level FC cell. If the DC-link voltage is assumed to be a constant

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and equal to $4E$, then the voltage stresses of the switches in the half-bridge cells and FC cell are $2E$ and E, respectively. Switches S_{1xy}-S_{4xy} and S'_{1xy} - S'_{4xy} are operated complementarily, and S_{3xy} and S_{4xy} are always switched synchronously, where the symbol x represents phase a, b, or c and y represents the left or right half-bridge L or R, respectively.

Each 5L-ANPC bridge can output five voltage levels with eight switching states. All the switching states are summarized in Tab. 1, where i_{fxy} and i_{Nxy} are the corresponding FC current and NP current, respectively, and i_{oxy} is the phase current.

Tab. 1   Switching states of the 5L-ANPC bridge

S_{4xy}	S_{3xy}	S_{2xy}	S_{1xy}	i_{fxy}	i_{Nxy}	V_{oxy}	Switching states
0	0	0	0	0	0	$-2E$	V0
0	0	0	1	i_{oxy}	0	$-E$	V1
0	0	1	0	$-i_{oxy}$	i_{oxy}	$-E$	V2
0	0	1	1	0	i_{oxy}	0	V3
1	1	0	0	0	i_{oxy}	0	V4
1	1	0	1	i_{oxy}	i_{oxy}	E	V5
1	1	1	0	$-i_{oxy}$	0	E	V6
1	1	1	1	0	0	$2E$	V7

The main defect of the 5L-ANPC topology is that switches (S_{3xy}, S'_{3xy}) and (S_{4xy}, S'_{4xy}) bear one-half of the DC-link voltage and requires two switches connected in series for medium-voltage applications; this may reduce the reliability of the inverter. Hence, the series-connected switches can be controlled to operate at the fundamental frequency such that the switching time can be extended appropriately. As shown in Tab. 1, S_{3xy} and S_{4xy} are turned off when the output voltage is negative and turned on when the output voltage is positive. Therefore, (S_{3xy}, S'_{3xy}) and (S_{4xy}, S'_{4xy}) can be operated at the fundamental frequency based on the polarity of the reference voltage.

Furthermore, the FC cell can be controlled by the classic PSPWM. The phase-shifted angle of the two carriers of each FC cell is $180°$. Moreover, to generate more voltage levels, the carriers of the two FC cells must be phase shifted. To achieve the best harmonic performance, the four carriers should be evenly distributed such that the phase-shifted angle between the two FC cells is $90°$.

In this study, the switching functions of switches S_{1xy}-S_{4xy} are S_{f1xy}-S_{f4xy} are defined. As shown in Tab. 1, two conditions apply for the instantaneous voltage V_{oxy} of bridge y in phase x, i.e.,

(1) When the output voltage is negative, S_{3xy} and S_{4xy} are turned off. Subsequently, the output bridge voltage V_{oxy} can be written as

$$V_{oxy} = -2E + (S_{f2xy} + S_{f1xy}) \cdot E \tag{1}$$

(2) When the output voltage is positive, S_{3xy} and S_{4xy} are turned on. Subsequently, the output bridge voltage V_{oxy} can be written as

$$V_{oxy} = (S_{f2xy} + S_{f1xy}) \cdot E \tag{2}$$

By combining the two conditions above, the output voltage V_{oxy} can be simplified to

$$V_{oxy} = [2 \cdot (S_{f3xy} - 1) + S_{f2xy} + S_{f1xy}] \cdot E \tag{3}$$

Therefore, the output voltage V_{ox} for phase x can be written as

$$V_{ox} = V_{oxL} - V_{oxR} =$$
$$[2(S_{f3xL} - S_{f3xR}) + (S_{f2xL} - S_{f2xR}) + (S_{f1xL} - S_{f1xR})] \cdot E \tag{4}$$

If E is selected as the base voltage value, then the voltage range of a single bridge is $[-2, 2]$. The switching function of the series-connected switches can be defined as follows

$$S_{f3xy} = S_{f4xy} = \begin{cases} 1 & 0 \leqslant u_{oxy} \leqslant 2 \\ 0 & -2 \leqslant u_{oxy} \leqslant 0 \end{cases} \tag{5}$$

where u_{oxy} is the reference voltage of a single bridge, whose value range is -2 to 2.

To operate the left and right bridges symmetrically, u_{oxy} can be expressed as follows

$$\begin{cases} u_{oxL} = u_{ox}/2 \\ u_{oxR} = -u_{ox}/2 \end{cases} \tag{6}$$

where u_{ox} is the reference phase voltage, whose value range is -4 to 4.

When (S_{3xy}, S'_{3xy}) and (S_{4xy}, S'_{4xy}) are operated at the fundamental frequency, the reference modulation voltage u_{refx} for (S_{1xy}, S'_{1xy}) and (S_{2xy}, S'_{2xy}) can be written as follows

$$u_{refxy} = \begin{cases} u_{oxy}/2 & 0 \leqslant u_{oxy} \leqslant 2 \\ (u_{oxy} + 2)/2 & -2 \leqslant u_{oxy} \leqslant 0 \end{cases} \tag{7}$$

Based on Eqs. (5)-(7), the diagram of the hybrid modulation method is shown in Fig. 2.

(a) The PWM signals and voltages of the left and right bridge
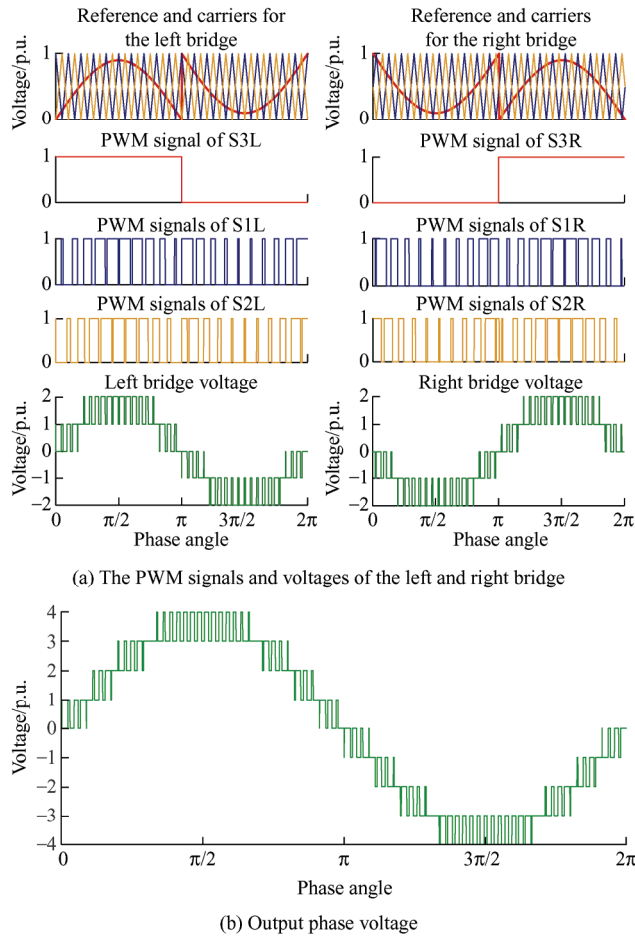

(b) Output phase voltage

Fig. 2   Hybrid modulation method for dual 5L-ANPC inverter

The NP voltage and FC voltages can only be balanced by regulating the NP current and FC currents. Therefore, the current model should be derived first.

For the DC-link capacitors, the load current flows out of the NP when S'_{3xy} and S_{2xy} are switched on or S_{4xy} and S'_{2xy} are switched on. Because S_{3xy} and S_{4xy} are turned on and off simultaneously, the instantaneous NP current of a single 5L-ANPC bridge can be written as follows

$$i_{Nxy} = \begin{cases} (1 - S_{f2xy}) \cdot i_{oxy} & 0 \leqslant u_{oxy} \leqslant 2 \\ S_{f2xy} \cdot i_{oxy} & -2 \leqslant u_{oxy} \leqslant 0 \end{cases} \quad (8)$$

Based on Eq. (8), the instantaneous NP current of a single phase can be written as

$$i_{Nx} = i_{NxL} + i_{NxR} = \begin{cases} -(S_{f2xL} + S_{f2xR} - 1) \cdot i_{ox} & 0 \leqslant u_{ox} \leqslant 4 \\ (S_{f2xL} + S_{f2xR} - 1) \cdot i_{ox} & -4 \leqslant u_{ox} \leqslant 0 \end{cases} \quad (9)$$

where i_{ox} is the phase current and $i_{oxL} = -i_{oxR} = i_{ox}$. If the carrier frequency is sufficiently higher than the fundamental frequency, then the reference modulation

voltage and phase current can be assumed as constant in a carrier period. Based on Eq. (9), the average NP current of a single phase in a carrier period can be written as

$$\bar{i}_{Nx} = \bar{i}_{NxL} + \bar{i}_{NxR} = \begin{cases} -(d_{2xL} + d_{2xR} - 1) \cdot i_{ox} & 0 \leqslant u_{ox} \leqslant 4 \\ (d_{2xL} + d_{2xR} - 1) \cdot i_{ox} & -4 \leqslant u_{ox} \leqslant 0 \end{cases} \quad (10)$$

where d_{2xL} and d_{2xR} are the duty ratios of S_{f2xL} and S_{f2xR} in a carrier period, respectively. Because switches S_{1xy} and S_{2xy} are controlled with PSPWM, the duty ratio of S_{f1xy} and S_{f2xy} in a carrier period can be written as

$$d_{1xy} = d_{2xy} = u_{refxy} \quad (11)$$

Using Eqs. (6), (7), and (11), the following equation can be obtained

$$d_{2xL} + d_{2xR} = u_{refxL} + u_{refxR} = (u_{oxL} + u_{oxR}) / 2 + 1 = 1 \quad (12)$$

Substituting Eq. (12) into Eq. (10), it can be concluded that the average NP current of a single phase is zero, which implies that the NP potential can be naturally balanced in a carrier period using the proposed hybrid modulation method under ideal and steady-state conditions.

For the FC C_{fxy}, the instantaneous flying capacitor current can be written as

$$i_{fxy} = (S_{f1xy} - S_{f2xy}) \cdot i_{oxy} \quad (13)$$

The average FC current in a carrier period is expressed as

$$\bar{i}_{fxy} = (d_{1xy} - d_{2xy}) \cdot i_{oxy} \quad (14)$$

Substituting Eq. (11) into Eq. (14), it can be concluded that the average FC current is zero, and the FC voltages can be balanced naturally in a carrier period under ideal and steady-state conditions.

3   Voltage balancing method

Although the NP voltage and FC voltages can be balanced naturally in a carrier period using the hybrid modulation method, it may diverge under non-ideal and dynamic conditions without closed-loop control. Based on Eqs. (10) and (14), the NP and FC currents can be adjusted by adjusting d_{1xy} and d_{2xy} without affecting the output phase voltage.

Based on Eq. (4), the average phase voltage u_{ox} in a carrier period can be written as

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$$u_{ox} = \begin{cases} 2 + (d_{2xL} - d_{2xR}) + (d_{1xL} - d_{1xR}) & 0 \leq u_{ox} \leq 4 \\ -2 + (d_{2xL} - d_{2xR}) + (d_{1xL} - d_{1xR}) & -4 \leq u_{ox} \leq 0 \end{cases}$$

$$(15)$$

The voltage deviations of the FCs and NP are defined as follows

$$\begin{cases} \Delta u_{fxL} = u_{fxL} - E \\ \Delta u_{fxR} = u_{fxR} - E \\ \Delta u_N = u_{d2} - u_{d1} \end{cases} \qquad (16)$$

where u_{d1} and u_{d2} are the voltages across the upper and lower DC-link capacitors, respectively; E is the nominal voltage of the flying capacitors and is defined as $V_{dc}/4$. To eliminate voltage deviations, the proposed voltage balancing method can be segregated into the following three steps.

Step 1: For the left bridge flying capacitor C_{fxL}, if $sign(\Delta u_{fxL}) \times sign(i_{oxL}) > 0$, then based on Eq. (14), the duty ratio of S_{f1xL} should be increased, whereas the duty ratio of S_{f2xL} should be decreased. To ensure that the output voltage and other capacitor currents are unaffected, the modified duty ratios of S_{f1xy} and S_{f2xy} can be written as

$$\begin{cases} d'_{1xL} = d_{1xL} + \Delta d_{xL} \\ d'_{2xL} = d_{2xL} - \dfrac{1}{3}\Delta d_{xL} \\ d'_{1xR} = d_{1xR} + \dfrac{1}{3}\Delta d_{xL} \\ d'_{2xR} = d_{2xR} + \dfrac{1}{3}\Delta d_{xL} \end{cases} \qquad (17)$$

By substituting Eq. (17) into Eq. (14), the average current of the left bridge flying capacitor C_{fxL} is expressed as follows

$$\bar{i}_{fxL} = (d'_{1xL} - d'_{2xL}) \cdot i_{oxL} = \frac{4}{3}\Delta d_{xL} \cdot i_{oxL} \qquad (18)$$

Substituting Eq. (17) into Eqs. (10), (14), and (15), it is demonstrated that the average NP current, average current of the FC in the right bridge, and average phase voltage are unaffected.

Step 2: Similar to C_{fxL}, for the right bridge flying capacitor C_{fxR}, if $sign(\Delta u_{fxR}) \times sign(i_{oxR}) > 0$, then based on Eq. (14), the duty ratio of S_{f1xR} should be increased, whereas the duty ratio of S_{f2xR} should be decreased. To ensure that the output voltage and other capacitor currents are unaffected, the modified duty ratios of S_{f1xy} and S_{f2xy} can be written as

$$\begin{cases} d''_{1xL} = d'_{1xL} + \dfrac{1}{3}\Delta d_{xR} \\ d''_{2xL} = d'_{2xL} + \dfrac{1}{3}\Delta d_{xR} \\ d''_{1xR} = d'_{1xR} + \Delta d_{xR} \\ d''_{2xR} = d'_{2xR} - \dfrac{1}{3}\Delta d_{xR} \end{cases} \qquad (19)$$

Substituting Eq. (19) into Eqs. (10), (14), and (15), it is demonstrated that the average NP current, average current of the FC in the left bridge, and average phase voltage are unaffected.

Substituting Eq. (19) into Eq. (14), the average current of the right bridge FC C_{fxR} is expressed as follows

$$\bar{i}_{fxR} = (d''_{1xR} - d''_{2xR}) \cdot i_{oxR} = \frac{4}{3}\Delta d_{xR} \cdot i_{oxR} \qquad (20)$$

Step 3: For the NP voltage, if $sign(\Delta u_N) \times sign(i_{ox}) \times sign(u_{ox}) > 0$, then based on Eq. (10), the sum of d_{2xL} and d_{2xR} should be decreased. To ensure that the output voltage and other capacitor currents are unaffected, the modified duty ratios of S_{f1xy} and S_{f2xy} can be written as

$$\begin{cases} d'''_{1xL} = d''_{1xL} - \Delta d_{xN} \\ d'''_{2xL} = d''_{2xL} - \Delta d_{xN} \\ d'''_{1xR} = d''_{1xR} - \Delta d_{xN} \\ d'''_{2xR} = d''_{2xR} - \Delta d_{xN} \end{cases} \qquad (21)$$

Substituting Eq. (21) into Eqs. (14) and (15), it is demonstrated that the average flying capacitor currents and the average phase voltage are unaffected. In this case, the average NP current is as follows

$$\bar{i}_{Nx} = 2\Delta d_{xN} \cdot i_{ox} \qquad (22)$$

where Δd_{xL}, Δd_{xR}, and Δd_{xN} are extremely small and can be controlled using a PI regulator.

Based on Eqs. (17), (19), and (21), the final duty ratio variations can be written as follows

$$\begin{cases} \Delta d_{1xL} = \Delta d_{xL} + \dfrac{1}{3}\Delta d_{xR} - \Delta d_{xN} \\ \Delta d_{2xL} = -\dfrac{1}{3}\Delta d_{xL} + \dfrac{1}{3}\Delta d_{xR} - \Delta d_{xN} \\ \Delta d_{1xR} = \dfrac{1}{3}\Delta d_{xL} + \Delta d_{xR} - \Delta d_{xN} \\ \Delta d_{2xR} = \dfrac{1}{3}\Delta d_{xL} - \dfrac{1}{3}\Delta d_{xR} - \Delta d_{xN} \end{cases} \qquad (23)$$

Subsequently, the four adjusted duty ratios are $d_{1xL} + \Delta d_{1xL}$, $d_{2xL} + \Delta d_{2xL}$, $d_{1xR} + \Delta d_{1xR}$, and $d_{2xR} +$

$\Delta d_{2\text{xR}}$. To minimize the effect of the voltage balancing method on the total harmonic distortion (THD) of the output voltage, the boundaries of $\Delta d_{1\text{xL}}$, $\Delta d_{2\text{xL}}$, $\Delta d_{1\text{xR}}$ and $\Delta d_{2\text{xR}}$ were limited to within ±10% of u_{refxy}. The block diagram of the voltage balancing method is shown in Fig. 3. As presented in Fig. 3, the voltage deviations of the FCs and NP were measured first and input to the respective PI regulators. Subsequently, the three duty ratio variations Δd_{xL}, Δd_{xR}, and Δd_{xN} can be generated. As shown, the voltage balancing of the two FCs and NP were decoupled and independent of each other. The final duty ratios can be obtained by the linear combination of Δd_{xL}, Δd_{xR}, and Δd_{xN}, based on Eq. (23). To avoid over-modulation, the maximum and minimum final duty ratios were set to 1 and 0. In other words, when the original duty ratios are extremely small or large, the final adjustments must be further restricted to ensure that the four duty ratios are between 0 and 1.
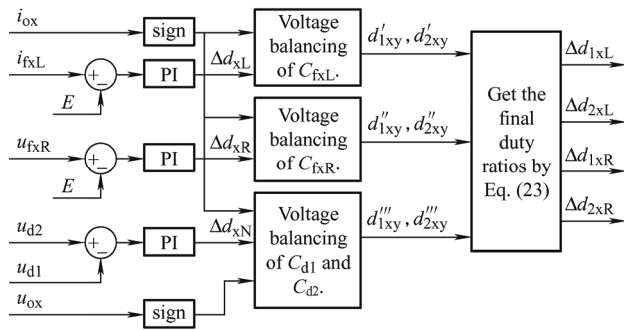
Fig. 3   Block diagram of the voltage balancing method

4   Simulation results

A three-phase dual 5L-ANPC inverter was simulated in the Matlab/Simulink environment, and the associated circuit configuration is shown in Fig. 4. The simulation parameters are shown in Tab. 2.
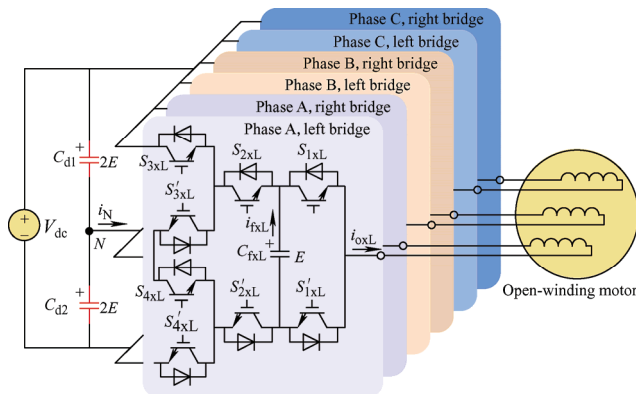

Fig. 4   Circuit configuration of the three-phase dual 5L-ANPC inverter

Tab. 2   Circuit parameters used for the simulation and experiments

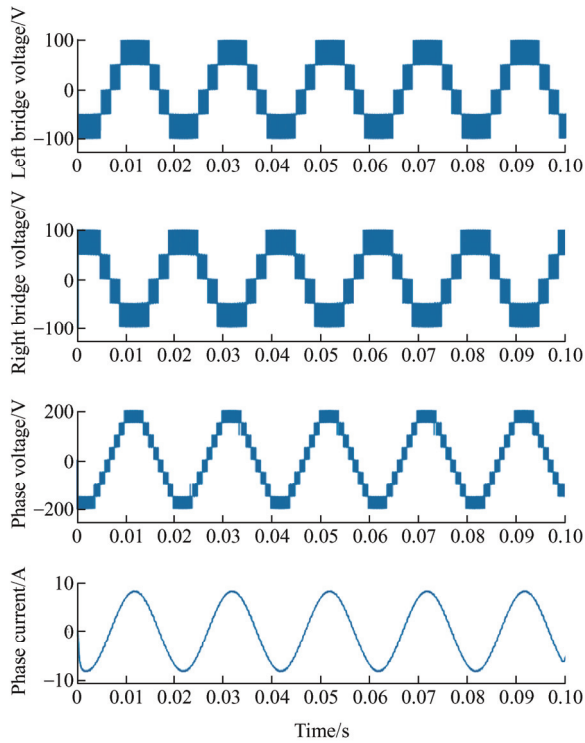| Parameter	Value
DC-link voltage U_{dc}/V	200
DC-link capacitor C_{d1}, C_{d2}/μF	4 700
Flying capacitor C_{fxy}/μF	470
Carrier frequency f_{c}/kHz	2
R-L load	R=20 Ω, L=5 mH

Figs. 5 and 6 present the steady-state simulation results under different modulation indexes. Fig. 5a shows the left and right bridge voltages, phase voltage, and phase current with modulation index $m = 0.9$. The two bridge voltages are out of phase and each comprises five voltage levels. The phase voltage is the difference of the two bridge voltages and comprises nine levels because of PSPWM. Fig. 5b shows the FC voltages and the DC-link capacitor voltages. As shown, all the capacitor voltages were well balanced around their nominal voltages when the proposed voltage balancing method was used.

Because the FC voltages can be balanced within a carrier period, the voltage ripples depend on the maximal charging/discharging time in a carrier period. Therefore, the maximal voltage ripple Δu_{fc} can be written as follows
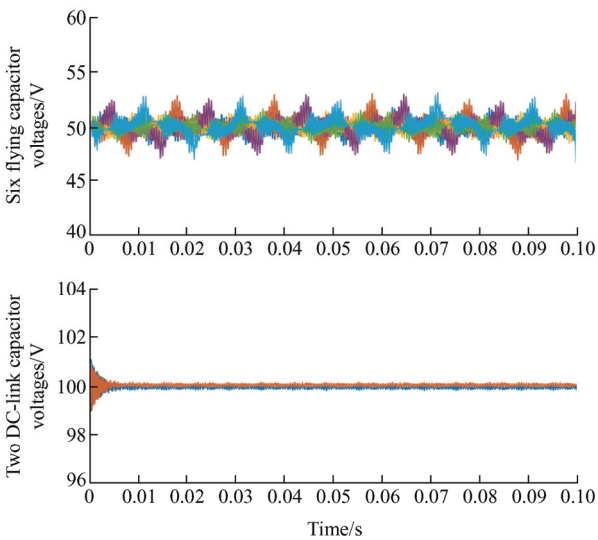
$$\Delta u_{\text{fc}} = \frac{i_{\text{oxy}}T_{\text{s}}}{2C_{\text{f}}} = \frac{i_{\text{oxy}}}{2f_{\text{c}}C_{\text{f}}} \qquad (24)$$

where C_{f} is the capacitance of the FCs, T_{s} the carrier period, and f_{c} the carrier frequency. The simulation result shown in Fig. 5 is consistent with the theoretical analysis.

Fig. 6 shows the simulation results with $m = 0.2$. Both the left and right bridge voltages comprise three levels, whereas the phase voltage comprises only three levels. This is because the reference voltage is extremely small, and a three-level voltage is sufficient to synthesize it. The simulation results demonstrate that the DC-link and FC voltages can be balanced under both high and low modulation indexes.

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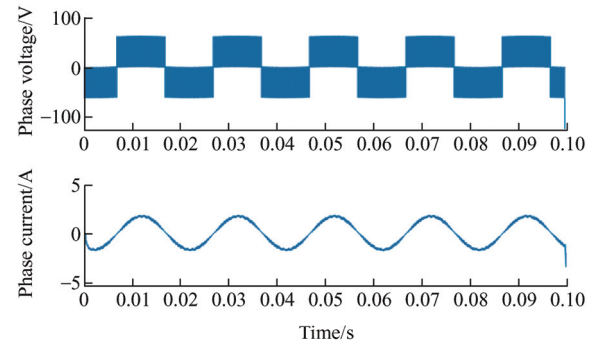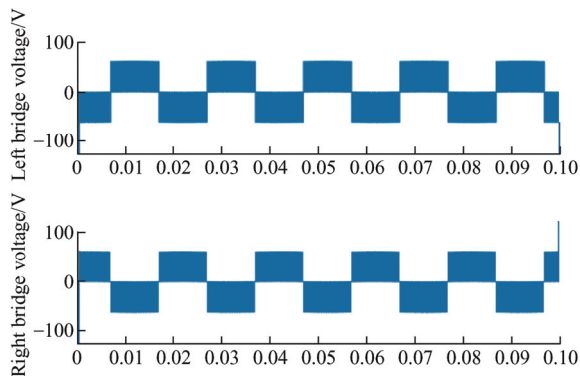Electric Propulsion Systems

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(a) From top to bottom are the left and right bridge voltages, phase voltage and phase current
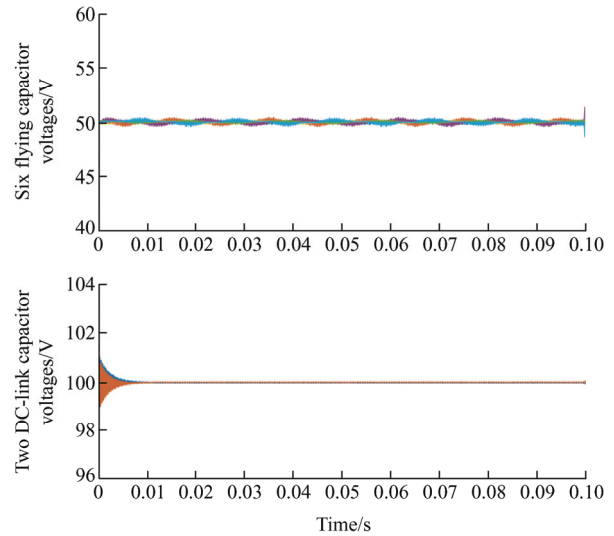

(b) The six flying capacitor voltages (top) and the two DC-link capacitor voltages (bottom)

Fig. 5 Simulation results with the modulation index m=0.9

(a) From top to bottom are the left and right bridge voltages, phase voltage and phase current

(b) The six flying capacitor voltages (top) and the two DC-link capacitor voltages (bottom)

Fig. 6 Simulation results with the modulation index m=0.2

Figs. 7 and 8 present the harmonic spectra of the bridge voltage, phase voltage, and phase current under m = 0.9 and m = 0.2, respectively. First, it is clear that the primary harmonic components were the carrier-frequency and multiple carrier-frequency components. Second, a significant number of double carrier-frequency (4 kHz) components appeared in the bridge voltage, which was caused by the two 180° phase-shifted carriers in a single bridge. However, owing to the phase-shifted angle between the two bridges, the double carrier-frequency components in the phase voltage reduced significantly. Therefore, the primary harmonics in the phase voltage and phase current were quadruple carrier-frequency components, and all the double carrier-frequency components were eliminated.

Figs. 9 and 10 show the dynamic-state results under m = 0.9 when the capacitor voltage balancing method was deactivated. The capacitances and equivalent series resistances of the two DC-link
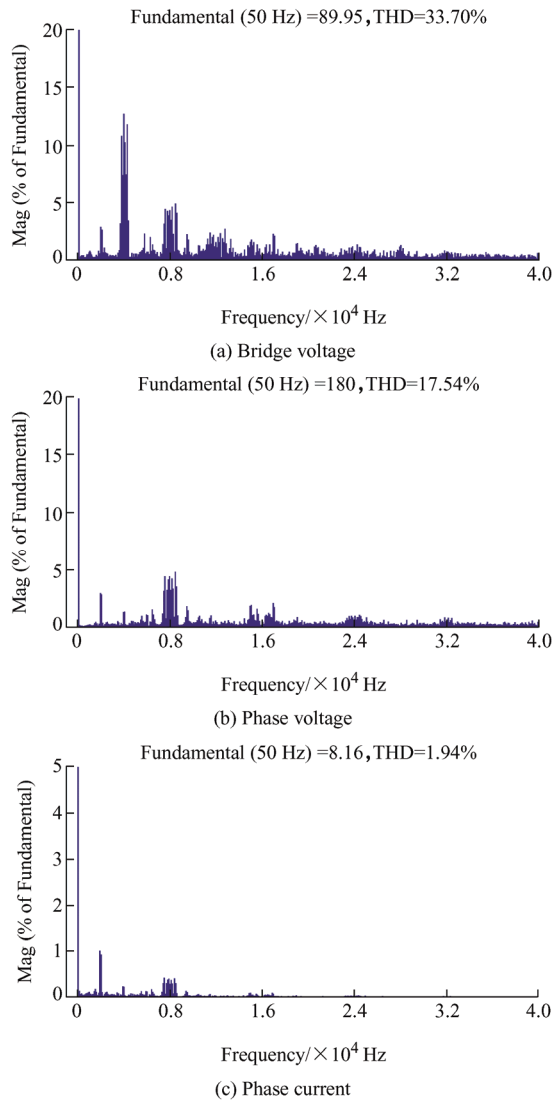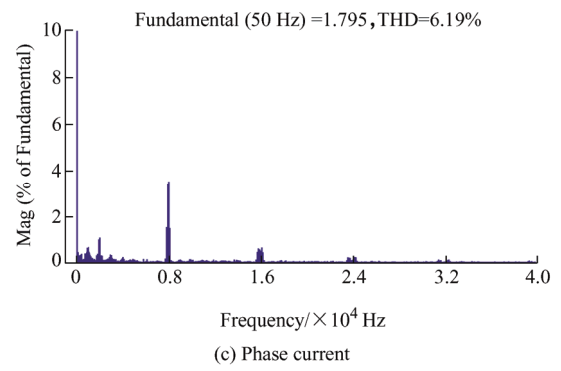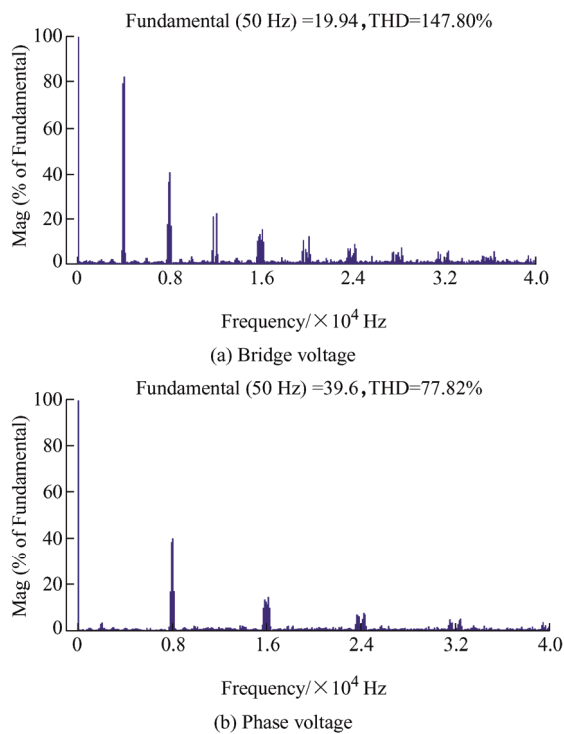
(a) Bridge voltage

(c) Phase current

Fig. 8   Harmonic spectrums with the modulation index m=0.2

capacitors were differently. As shown in Fig. 9, when the capacitor voltage balancing method was deactivated at 0.2 s, the two DC-link capacitor voltages deviated from the reference values rapidly, thereby resulting in a higher voltage stress on the capacitors and switches. Moreover, the harmonic performance of the phase current deteriorated. As shown in Fig. 10, the THD of the load current increased significantly compared with the results shown in Fig. 7c.

(b) Phase voltage

(c) Phase current

Fig. 7   Harmonic spectrums with the modulation index m=0.9

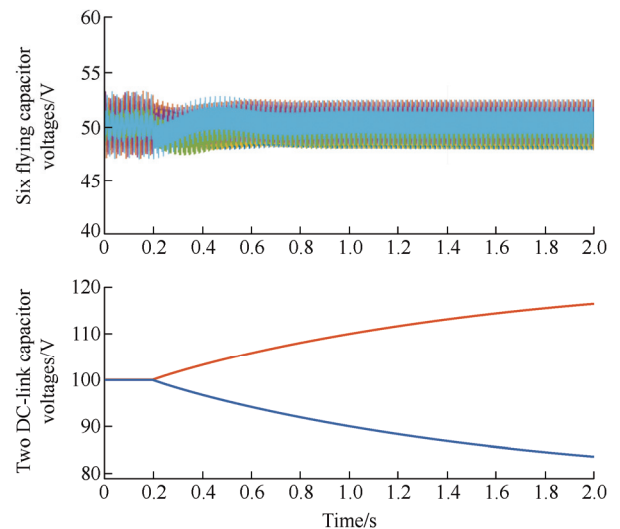(a) Bridge voltage

(b) Phase voltage

Fig. 9   Capacitor voltages when the voltage balancing method is deactivated
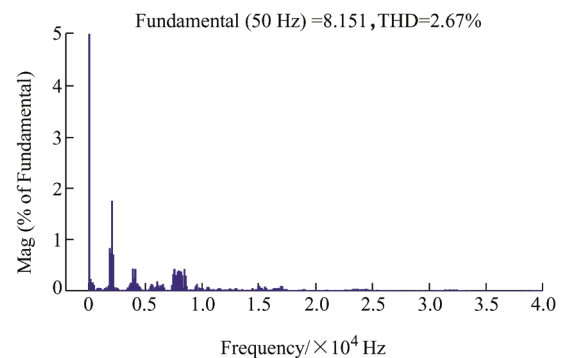
Fig. 10   Harmonic spectrums of the phase current when the voltage balancing method is deactivated

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5 Experimental results

A downscaled three-phase dual 5L-ANPC inverter was built to demonstrate the validity of the proposed modulation and voltage balancing method, as shown in Fig. 11. The control board was based on a DSP chip (TMS320F28335) and a CPLD chip (EPM1270T144C5). The experimental parameters were the same as the simulation parameters.
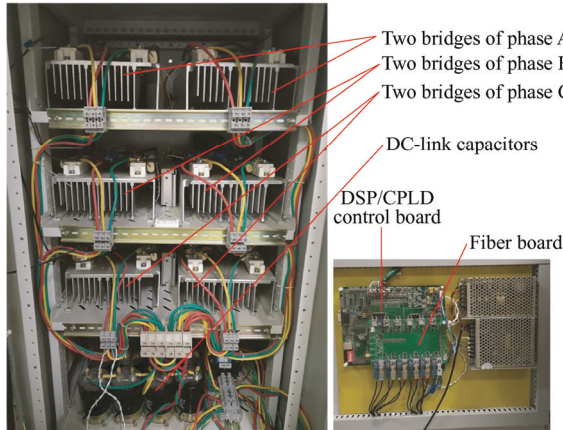

Fig. 11 The down-scaled prototype of
the dual 5L-ANPC inverter

Figs. 12 and 13 present the experimental results with modulation index $m = 0.9$ and $m = 0.2$, respectively. Similar to the simulation results, the phase voltage comprised nine levels when $m = 0.9$ and was reduced to three when $m = 0.2$. The DC-link capacitor and FC voltages were balanced well under these two modulation indexes.

(a) From top to bottom are the left and right bridge voltages,
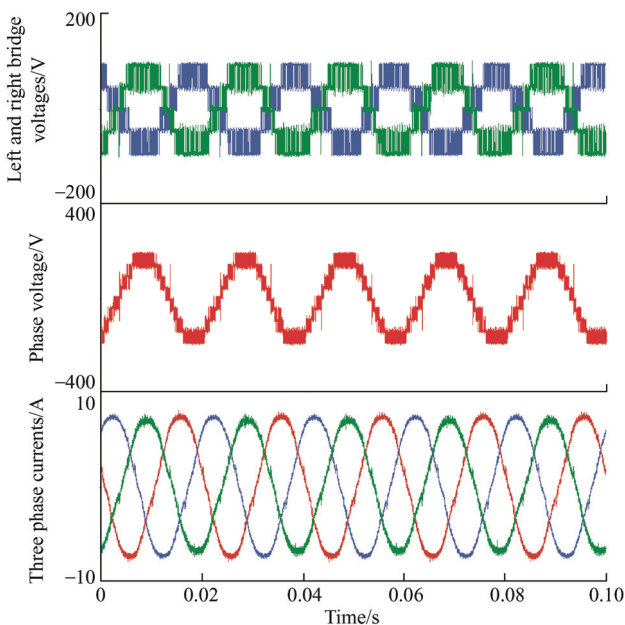phase voltage and three phase currents
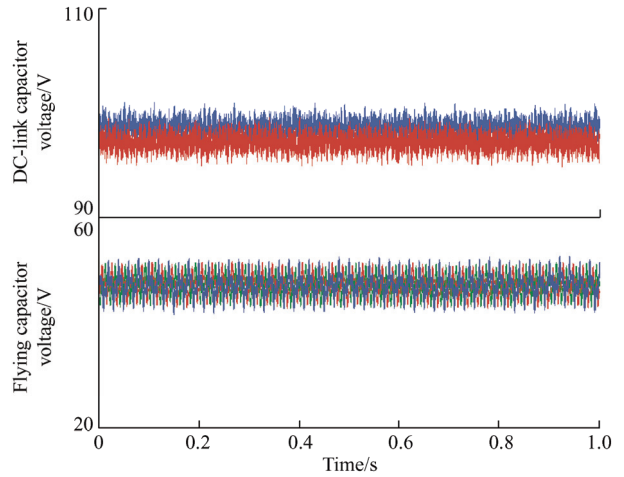
(b) The DC-link capacitor voltage (top) and the flying
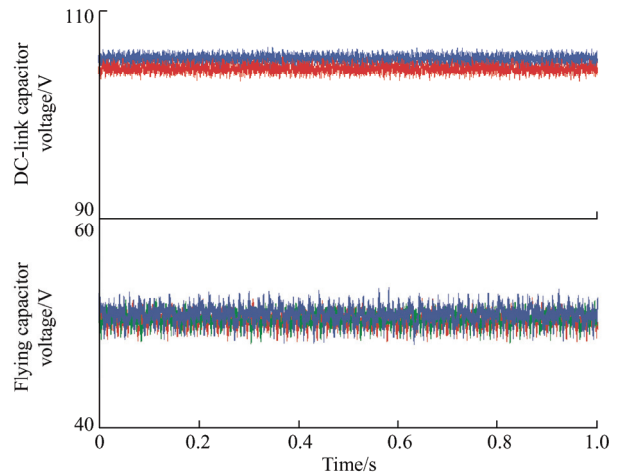capacitor voltage (bottom)

Fig. 12 Experimental results with $m=0.9$
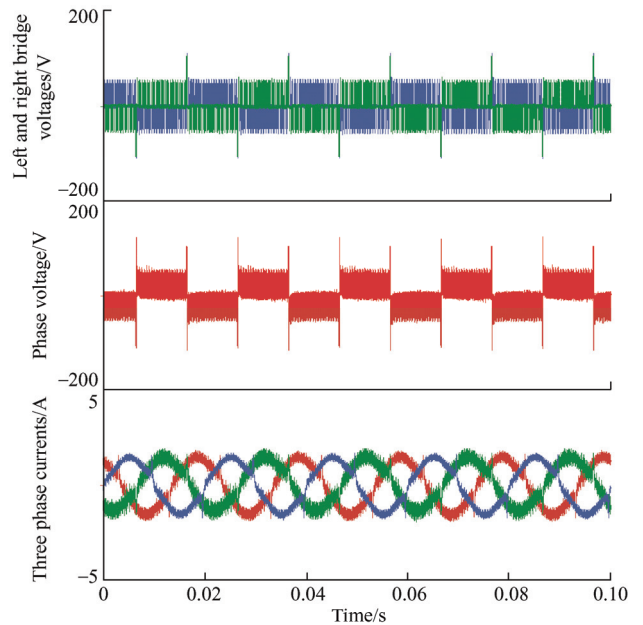
(a) From top to bottom are the left and right bridge voltages,
phase voltage and three phase currents

(b) The DC-link capacitor voltage (top) and the flying
capacitor voltage (bottom)

Fig. 13 Experimental results with $m=0.2$

Figs. 14 and 15 present the harmonic spectra of the bridge voltage, phase voltage, and phase current under $m = 0.9$ and $m = 0.2$, respectively. The THD from the experimental results was similar to the simulation results. Similar to the simulation results, it was clear that a significant number of double carrier-frequency (4 kHz) components existed in the bridge voltage, as shown in Figs. 14a and 15a. However, they were almost completely eliminated in the phase voltage under both conditions, as shown in Figs. 14b and 15b. The main harmonic component in the phase voltage and phase current was the quadruple carrier-frequency (8 kHz) component.
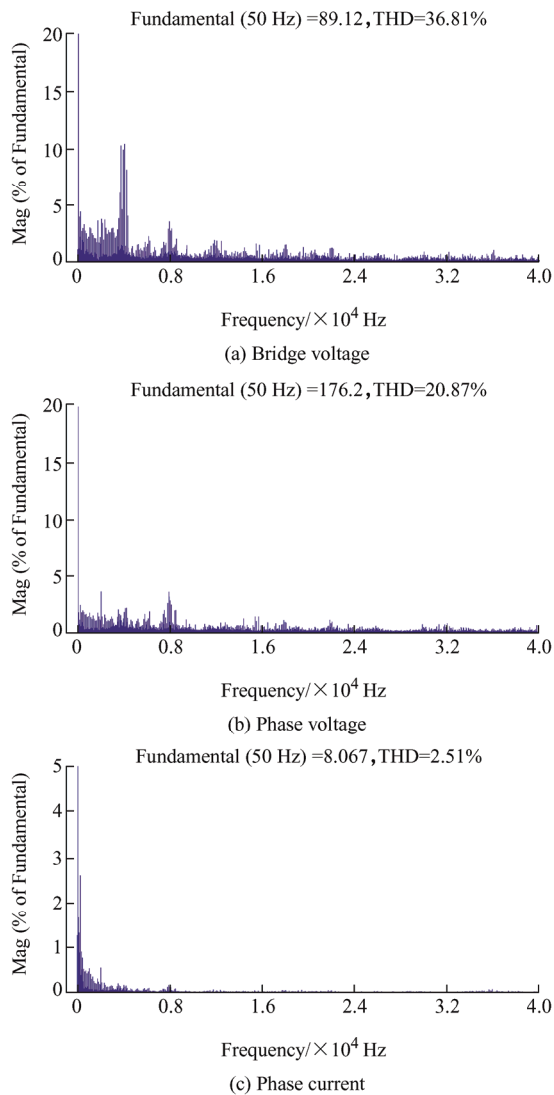

Fundamental (50 Hz) =89.12，THD=36.81%

(a) Bridge voltage

Fundamental (50 Hz) =176.2，THD=20.87%

(b) Phase voltage

Fundamental (50 Hz) =8.067，THD=2.51%

(c) Phase current

Fig. 14   Experimental harmonic spectrums with the modulation index m=0.9

Fundamental (50 Hz) =17.87，THD=180.04%

(a) Bridge voltage

Fundamental (50 Hz) =35.72，THD=91.19%

(b) Phase voltage

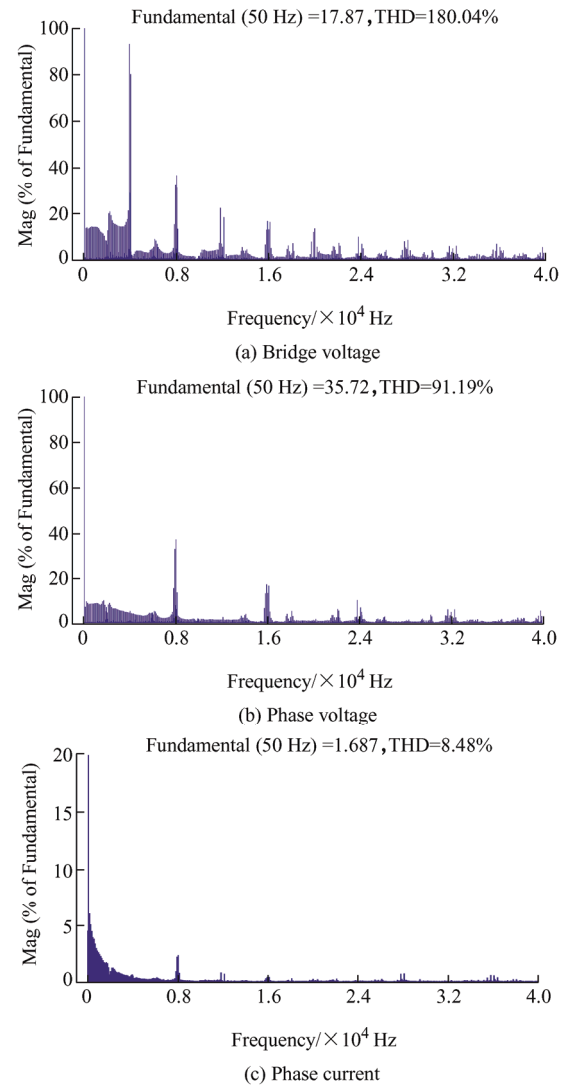Fundamental (50 Hz) =1.687，THD=8.48%

(c) Phase current

Fig. 15   Experimental harmonic spectrums with the modulation index m=0.2

Fig. 16 shows the dynamic experimental results of the DC-link capacitor voltages, FC voltages, and phase currents under an abrupt load change. The load resistance changed abruptly from 20 Ω to 150 Ω and then returned to 20 Ω. During the entire process, the DC-link capacitor voltages and the FC voltages remained balanced.

Fig. 17 shows the dynamic-state performance of the capacitor voltage balancing method. As shown in Fig. 17a, the reference voltages of the upper and lower DC-link capacitors were set to 10% higher and 10% lower than the nominal value first, respectively; subsequently, they were set to the nominal value 5 s later. The two DC-link capacitor voltages traced the new reference values accurately. As shown in Fig. 17b, the reference voltages of the three FCs were set to
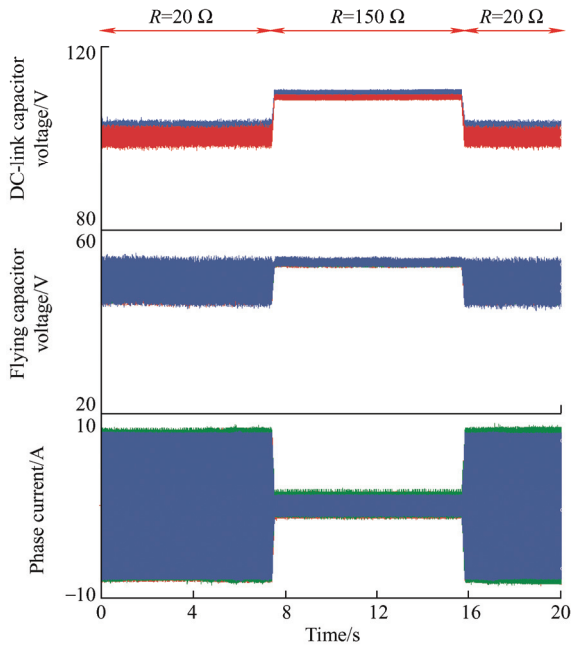
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Fig. 16   Dynamic-state experimental result when the load
resistance is suddenly changed

(a) DC-link capacitor voltages

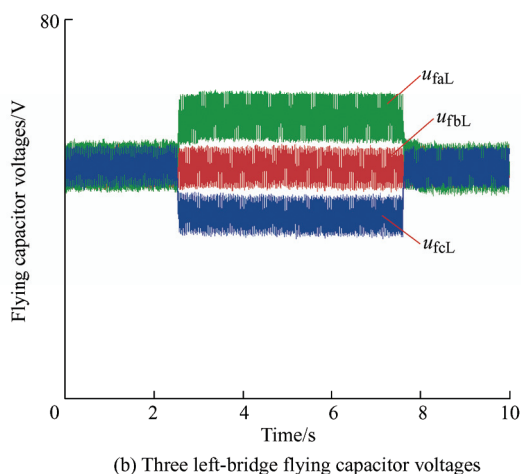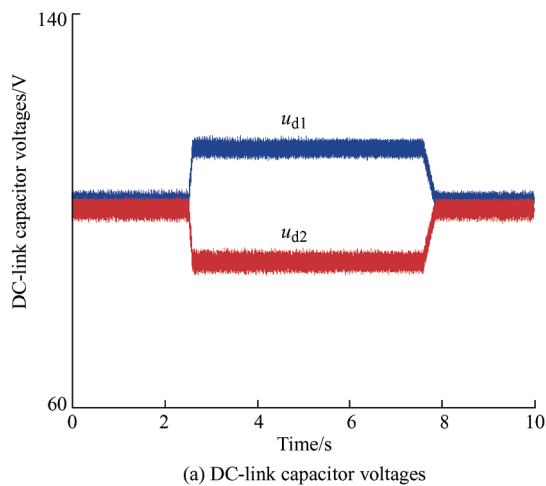(b) Three left-bridge flying capacitor voltages

Fig. 17   Dynamic-state experimental results when the
reference voltages are suddenly changed

20% higher than, equal to, and 20% lower than the
nominal value first and then reset to the nominal value

5 s later. Similarly, the three FC voltages traced the
new reference values accurately. The dynamic-state
results demonstrate that the proposed voltage
balancing method can control the NP and FC voltages
effectively. Moreover, the NP voltage and FC voltages
can be controlled independently without affecting the
other voltages.

6   Conclusions

To fulfill the demands of ship electric propulsion
systems for medium-voltage high-power inverters, a
dual 5L-ANPC inverter for open-end winding motors
was proposed herein. Two 5L-ANPC bridges
constitute an H-bridge for driving an isolated load, and
a nine-level phase voltage can be obtained. A hybrid
modulation method based on PSPWM was proposed
to control this inverter; it permits the fundamental
frequency switching of series-connected switches and
equal frequency switching of other switches. Moreover,
mathematical models of the NP current and FC
currents based on this modulation method was derived.
The average values of both the FC currents and NP
current were zero in a carrier period under ideal
conditions. Therefore, the voltage ripples of both the
NP voltage and FC voltages were of high frequency. A
closed-loop capacitor voltage balancing method based
on adjusting the duty ratios of the PWM signals was
proposed. Simulation and experimental results
validated this method.

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