Fast Online Diagnosis of Open-circuit Switching Faults in Flying Capacitor Multilevel Inverters

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Abstract: Flying capacitor multilevel (FCML) inverter is an attractive power converter topology which provides high-quality staircase output voltage waveforms by cascading flying capacitor cells. However, the large number of semiconductor devices utilized in the FCML inverters degrades the hardware reliability, which may constrain such converters from being applied in safety-critical applications. Targeting at open-circuit switching faults, a fast online fault diagnostic method for FCML inverters is presented. Conventional phase-shifted PWM (PSPWM), which can naturally balance the voltage across flying capacitors, is used as the modulation method in this work. Hence, to retain the simplicity feature of the PSPWM, the proposed diagnostic method is developed so that it does not require any voltage measurements of flying capacitors. Only the output AC voltage and current data along with the switching PWM signals from the microcontroller are needed to detect an open-circuit switching fault, and all such sensory data is typically available in the inverter, requiring no additional sensors or hardware for the implementation of this diagnostic method. The detection process takes 5% of the fundamental period of the inverter output signals to diagnose the faulty switch. Simulation and experimental results are presented to verify the effectiveness of the proposed diagnostic method.

Keywords: Open-circuit, fault diagnosis, flying capacitor, multilevel inverter, wide bandgap devices, PSPWM

1 Introduction

In the past decade, multilevel voltage source converters have gained increasing applications due to their advantages over the conventional two-level counterparts. These advantages include reduced voltage stress on power semiconductor devices, lower output harmonics and common-mode voltage, higher converter efficiency, and increased power capability [1]. As one of the main breeds of multilevel converters used in various industrial applications, flying capacitor multilevel (FCML) converters can achieve higher power density with the advent of wide bandgap (WBG) semiconductor devices, since the size of the flying capacitors is inversely proportional to the converter switching frequency [2-3]. Such high power density feature will likely embrace a promising prospect in weight and space constraint applications, such as electric vehicles and electric airplanes.

In a general FCML converter topology, staircase multilevel output voltage waveforms are obtained by cascading flying capacitor cells along with a number of low voltage switches. However, the high number of semiconductor switches decreases the reliability of the converter by increasing the probability of semiconductor failure occurrence, which constrains the converters from being applied in safety-critical applications [4-5]. Therefore, it is very necessary to diagnose the faulty switches to minimize the downtime cost and enable the potential fault-tolerant operation strategy.

Wire-bonding lift-off due to thermal stress and mismatched coefficients of thermal expansion (CTE) between wire-bonds, chips and the substrate is the root cause for open circuit (OC) faults of power switches [6-7]. Overload operation, gate driver failures, or a short-circuit-fault-induced switch rupture may also lead to such an OC failure mode. OC faults usually result in significant dc offset current, distorted output voltage and current, unequal thermal stress over switching devices, and pulsating torque in motor-drive applications. These can cause cascaded failures and

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eventually complete collapse of the holistic system if an effective diagnostic method is unavailable [8].

On the other hand, short-circuit faults in semiconductor devices typically require ultra-fast diagnosis and protection speed (less than 10 microseconds) due to the limited short-circuit withstanding time [9]. For the emerging wide bandgap semiconductor devices, the required short-circuit fault detection speed becomes shorter, in the range of a few microseconds or even hundreds of nanoseconds, due to the increasing transconductance and decreasing thermal capacity with the small die size [10-11]. Therefore, to guarantee prompt protection speed, instead of relying on online diagnostic algorithms embedded in microcontrollers, short-circuit detection is typically implemented through the gate driver circuits, such as the well-known desaturation circuits implemented in many commercial gate drivers [9]. Therefore, this paper focuses only on the online diagnosis of open-circuit faults of the FCML inverters.

Existing fault-diagnosis methods for FCML inverters mostly use finite control set model predictive control (FCS-MPC) method which requires numerous voltage sensors to monitor the flying capacitors (FC) voltage, increasing the diagnosis implementation cost [12-14]. Should capacitors voltage be measured in this topology, the OC fault detection will be a simple comparison between the reference and actual values of voltages across capacitors. Proposed fault-tolerant scheme for FCML converters in Refs. [15-16] can provide the same number of output voltage levels by shorting the faulty power semiconductors and reconfiguring the gate controls of the inverter. However, their focus is solely on fault-tolerant operation and they lack a reliable and an appropriate fault-diagnosis method to firstly detect the faulty switch and then initiate the post-fault operation mode.

The diagnosis process sometimes is related to the modulation method of the converter, especially if the PWM signals are to be leveraged [17-18]. Among several modulation methods which have already been reported in the literature, phase-shifted PWM (PSPWM) is the one which has the capability to inherently balance the capacitors' voltage without any capacitor voltage measurements [19-20]. Therefore, a fast fault detection method based on PSPWM is proposed in this paper. To accomplish this objective, the available PWM signals and output voltage and current of the inverter will be comprehensively analyzed to detect the faulty switch of the FCML topology.

The remaining content of this paper is organized as follows. Section 2 elaborates the negative impact of an open-circuit switching fault on the FCML converter performance. Section 3 introduces the operating principle of the proposed diagnostic method. Section 4 presents the simulation results and analysis. Section 5 provides the experimental verifications based on a Gallium Nitride (GaN) five-level FCML inverter prototype. Finally, conclusions are given in Section 6.

2 Impact of open-circuit switching faults on FCML inverter

The circuit topology of a five-level FC inverter is shown in Fig. 1. It consists of three flying capacitors with the voltage increments of $V_{dc}/4$ across them and two DC-link capacitors that share the DC-link voltage equally [21]. Provided that dc link capacitor voltages are well-balanced to follow their reference values of $V_{dc}/2$, which can be naturally achieved by using the conventional PSPWM method, the instantaneous output voltage of the inverter can be calculated by using the PWM signals as follows

$$V_o = \frac{V_{dc}}{2}\left(S_1 - \overline{S_1}\right) - V_{c1}\left(S_1 - S_2\right) - V_{c2}\left(S_2 - S_3\right) - V_{c3}\left(S_3 - S_4\right) \quad (1)$$

where $V_{ci,i\in\{1-3\}}$ is the FC voltage and $S_{i,i\in\{1-4\}}$ is 1 if the corresponding switch is ON, and 0 if it is OFF. $\overline{S_i}$ represents the complementary devices in the negative rail of the inverter (bottom devices).

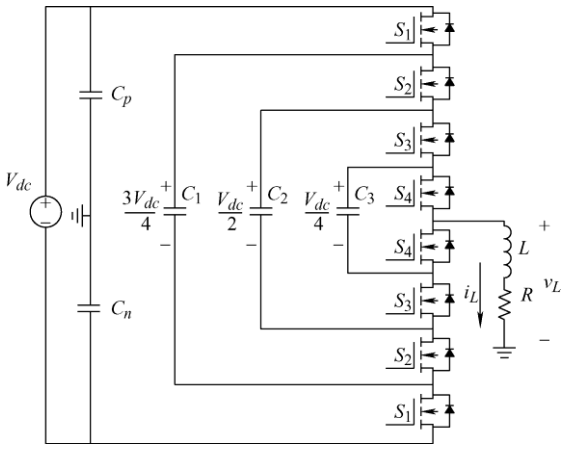
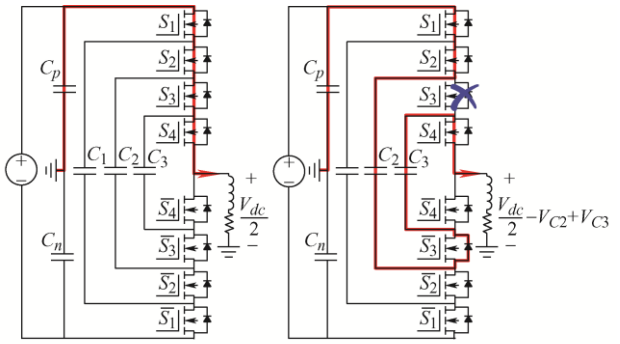


Fig. 1 Single phase 5-level flying capacitor inverter

If the fault occurs in one of the top switches in a positive half-cycle, as shown in Fig. 2, taking an OC fault in S_3 as an example, the load's inductive current will force the diode of the complementary switch, $\overline{D_3}$, to conduct and the current will change its path accordingly until it drops to zero. This will charge and discharge capacitors C_2 and C_3, respectively.



(a) Normal healty opeation (b) An OC fault in S_3 changes the current path

Fig. 2 Current flowing path in 5-level flying capacitor inverter when all switches in the positive rail are conducting

The load voltage and current as well as the voltage waveforms across the flying capacitors and DC-link capacitors are depicted in Fig. 3. The fault dramatically distorts the output voltage and current waveforms, and the desired voltage levels involving the faulty switch will not be available anymore. In addition, the positive half-cycle of the current waveform is clipped due to a fault in one of the positive switches. Following the initial deviation with a high rise time, the voltage across FCs will keep diverging gradually. Depending on the fault location, the voltages may diverge or converge from or to each other. The expected voltage balance across the DC-link capacitors will also be lost. Since each semiconductor switch in a FCML is rated at the potential difference between two adjacent FCs, the remaining healthy semiconductor devices may also fail as a result of over-voltage due to the loss of control over FC and DC-link capacitor voltages. This will likely cause irreversible damages to the inverter and even cascaded failures or disasters to the overall system. Therefore, it is of paramount importance to develop a fast online diagnostic method to promptly detect the faulty switch and achieve fault-tolerant post-fault operation, in order to improve the system reliability.

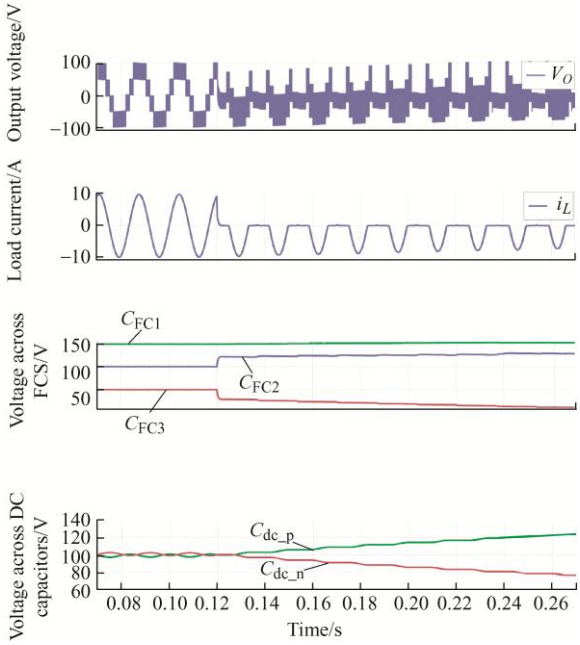


Fig. 3 OC fault of S_3 occurred at t=120 ms

3 Proposed fault diagnostic method

The proposed fault diagnostic method will be introduced in this section. One assumption is that, only single OC fault is considered in this work, rather than multiple OC faults occurring at the same time to the inverter. The proposed method for detecting the faulty switch requires the PWM signals as well as load voltage and current sensory data. As illustrated in Fig. 4, a comparison between the expected output voltage based on the switching function defined in Eq. (1), and the measured output voltage will generate HIGH-logic level signal as a trigger to initiate the diagnosis procedure. A moving average filter block with small averaging time is used to prevent any undesired trigger caused by unbalanced capacitors or electrical noises from the controller or measurements.

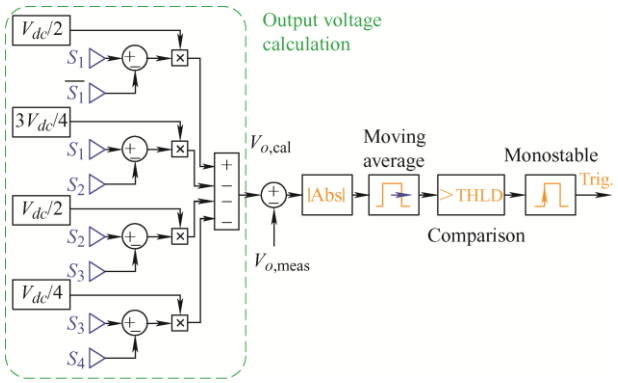


Fig. 4 Comparison between the calculated and the measured voltages to trigger the fault detection algorithm

The second stage of the fault-detection process is assuming that each switch in the circuit is potentially the faulty one. Since there are total eight switches in a phase leg of the five-level FCML topology, an array of eight output voltages will be calculated as follows in which every single element denotes the load voltage supposing that the corresponding switch has failed due to an OC fault

$$V_{o[1\times8]}=\{v_{o1},v_{o2},\cdots,v_{o8}\} \tag{2}$$

Due to the initial rapid change of voltage across FCs following a fault, it is necessary to consider the capacitors' voltage change into Eq. (1). Hence, assuming that flying capacitors $C_{i,i\in\{1-3\}}$ have already been charged to their steady state values, the voltage variation across them can be obtained as follows

$$\Delta v_{c_i}=\frac{1}{C_i}\int_0^t i_L\left(S_i-S_{i+1}\right)\mathrm{d}t \tag{3}$$

where i_L is the measured load current. The block diagram implementation of Eq. (3) is depicted inside a box in Fig. 5. This figure assumes a fault on S_1 and sets S_1 to zero in positive half-cycles since it would not be able to conduct current anymore. However, the anti-parallel diode of the faulty switch will conduct current during negative half-cycles. Therefore, trigger pulse will only affect the calculations when the current direction is positive. Likewise, the remaining seven elements of output voltage array can be simply computed by using similar approach as in Fig. 5.

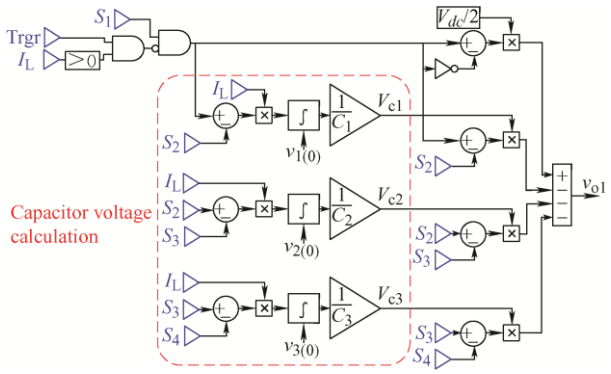


Fig. 5 Output voltage calculation by assuming that S_1 is the faulty switch

In essence, the proposed method calculates the capacitor voltages for each fault scenarios. Meanwhile, based on the calculated FC voltages, the output voltage of the inverter is also calculated. Then, among all the calculated output voltages, the one which is closest to the actual output will be considered as a correct assumption and the corresponding switch will be announced as the faulty switch.

Therefore, as shown in Fig. 6, each element of the calculated output voltage array, $V_{o[i]}$, should be subtracted from the measured voltage separately to generate an array of errors with eight elements, $E_{[1\times8]}$. A moving average filter with a small averaging time is used here to make the error signals more reliable and immune from unwanted noise. This block will be enabled only after trigger signal becomes HIGH. Then, the fault scenario which yields the minimum error of $E_{[1\times8]}$ and remains minimum for at least 5% of the fundamental period will be considered as a correct assumption and the faulty switch will be detected accordingly. The 5% threshold, which makes system robust against any instability issue, is an arbitrary factor and it can be lowered to increase the diagnosis speed. The flowchart in Fig. 7 summarizes the proposed fault detection method.

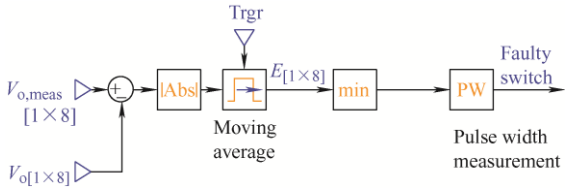


Fig. 6 Comparison between the calculated and the measured voltage values and determining the faulty switch based on the signal with minimum error

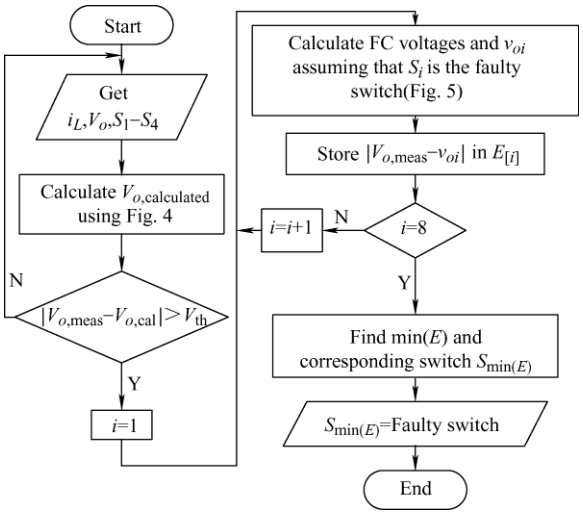


Fig. 7 Flowchart of the proposed diagnostic method

Not only should a fault detection method be accurate, fast, minimally invasive, cost-effective, simple to implement, and computationally efficient, it also should be robust against internal and external disturbances to prevent any erroneous detection [22].

Hence, the robustness of the proposed OC fault detection method against load and modulation index variations will be evaluated in this subsection.

Load changes will affect the ripple voltage across the FCs. In addition, after a fault, it will cause different deviations for FC voltages. However, compared with voltage across the FCs, these effects are negligible and the load voltage, which is the basis of the proposed detection method, will not change considerably. Therefore, the proposed method is robust against load variations.

The five-level flying capacitor inverter can generate five voltage levels in high modulation indices (m>0.51) while the output voltage for lower modulation indices will only have three distinct voltage levels. Hence, it is of significant importance for the fault detection method to cope with varying output voltage levels. As shown in Fig. 4, the expected output voltage of the inverter is being calculated based on the FCs voltage and PWM signals. Accordingly, in lower modulation indices, where the output voltage consists only three levels, the PWM signals will work in such a way that calculated output voltage also has three levels. This means that the OC detection method needs to do the exactly similar comparison as before, but with different waveform of the output voltage.

4 Simulation results

To verify the proposed fault diagnosis method, modeling and simulations have been conducted in PLECS software, with the test parameters provided in Tab. 1. An OC fault is applied on S_2 at t=55 ms. The measured and the expected output voltages as well as the load current are shown in Fig. 8. Following the fault, voltage drops immediately and triggers fault detection circuit. In addition, the load current loses the positive half-cycle due to the fault in one of the top switches.

Tab. 1 Main parameter ratings of the FCML inverter

Parameter	Value
DC-bus voltage V_{dc}/kV	1.5
Rated power P/kW	30
Output frequency f_o/Hz	60
Switching frequency f_{sw}/kHz	100
Load resistance R/Ω	10
Load inductance L/μH	815

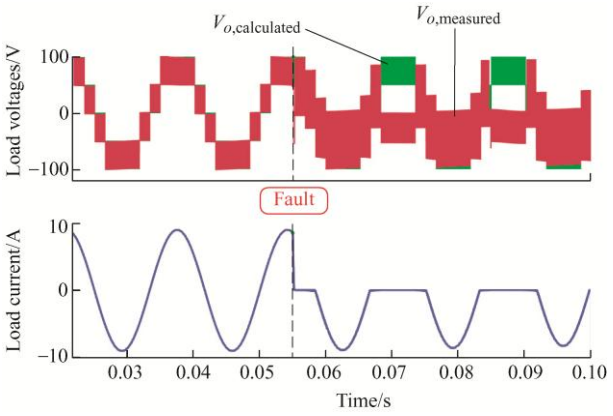
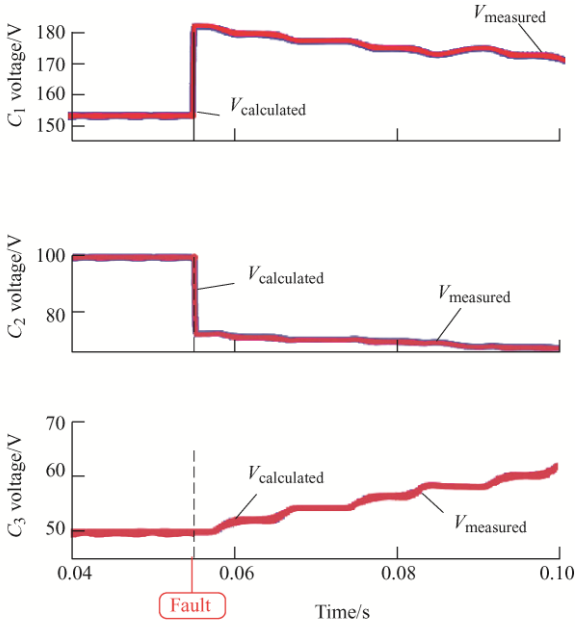


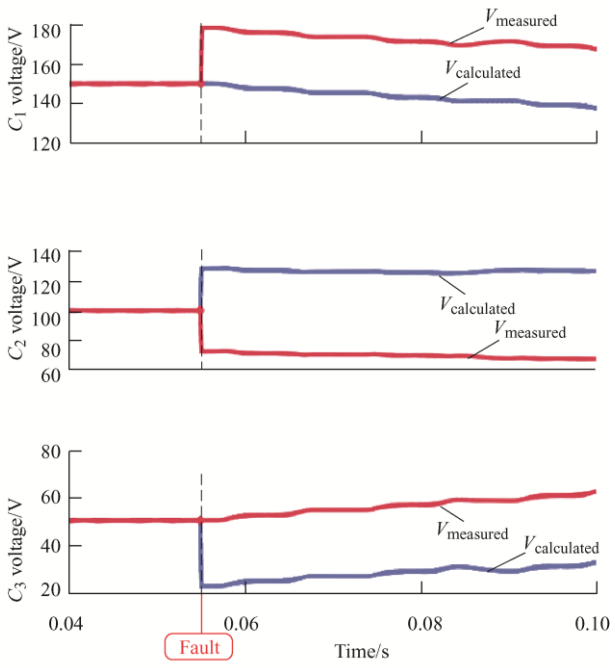
Fig. 8 Calculated/expected and the measured output voltages and load current

As discussed in the previous section, eight assumptions have been made for faulty switch in phase leg of the inverter, but only one of them is correct. The calculated and actual FC voltages for the correct (fault in S_2) and an incorrect (fault in S_3) assumptions are shown in Fig. 9. For a correct assumption, the calculated voltage across the FCs follows the actual values perfectly. However, there is error for an incorrect assumption, which will be the root-cause for a large error in output voltage calculations. The higher the capacitance of FCs, the more accurate will be the voltage calculations.

Finally, Fig. 10 shows the error signals in green and the minimum of all eight error signals in red. The minimum error is for S_2 which lasts for 5% of the fundamental cycle and confirms the fault for this



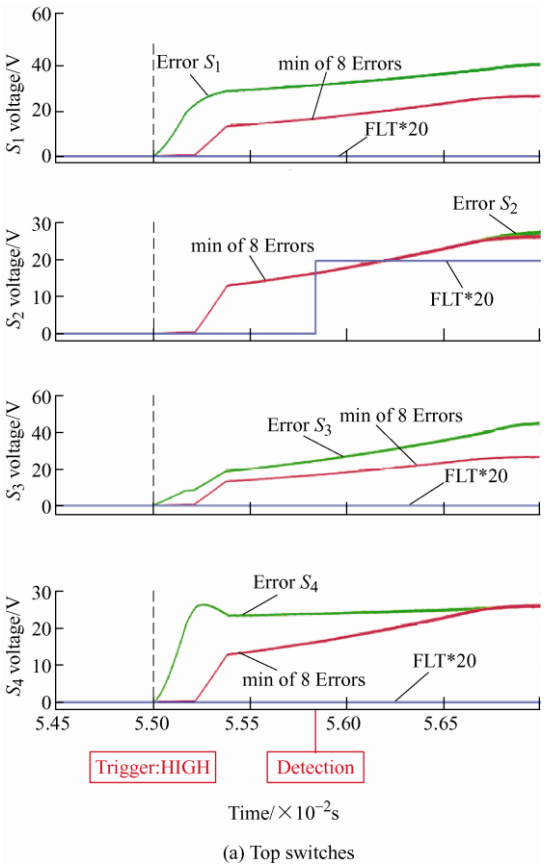
(a) Correct assumption: Fault in S_2



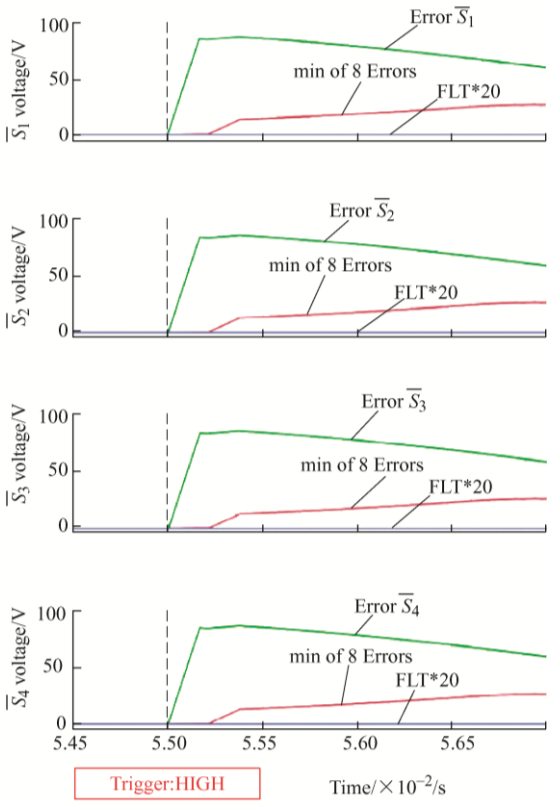
(b) Incorrect assumption: Fault in S_3

Fig. 9 FC voltage calculation

switch at t=55.83 ms. That is the time when fault signal, shown in blue, goes HIGH for S_2 in Fig. 10 to indicate that as a faulty switch.



(a) Top switches



(b) Bottom switches

Fig. 10 Comparing the error signals and detecting the minimum one as a faulty switch

5 Experimental verification

To verify the performance of proposed diagnostic strategy, a 5-Level FCML inverter prototype based on GaN transistors was designed and tested with the same parameters provided in Tab. 1. The inverter was configured with eight GaN MOSFETs with each rated at 650 V/60 A (Model No: GaN Systems GS66516B), and a digital signal processor TMS320F28379D was used in the setup to control the inverter. To emulate an OC fault in the test, the corresponding PWM signal of the switch under diagnosis was set to zero, but it was saved in another variable to carry out the diagnosis process. The experimental setup is shown in Fig. 11. The PSPWM method with an amplitude modulation index of 0.9 is used in the tests and the results are shown Figs. 12-15. The OC fault tests and analyses have been conducted for all the top switches. However, due to similarity and symmetry of the inverter topology, only part of these faults will be discussed here. Starting with S_3, as depicted in Fig. 12, the fault is applied at t=48 ms. Switch S_3 is not conducting any

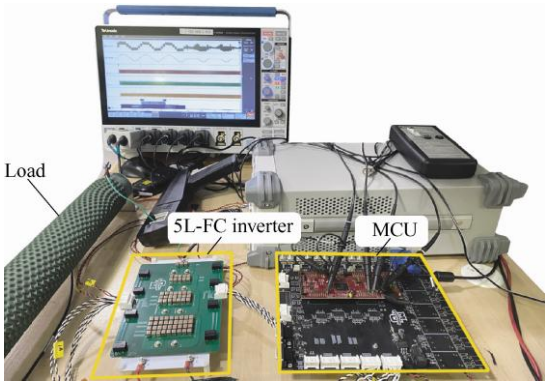


Fig. 11 Experimental setup of the GaN 5-level FCML inverter

current at that moment since the load current is in the negative half cycle. As soon as i_L crosses the zero to enter the positive half cycle, the output voltage becomes distorted and deviates from its expected value which enables the diagnosis process by setting the trigger signal to HIGH logic level. Zones Z_1 and Z_2, shown with blue in Fig. 12, are designating normal and faulty modes of the inverter. Zoom-in views of these zones are shown in Fig. 13. During the normal mode, the measured voltage follows the expected signal. Although there is some discrepancy between expected and actual waveforms, particularly in the falling or rising edges of the waveform, the trigger signal will remain LOW since the output of the moving average block used in Fig. 4 will not change with such instantaneous or negligible discrepancies. On the other hand, as illustrated in Fig. 13b, except some switching states which excludes the faulty device, the measured signal does not follow the reference. This will trigger the fault diagnosis algorithm. In addition, a detail illustration of output voltages for correct and incorrect assumptions are shown in dashed line in Figs. 13b and 13c. For a correct assumption of fault on S_3, the output voltage matches well with the measured waveform. However, the incorrect assumption of fault on S_1 results in a large discrepancy between the waveforms.

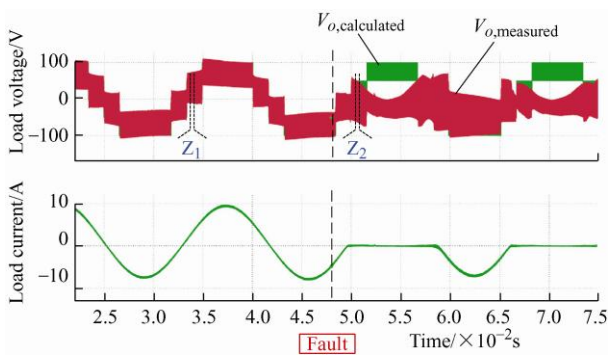


Fig. 12 Experimental results for a Fault in S_3)

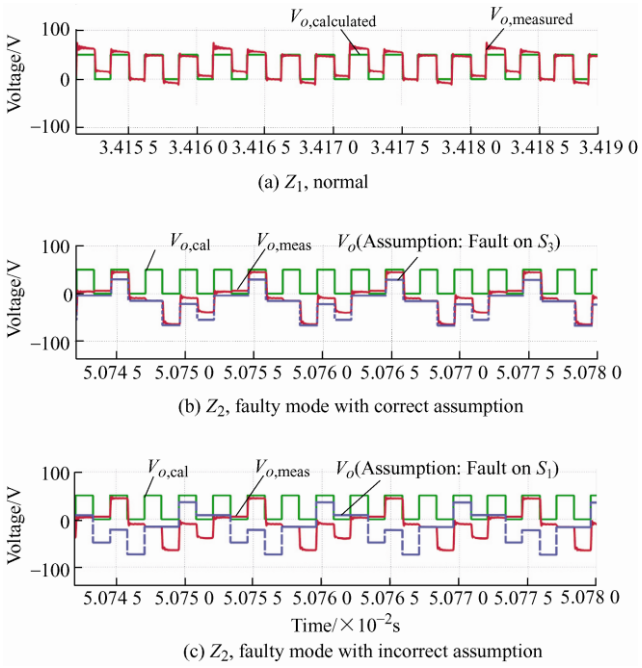


Fig. 13 Zoom-in view of the zones specified in Fig. 12

Fig. 14 shows the results of post-processing the data obtained from the OC fault on S_3. The output voltage starts to deviate from its reference value at t=50 ms, when the positive half-cycle starts. Trigger signal becomes HIGH at t=50.11 ms. Then, the comparison between error signals and the minimum

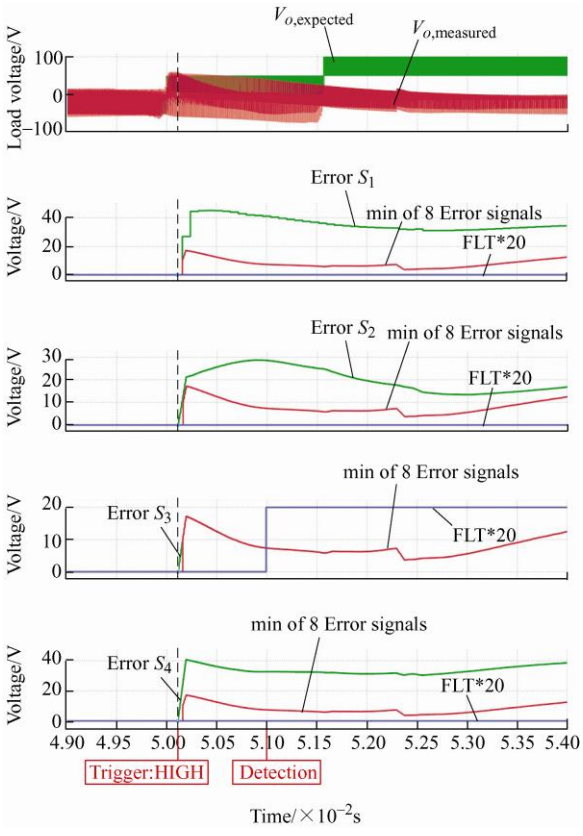


Fig. 14 Experimental verification for a fault in S_3; Load voltage, and error signals comparison

value among them begins. Observing the blue signal indicating the faulty switch in Fig. 14 reveals that the error signal for S_3 is minimum for the specified duration. Therefore, the algorithm ends up with detecting S_3 as a faulty switch at t=50.95 ms.

To demonstrate the effectiveness of the proposed method in diagnosing other switches, the fault in S_4 is investigated in Fig. 15 by providing the load voltage and error signals comparison. The fault is applied at t=48 ms and the trigger announces a fault at t=50.1 ms. Finally, the exact faulty switch is detected at t=51.03 ms, when the blue signal for S_4 becomes HIGH.

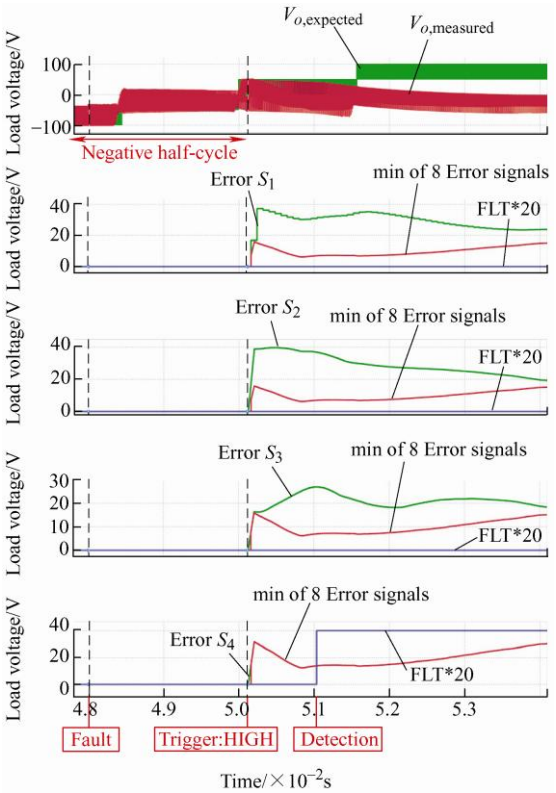


Fig. 15 Experimental verification for a fault in S_4; Load voltage and error signals comparison

To evaluate the robustness of the proposed method against load and modulation index variations, two sets of tests are conducted and the results are depicted in Figs. 16 and 17. The case with a high modulation index of m=0.9 is illustrated in Fig. 16 where, using a parallel load, the current is doubled at t=62 ms and stepped down to the previous value at t=165 ms. Then, an OC fault is applied on S_1 at t=240 ms. The measured output voltage remains almost the same during the load variations. Since the fault detection method is enabled by a trigger signal which uses output voltage waveform for comparison (Fig. 4), error signals remain unchanged until the time when trigger signal becomes HIGH. Nevertheless, after the fault, error signals start to increase and that of the S_1 is the minimum among other error signals. Consequently, the fault is detected at t=240.95 ms.

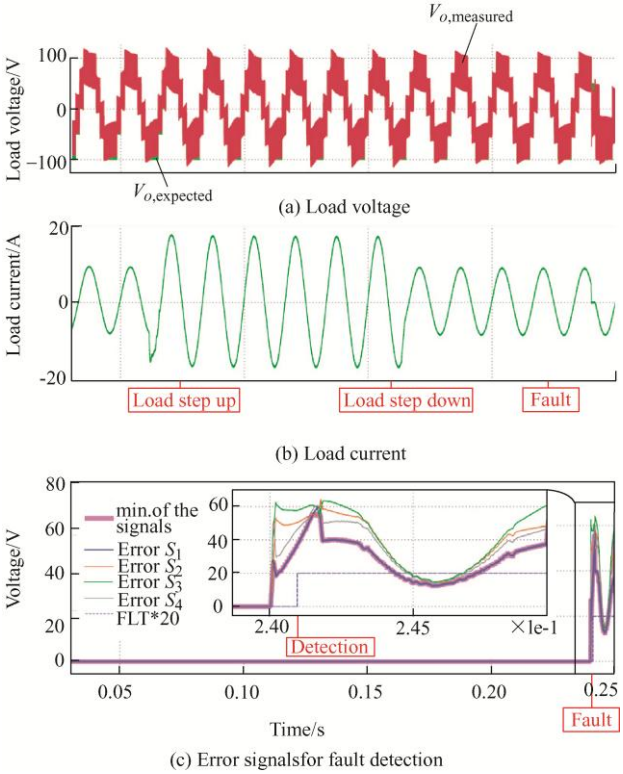


Fig. 16 Experimental verification of the robustness against load variation for a fault in S_1 and modulation index of 0.9

The second set of the robustness tests includes low modulation index of m=0.3 shown in Fig. 17,

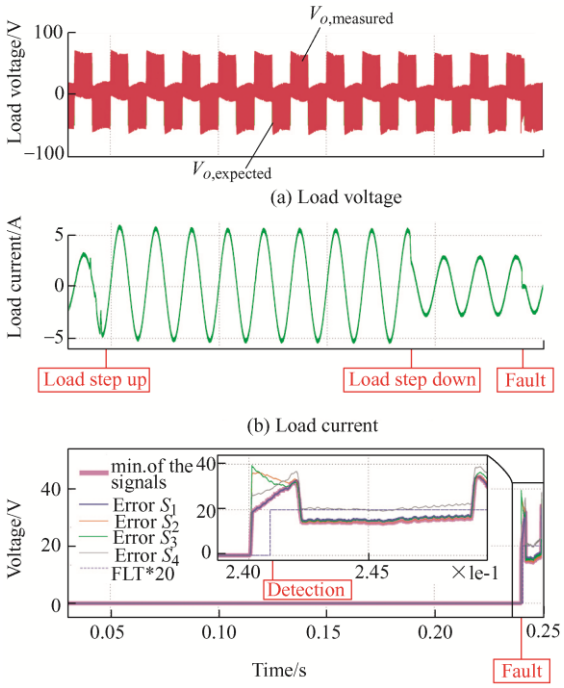


Fig. 17 Experimental verification of the robustness against load variation for a fault in S_1 and modulation index of 0.3

where the load voltage waveform has only three levels. The current is doubled at t=45 ms and stepped down to the previous value at t=188 ms. Afterwards, an OC fault is applied on S_1 at t=240 ms. Again, load variation does not affect the detection process and the fault is successfully detected at t=240.9 ms.

6 Conclusions

Flying capacitor multilevel converters have received increasing attention in recent years, and the emerging WBG devices enable higher switching frequency and accordingly high power density of such converters. However, the degraded hardware reliability due to the utilization of large number of semiconductor devices has been a major concern for these converters used in safety-critical applications such as electric vehicles or electric airplanes. In this paper, targeting at the open-circuit switching faults, an on-line low-cost fast diagnostic method is proposed, which can effectively detect and identify the faulty switches by fully leveraging the existing information of the converter, including the output voltage and current, as well as PWM signals. Simulation and experimental results have been presented to verify the efficacy and robustness of this proposed diagnostic method. By embedding such a diagnostic method in the system microcontrollers, downtime cost can be minimized and potential cascaded failures due to open-circuit switching faults can be avoided.

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