Switched-capacitor Multi-level Inverter with Equal Distribution of the Capacitors Discharging Phases*

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Abstract: A new switched-capacitor ($2n$+1) levels inverter with a single input source and equal charge of the capacitors at the input voltage V_{in} is presented. Compared with its peers from the same class of inverters, the proposed one features an equal or lower components count referred to the boost factor. And, it presents an additional advantage: each voltage level can be obtained by using different capacitors in the discharging phase, such that the decreasing part of the staircase output waveform can be synthesized with different switching topologies than those used in the increasing part. As a consequence, all the capacitors are discharged at the same voltage value at the end of each half-cycle, allowing for the use of smaller capacitors of equal values. When the capacitors are connected in parallel in the charging phase, there is no need to equalize their voltages, so no additional current spikes appear. This also implies less electromagnetic emission (EMI). Two types of modulation strategies are proposed. A half-height fundamental switching frequency modulation strategy allows for reaching the desired peak of the output voltage during the highest voltage level operation. It is advantageous in application of the inverter as a front end of a grid supplied by green sources of energy. A high frequency (f_s=200 kHz) modulation strategy accompanied by a duty-cycle control is advantageous for applications which require miniaturization. A 9-level switched-capacitor multi-level inverter (SCMLI) is analyzed and designed. The power losses are calculated. The experimental results for a 9-level inverter with V_{in}=40 V, V_{out}=110 Vrms 50 Hz, 200 W confirm the theoretical expectations.

Keywords: Switched-capacitor, multi-level inverter, half-height frequency modulation

1 Introduction

For a long time now, multi-level inverters MLI have been preferred at the front end of electrical grids or in other applications requiring an ac voltage obtained from a dc voltage source as they can provide a clean sinusoidal voltage, with a low total harmonic distortion (THD) without the need of a bulky output filter. The switched-capacitor (SC) multi-level inverters (MLI) took the place of the traditional multi-level inverters (neutral-point-clamped, flying-capacitor, cascaded H-bridge) due to their advantages: less capacitors, switches or input sources, automatic capacitor voltages balancing, capability of boosting the input voltage to a much higher output voltage [1]. They found multiple applications, from inverters for portable equipment to electrical vehicles and grid-tied inverters supplied by renewable sources. In grids supplied by green sources of energy, the boost factor of the SC inverters is essential, as the output voltage provided by the renewable energy cells is much lower than the peak of the desired grid voltage.

Since the first switched capacitor multi-level inverter (SCMLI) with full line and load regulation circuit published in 1998 [2], a lot of solutions have been proposed. Some of them were requiring single voltage sources, others multiple input sources. The advantage of the later is their need of less switches for getting the same number of levels, but they present the disadvantage of requiring sources providing outputs in

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exact voltage ratios. This is difficult to be achieved by photovoltaics or other green sources of energy. The line regulation of the multiple-source inverters is also problematic, as each source voltage can change independently at any moment due to unforeseeable climatic factors (insolation, etc.) [3-4]. Regardless of the number of input sources, two options exist for charging the capacitors in the switched-capacitor (SC) part: (a) either at equal voltage, by using a switching pattern of parallel/series connections of the capacitors or (b) at exponential or Fibonacci voltage ratios. The former method necessitates more components, but the switches are submitted at lower voltage stresses than in the later method.

Refs. [5-8] present different solutions of SC inverters supplied by a single input source in which the capacitors are charged at an equal voltage. A common drawback of these circuits is due to the no symmetry in the discharging process of the capacitors to the load: there are some capacitors that are discharged for synthesizing all the levels of the staircase output waveform, and other capacitors that are discharged just for realizing one voltage level [9-12]. As a result, either the capacitors in the first group have to be much oversized for diminishing their voltage ripple, or every capacitor finishes the discharging phase at a different voltage from the others [13-15]. The consequence of different capacitor voltage ripples is serious current spikes appearing then when the capacitors are reconnected in parallel for being charged from the input source in each half-switching cycle. These spikes affect the quality of the input current and lead to additional electromagnetic emission (EMI).

This paper proposes a new SCMLI with ($2n$+1) levels, supplied by a single voltage source in Section 2.1. It uses a generalized step-up switched-capacitor network with n cells, in which each capacitor is charged at the input voltage value. An advantage of the proposed solution is the possibility of achieving each level of the staircase output voltage by using different switching topologies. By combining in a different way these topologies for synthesizing the ascending and descending parts of the staircase waveform, the capacitors are discharged at the approximatively same value in each half-switching cycle, entering the charging phase from the same voltage. The proposed solution features a low components count relative to its highest level voltage (nV_{in}). Two modulation strategies are proposed in Section 2.2. Each one of the strategies is useful in certain types of applications. The theoretical analysis is presented in Section 3 for an inverter with 9 levels. The design of the capacitors and the analytical calculation of the losses allows for the theoretical calculation of the efficiency. The simulation and experimental results of Section 4 prove the expected advantages of the proposed inverter and the correctness of the theoretical formulation.

2 Proposed inverter and its switching topologies: Modulation strategy

2.1 Proposed SCML inverter

The proposed inverter is shown in Fig. 1, it consists of n SC cells and an output bridge. The first and last cells contain a capacitor and two switches, the other cells are formed by a capacitor and three switches.

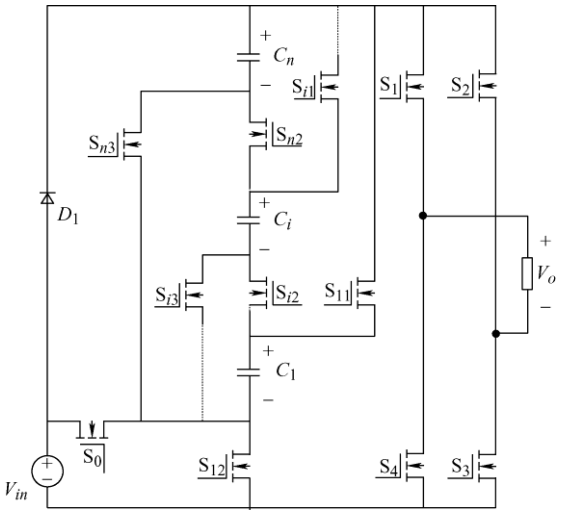
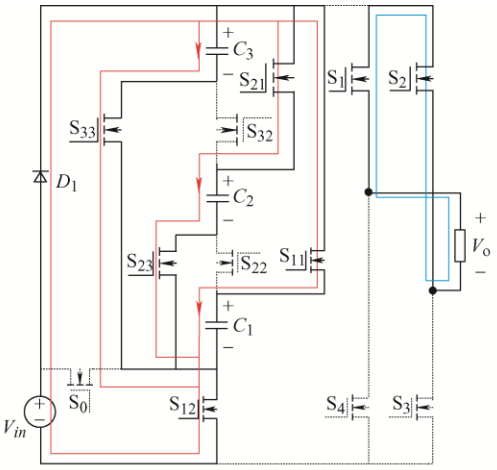


Fig. 1 Proposed ($2n$+1) levels SC inverter

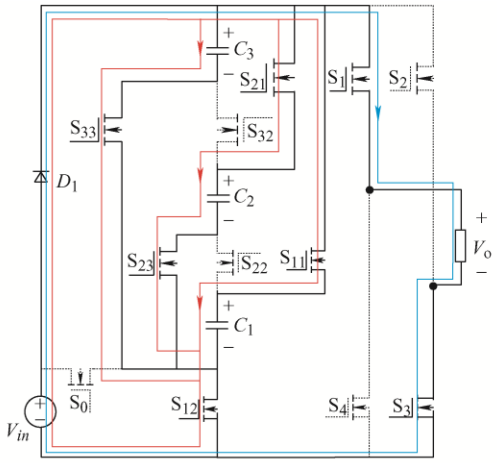
Its detailed operation is shown for a particular case where n=4. The switching topologies for creating the positive part of the staircase (levels 0, V_{in}, $2V_{in}$, $3V_{in}$ and $4V_{in}$) are shown in Fig. 2. In these cases, the output current flows through the bridge switches S_1 and S_3, the other two switches of the bridge are submitted to the load voltage corresponding to the

synthesized level. Similar topologies are used for getting the negative voltage levels, just that the other two switches of the output bridge, S_2 and S_4, are used.

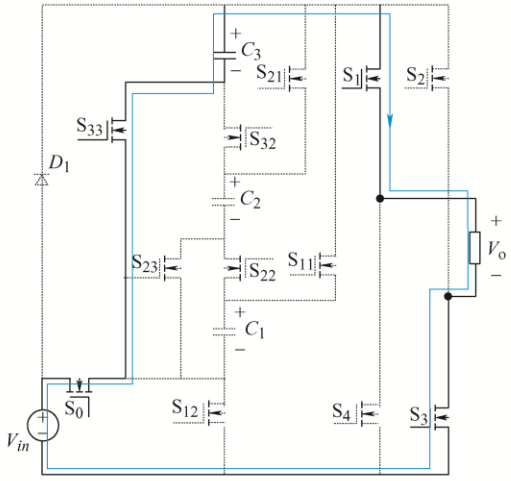
According to Fig. 2a, the capacitors are charged in parallel from the input source. One gets the level 0 of the output voltage.



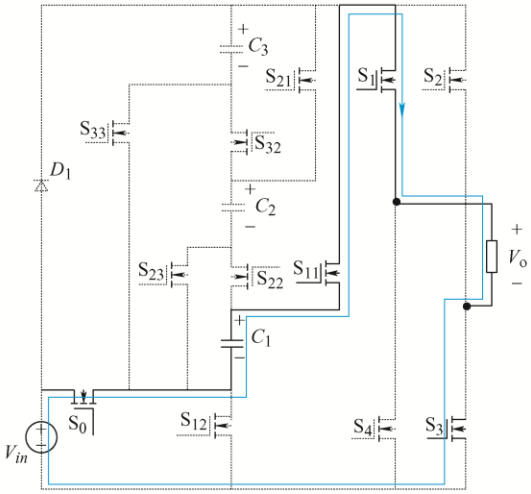
(a) V_o=0



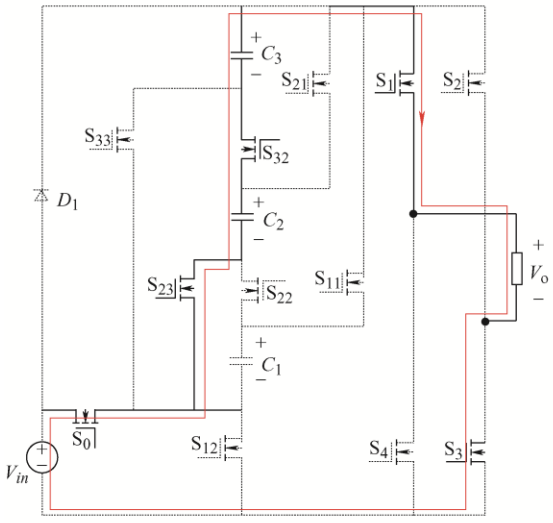
(b) V_o=V_{in}



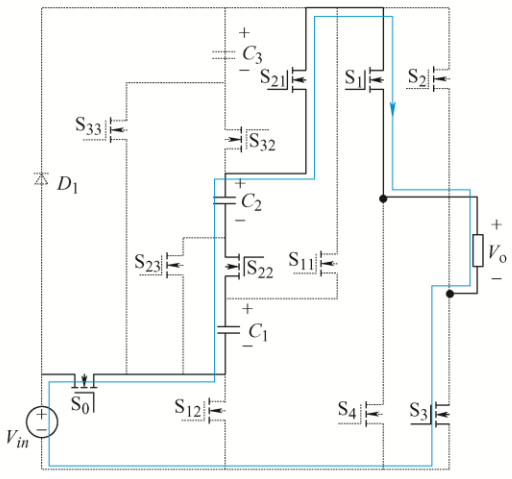
(c) V_o=2$V_{in}C_3$



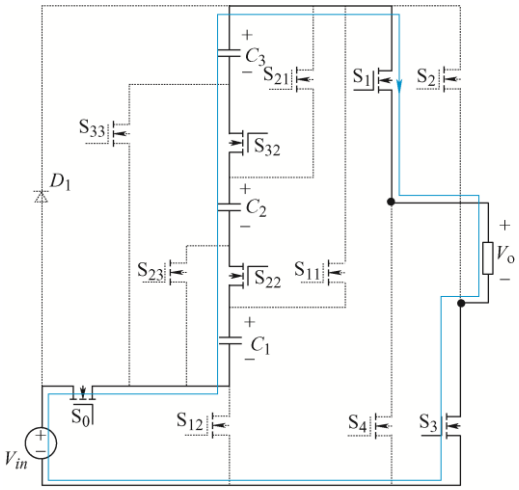
(d) V_o=2$V_{in}C_1$



(e) V_o=3$V_{in}C_2$,C_3



(f) V_o=3$V_{in}C_1$,C_2



(g) $V_o=4V_{in}$

Fig. 2 Switching topologies for synthesizing the voltage levels for the 9-level inverter

The parallel charging of the capacitors continues when synthesizing the output voltage level V_{in} , just that the input source also transfers energy to the load (Fig. 2b). During this mode, the voltage on each capacitor reaches $V_{in}-V_F$, with V_F denoting the forward voltage of the diode D_1.

The charging process of the capacitors is stopped when synthesizing the higher levels of the output voltage. According to Fig. 2c and Fig. 2d, there are two different topologies for creating the output voltage level $2V_{in}$: either the input source in series with capacitor C_1 are discharged to the load, with C_2 and C_3 keeping their initial voltage V_{in}, or the input source in series with capacitor C_3 are discharged to the load, with C_1 and C_2 holding their voltage at V_{in}.

The output voltage level $3V_{in}$ is obtained according to one of the topologies shown in Fig. 2e and Fig. 2f. In Fig. 2e, the input source in series with capacitors C_2 and C_3 are discharged to the load, with C_1 holding its voltage attained at the end of the previous topology which was shown in Fig. 2c. In Fig. 2f, the input source in series with capacitors C_1 and C_2 are discharged to the load, with C_3 holding its previously attained voltage.

To obtain the output voltage $4V_{in}$, the input source in series with all the capacitors are discharged to the load (Fig. 2g).

As it will be seen when discussing the modulation strategy, when approximating a sinusoid waveform with a staircase one, the time durations of the levels are not equal. As a result, if one would use only the switching topologies given by either Fig. 2a, 2b, 2c, 2e, 2g or only those given by Fig. 2a, 2b, 2d, 2f, 2g, the capacitors will be discharge in the end at different voltage values, meaning that they would start the next switching cycle from different initial conditions. When connected in parallel for being charged at the beginning of each half switching cycle, inner current pulses would appear for equalizing firstly their voltages. However, the proposed inverter in Fig. 1 allows for different options of discharging the capacitors. In the case of the considered example (9 levels inverter), the topologies in Fig. 2a, 2b, 2c, 2e, 2g will be followed for synthesizing the ascending part of the half sinusoid, and the topologies of Fig. 2a, 2b, 2d, 2f, 2g for getting the descending part of the half sinusoid. It has to be noted that in each half switching cycle, there are two time intervals in which the level $2V_{in}$ is reached and two time intervals in which the level $3V_{in}$ is reached, but only one interval in which the level $4V_{in}$ is reached. At the end of each half switching cycle, in the proposed MLI, all the capacitors will be discharged at almost similar voltage values.

In the 9-level inverter, for creating each of the levels $2V_{in}$ and $3V_{in}$, two different discharging paths could be followed. A larger variety of options for synthesizing each level is available if the proposed inverter is designed with a larger n.

Therefore, the first advantage of the operation described for the proposed inverter is that there is no need of equalizing the capacitor voltages at the

beginning of each switching cycle, so no inner current spikes appear in such a purpose. One more positive consequence of less current spikes is the reduction in the electromagnetic emission (EMI).

In Tab. 1, the proposed inverter is compared to other inverters with a single input source and with capacitors charged at equal voltage [2, 5-11]. For all the compared inverters, the boost factor (i.e. the ratio between the highest output voltage level nV_{in} and the input voltage) is the same: n. The last two columns refer to an element very influential on the total conduction loss: how many active and passive switches are actually turned-on in each operating circuit? Looking to all the charging capacitors loops, in which one of them there are more switches in conduction? The maximum number is shown in the fifth column of Tab. 1. And considering the equivalent networks in which the nonzero voltage levels are synthesized, in which one of them there are more switches actually in conduction? The maximum number is given in the last column of Tab. 1. The total components (capacitors, active and passive switches) count referred to the highest voltage level for the proposed converter is similar to that of the best available solutions.

Tab. 1 Comparison of SCML inverters with a single input source and equal charge of each capacitor at V_{in}

Paper No.	Active and passive switches No.	Level No.	Cap. No.	Number of charging circuit switches	Number of discharging circuit switches
Ref. [1]	$4n-1$	$2n+1$	$n-1$	3	$n+4$
Ref. [2]	$3n+1$	$2n+1$	$n-1$	n	$n+1$
Ref. [5]	$3n+1$	$2n+1$	$n-1$	$n-2$	$n+1$
Ref. [6] half cell	$6n-2$	$2n+1$	$2n-2$	$2n-2$	$2n$
Ref. [6] full cell	$6n-2$	$2n+1$	$n-1$	$4n-4$	$n+1$
Ref. [7]	$3n+2$	$2n+1$	$n-1$	3	$n+1$
Ref. [8]	$5n-1$	$2n+1$	$n-1$	3	$2n$
Ref. [9]	$6n-2$	$2n+1$	$n-1$	$4n-4$	$2n$
Ref. [10]	$5n+2$	$2n+1$	n	$2n+1$	$2n$
Ref. [11]	$3n+5$	$2n+1$	$n-1$	$2n+1$	$2n$
Proposed topology	$3n+1$	$2n+1$	$n-1$	4	$n+1$

The solution in Refs. [12, 16] makes use of a step-down SC cell, in which the capacitors are charged in series, the resulting boost factor is much smaller for the same components count. The capacitors in the solutions Refs. [13-14] are also charged in series, resulting in a maximum of the highest level boost factor of $nV_{in}/2$ or even smaller, this is why the Refs. [12-14] are not included in the comparison.

2.2 Modulation strategy

2.2.1 Low frequency modulation

As typically in MLI, the desired output voltage sinusoid is approximated by a staircase waveform [17-18]. By increasing the number of levels, a better approximation of the sinusoid is obtained, but at the cost of increasing the components count. The designer has always to trade-off the quality of the output waveform with the cost and efficiency of the inverter.

A half-height fundamental frequency f modulation strategy is chosen, as then the highest voltage level can give the sinusoidal output peak(Fig. 3). Frequency f is that of the synthesized output voltage. For example, in applications supplying the national electric grid, f=50 Hz. Accordingly, for the N=9 levels inverter, the transitions times defining the operation of the circuit for creating each voltage level are calculated as

$$t_i = \frac{1}{2\pi f}\arcsin\left(\frac{2i-1}{N-1}\right) \quad i=1,\cdots,4 \tag{1}$$

resulting in the values (with t_5–t_8 calculated by symmetry relative to $T/4$, $T=1/f$)

$$t_1 = 3.99\times10^{-4}\ \text{ms};\quad t_2 = 1.22\times10^{-3}\ \text{ms};$$
$$t_3 = 2.15\times10^{-3}\ \text{ms};\quad t_4 = 3.39\times10^{-3}\ \text{ms};$$
$$t_5 = 6.6\times10^{-3}\ \text{ms};\quad t_6 = 7.85\times10^{-3}\ \text{ms};$$
$$t_7 = 8.78\times10^{-3}\ \text{ms};\quad t_8 = 9.6\times10^{-3}\ \text{ms};$$
$$t_9 = \frac{T}{2} = 0.01\ \ \text{ms}$$

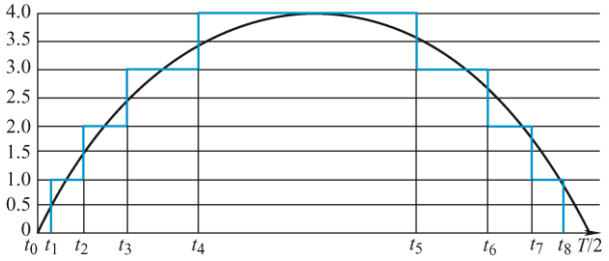


Fig. 3 Half-height fundamental frequency modulation strategy for getting the levels: 0, V_{in}, $2V_{in}$, $3V_{in}$, $4V_{in}$ (similar for the negative half-sinusoid)

2.2.2 High frequency modulation

A high frequency (f_s=200 kHz) modulation accompanied by a duty-cycle control is proposed for getting an output voltage of frequency f. Fig. 3 and the transition times calculated above are still valid, just that, for creating each output voltage level, a cyclically switching operation with the frequency f_s is implemented.

Similar to the inverter presented in Ref. [2], two identical SC sub-circuits are used for getting a DC-DC behavior when synthesizing each output voltage level. The two SC cells operate with a half-switching period symmetry. Each cell consists of the original structure proposed in Fig. 1.

In each half switching cycle $T_s/2$ (T_s=1/f_s), the first SC network capacitors are charged in parallel from the source during the first t_{on}(=DT_s) interval [0, DT_s]. During this time, several flying capacitors belonging to the second SC network, depending on which level has to be synthesized, in series with the input source are discharged to the load. In the second time interval [DT_s, T_s/2], the capacitors belonging to the first SC cell are disconnected from the input voltage, remaining at the charge level attained at the instant DT_s, but the capacitors of the second SC cell in series with the input voltage continue their discharging to the load. The two SC cells interchange their role in the second half-cycle. In the second t_{on} interval [T_s/2, T_s/2+DT_s], the capacitors of the second SC cell enter a charging process, that is discontinued at the instant T_s/2+DT_s, remaining so until the end of the cycle. During all the time duration [T_s/2, T_s] those capacitors of the first SC cell needed to synthesize the desired voltage level, in series with the input voltage, are discharged on the load. The equivalent switching topologies for synthesizing each voltage level are the same as shown in Fig. 2, just that a high number of switching cycles are necessary for creating each level of the output staircase, as T_s is much smaller than T, or than any time interval discussed in Fig. 3.

The nominal duty-cycle D is calculated for getting the output sinusoidal peak of 155 V at the nominal input voltage. As in DC-DC SC converters, for the nominal line and load values, the capacitors are designed such that they don't reach saturation in the interval t_{on}. For a good line regulation, it is preferred to have the nominal operating point in the middle of the linear part of the charging capacitor voltage characteristic. With a simple PWM control, typical for SC converters, the duty-cycle will be increased (respectively decreased) if the input voltage drops (respectively raises) below(over) its nominal value. A fast line regulation is assured, as the controller reacts promptly to any input voltage variation. Similarly, for regulating a load variation.

This strategy cannot be applied in applications where the input source requires a non-pulsating input current, but it is very advantageous in applications requiring miniaturization. Due to the extreme minimal time durations in which the capacitors are discharged in each switching cycle, the calculation of the capacitors values for the same voltage ripples as considered in the preceding low frequency modulation will result in capacitors of a few μF order. A high power density is thus obtained (even if the numbers of the components is doubled), contrary to all the inverters based on a fundamental frequency modulation in which the capacitors, of several mF value, are the bulky part of the circuit.

3 Design of the 9-level inverter with fundamental switching frequency modulation: Calculation of the losses

3.1 Design of the capacitors

According to the switching pattern described in Section 1, the capacitors feature three discharging periods in each half-cycle

C_1: t_2-t_3 t_4-t_5 t_5-t_6

C_2: t_3-t_4 t_4-t_5 t_5-t_6

C_3: t_3-t_4 t_4-t_5 t_6-t_7

allowing to express the capacitor voltage ripples ΔV_{C_k}, k=1, 2, 3 as follows

$$\Delta V_{C_1}=\frac{1}{2\pi fC_1}\left[\int_{\theta_2}^{\theta_3} i_{C_1}\mathrm{d}(\omega t)+\int_{\theta_4}^{\pi-\theta_3} i_{C_1}\mathrm{d}(\omega t)\right]=$$

$$\frac{1}{2\pi fC_1}\left[\int_{\theta_2}^{\theta_3} i_o\mathrm{d}(\omega t)+\int_{\theta_4}^{\pi-\theta_3} i_o\mathrm{d}(\omega t)\right] \quad (2)$$

$$\Delta V_{C_2}=\frac{1}{2\pi fC_2}\int_{\theta_3}^{\pi-\theta_3} i_{C_2}\mathrm{d}(\omega t)=$$

$$\frac{1}{2\pi fC_2}\int_{\theta_3}^{\pi-\theta_3} i_o\mathrm{d}(\omega t) \quad (3)$$

$$\Delta V_{C_3}=\frac{1}{2\pi fC_3}\left[\int_{\theta_3}^{\pi-\theta_4} i_{C_3}\mathrm{d}(\omega t)+\int_{\pi-\theta_3}^{\pi-\theta_2} i_{C_3}\mathrm{d}(\omega t)\right]=\frac{1}{2\pi fC_3}\left[\int_{\theta_3}^{\pi-\theta_4} i_o\mathrm{d}(\omega t)+\int_{\pi-\theta_3}^{\pi-\theta_2} i_o\mathrm{d}(\omega t)\right] \quad (4)$$

where f is the fundamental switching frequency, $\theta_i=2\pi ft_i$, i=1,2,3,4, and i_o is the output current, resulting in

$$\Delta V_{C_1}=\Delta V_{C_2}=\Delta V_{C_3}=2.8\ \text{V}$$

It can be noted that the interval [t_4-t_5] is slightly longer than the other intervals, this is why theoretically ΔV_{C_2} is slightly larger than the voltage ripples on the other two capacitors, but the influence on the practical results is insignificant. In the above equations, the output current is different in each discharging circuit corresponding to the synthesis of each output voltage level ($2V_{in}$, $3V_{in}$, and $4V_{in}$).

Imposing a capacitor voltage ripple of 7.5% of its maximum voltage, one gets equal capacitor values, what is another advantage of the proposed inverter. Accordingly, it has been chosen C_1=C_2=C_3=4 700 μF.

3.2 Calculation of the power losses and theoretical efficiency

The conduction and switching losses are calculated according to the procedure and equations of Ref. [19].

In the following equations, V_F represents the forward voltage drop of diode D_1, r_T is the on-resistance of S_0, S_{12}, $S_{21\text{-}23}$, S_{32}, $r_{T'}$ is the on-resistance of S_{11}, S_{33}, r_Q is the on-resistance of $S_{1\text{-}4}$, r_C is the equivalent series resistance of each capacitor C_k, k= 1,2,3, R is the resistance of the load. Their values are given in Tab. 2. The power losses are calculated accordingly.

(1) Power loss due to the capacitor charging process. As, in each cycle, all the capacitors are charged in parallel from the input source when getting the levels of voltage 0 and V_{in} in the staircase output voltage, the corresponding power loss for the three floating capacitors can be expressed as

$$P_{loss-ch}=2f\sum_{k=1}^{3}\Delta E_{C_k}=8.76\ \text{W} \quad (5)$$

where $\Delta E_{C_k}=C_k\Delta V_{C_k}V_F+C_k\Delta V_{C_k}^2$ k=1,2,3.

(2) Conduction power loss in the parasitic resistances during the time durations corresponding to the levels $\pm V_{in}$ in the staircase output waveform, when the input source energy is also transferred to the load

$$P_{loss-disch1}=4f\frac{\theta_2-\theta_1}{2\pi f}\left[2r_Q\left(\frac{V_{in}-V_F}{R+2r_Q}\right)^2+V_F\left(\frac{V_{in}-V_F}{R+2r_Q}\right)\right]=0.108\ \text{W} \quad (6)$$

(3) Conduction power loss in the parasitic resistances during the time durations corresponding to the levels $\pm 2V_{in}$, $\pm 3V_{in}$, respectively $\pm 4V_{in}$, (the discharging phase of the capacitors)

$$P_{loss-disch2}=(4\Delta E_{d1}+4\Delta E_{d2}+2\Delta E_{d3})=1.14\ \text{W} \quad (7)$$

where

$$\Delta E_{d1}=I_1^2r_1\frac{\theta_3-\theta_2}{2\pi f}=\left(\frac{2V_{in}}{R+r_1}\right)^2 r_1\frac{\theta_3-\theta_2}{2\pi f}$$

$$r_1=r_C+r_T+r_{T'}+2\times r_Q$$

$$\Delta E_{d2}=I_2^2r_2\frac{\theta_4-\theta_3}{2\pi f}=\left(\frac{3V_{in}}{R+r_2}\right)^2 r_2\frac{\theta_4-\theta_3}{2\pi f}$$

$$r_2=2\times r_C+3r_T+2\times r_Q$$

$$\Delta E_{d3}=I_3^2r_3\frac{\pi-2\theta_4}{2\pi f}=\left(\frac{4V_{in}}{R+r_1}\right)^2 r_3\frac{\pi-2\theta_4}{2\pi f}$$

$$r_2=3\times r_C+3r_T+2\times r_Q$$

where I_1, I_2 and I_3 are the currents in the discharging capacitors loops corresponding to the synthesized level.

(4) Switching losses accompanying each turn-on and turn-off of each switch i (N_{switch} denotes the number of the switches)

$$P_{sw-total}=\sum_{i=1}^{N_{switch}}\left[\sum_{j=1}^{N_{(i)}}P_{sw,on(ij)}+\sum_{j=1}^{N_{(i)}}P_{sw,off(ij)}\right]=0.003\,4\ \text{W} \quad (8)$$

where $P_{sw,on(ij)}$ represents the switching power loss at the j-th turn-on of switch i in a cycle, and $P_{sw,off(ij)}$ represents the switching loss of the same switch at its turn-off. With $N(i)$ denoting the number of turns-on (or off) of switch i in a switching cycle (i.e. j= 1, 2,⋯, $N(i)$) ,$V_{off-stage(ij)}$ the off-state voltage of switch i after a turning-off action j, $I_{on-stage1,(ij)}$ the current through switch i after a turning-on action j, and $I_{on-stage2,(ij)}$ the current through switch i before a turning-off action j, the expressions in the previous equation are calculated with the formulas

$$P_{sw,on(ij)}=\frac{1}{6}fV_{off-stage(ij)}I_{on-stage1,(ij)}t_{on} \quad (9)$$

$$P_{sw,off(ij)} = \frac{1}{6} f V_{off-stage(ij)} I_{on-stage2,(ij)} t_{off} \quad (10)$$

According to the above calculations, the total power loss results as 10.01 W, giving a theoretical efficiency of 95.2 %.

4 Simulation and experimental results for the 9-level inverter

The components specifications are given in Tab. 2.

Tab. 2 Components specifications

Component	Model and DC resistance
Electrolytic capacitor C_1, C_2, C_3	4 700 μF, r_C= 0.12 Ω
N-channel MOSFET S_1, S_2, S_3, S_4	IRFB4332PBF, r_Q= 0.033 Ω
N-channel MOSFET S_{11}, S_{33}	IRF3415PBF, r_T= 0.042 Ω
N-channel MOSFET S_0, S_{12}, S_{21}, S_{22}, S_{23}, S_{32}	IPP093N06N3G, r_T= 0.009 3 Ω
Schottky diode D_1	MBR40250TG, V_F = 0.97 V

Fig. 4 gives the simulated waveforms of the input and staircase output voltages, and capacitor voltages for the inverter designed for V_{in}=40 V, P_{out}=200 W. The frequency of the output voltage is 50 Hz. It can be noticed that all the capacitors start each charging phase from the same voltage. According to the graphs, the capacitors voltage ripples are almost equal: $\Delta V_c = 2.65$ V.

The inverter was implemented in the laboratory by using the components given in Tab. 2. (As in Refs. [11, 20], a choke paralleled to a freewheeling diode can be added in the input circuit to assure a non-pulsating input current, as required when green sources of energy are the front end of the system (Fig. 5). The experimental results on the prototype described in Fig. 2 and Tab. 2 are shown in Fig. 6.

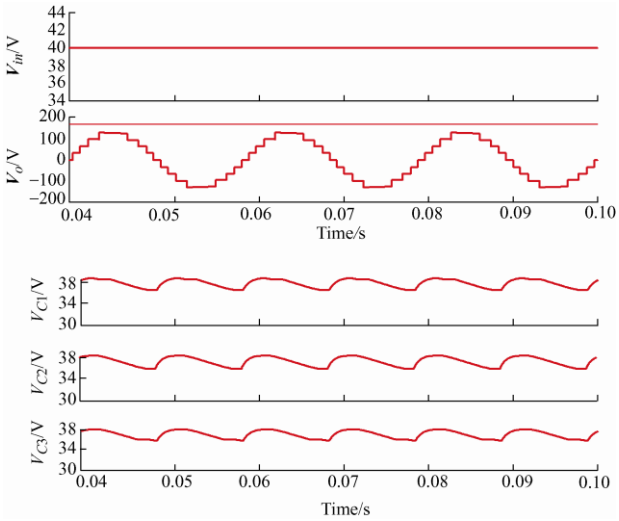


Fig. 4 Simulation results (V_{in}, V_o, V_{C1}, V_{C2}, V_{C3})

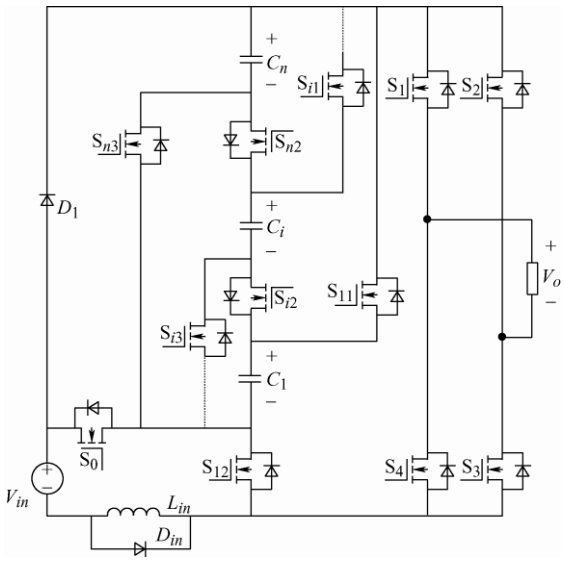
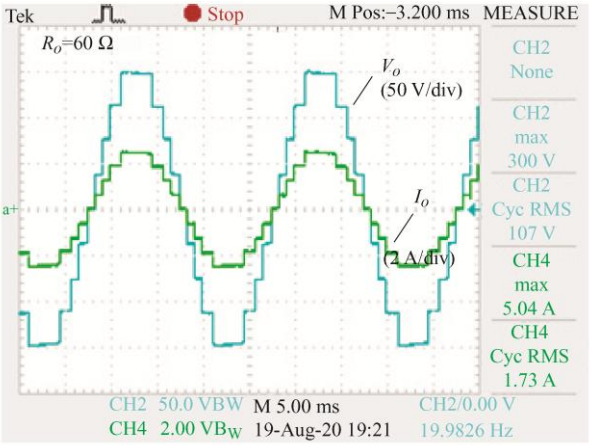
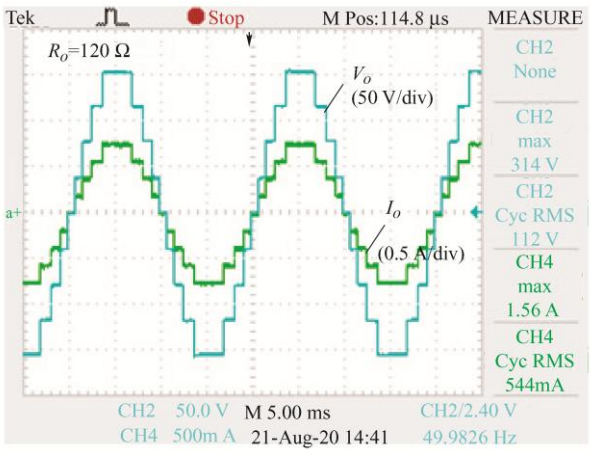


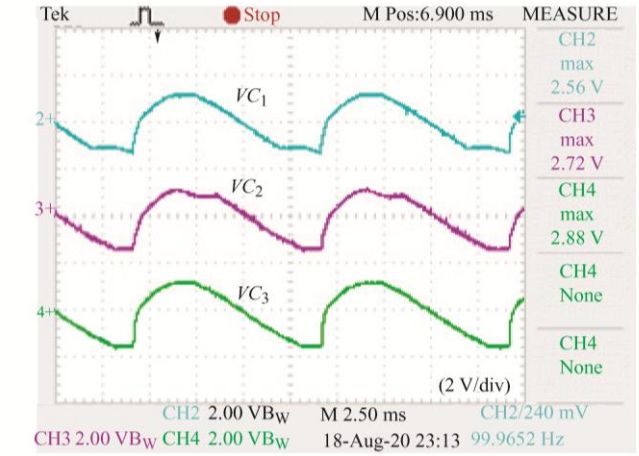
Fig. 5 Diagram of the inverter prototype with an inserted choke as in Ref. [9]



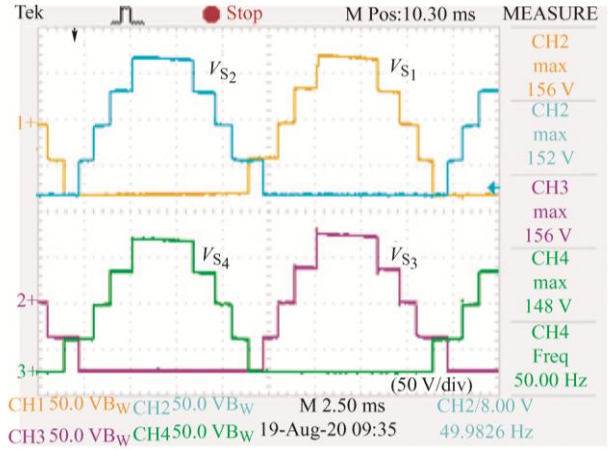
(a) Output volage and currcnt for V_{in}=40 V, R=60 Ω



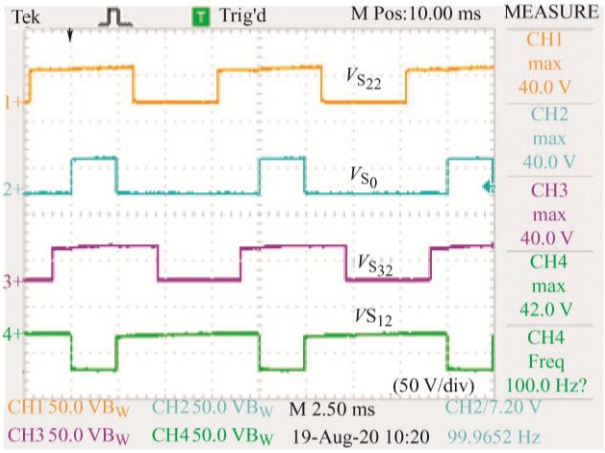
(b) Output volage and currcnt for V_{in}=40 V, R=200 Ω



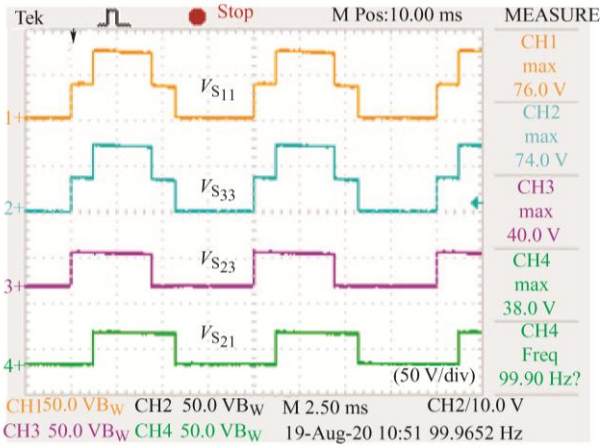
(c) Capacitor volages for V_{in}=40 V, R=60 Ω



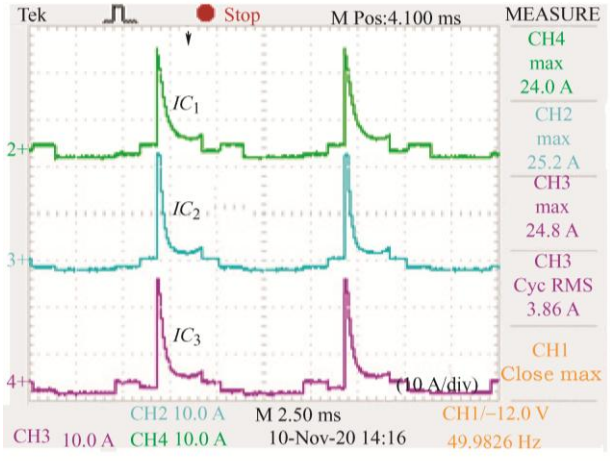
(d) Voltages stresses V_{ds} on the output bridge switches S_1, S_2, S_3, S_4



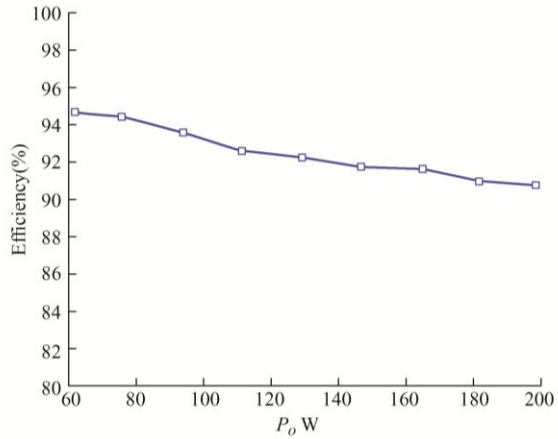
(e) Voltage stresses V_{ds} for S_{22}, S_0, S_{32}, S_{12}



(f) Voltage stresses V_{ds} on S_{11}, S_{33}, S_{23}, S_{21}



(g) Capacitor currents



(h) Efficiency versus power value

Fig. 6 Experimental waveforms

The experimental results are in a good agreement with the theory. A 9-level inverter gives a staircase waveform very close to a sinusoid. The measured Total Harmonic Distortion THD is only 8.18%, what is an advantage of the chosen half-height fundamental frequency modulation strategy. The voltage of the highest voltage level of the output staircase is 154.5 V, corresponding to the desired rms value of 110 Vrms, typical for some electrical grids. The capacitors voltage ripples are practically equal, as it was expected in the

theoretical explanations of Section 1. The measured efficiency (Fig. 6h) is between 91.51% at high power to 94.4% at low powers, when the values of the input voltage and output voltage were kept constant.

5 Conclusions

A new SCMLI proved to be advantageous by allowing an equal voltage ripple for all the flying capacitors, what lead to a lack of voltage equalizing-purposed current spikes when the capacitors are connected in parallel for being charged. The components count referred to the staircase highest level voltage is kept at minimum, contributing to a good energy efficiency. A half-height fundamental frequency modulation resulted in an output waveform with a low harmonic distortion. The experimental results confirmed the expected good features of the proposed inverter and its suitability for supplying electrical grids from dc solar or other green energy cells. An efficiency of 91.5% was measured at the nominal load.

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