A Double Input-parallel-output-series Hybrid Switched-capacitor Boost Converter

Jianfei Chen[1*], *Kewei Ding*[1], *Yulin Zhong*[2], *Fujin Deng*[3] and *Sayed Abulanwar*[4]
(1. Department of Electrical and Computer Engineering, Wayne State University, Michigan 48202, USA;
2. Broad-Ocean Technologies, Novi, Michigan 30120, USA;
3. School of Electrical Engineering, Southeast University, Nanjing 210096, China;
4. Electrical Engineering Department, Mansoura University, Mansoura 35516, Egypt)

Abstract: A double input-parallel-output-series hybrid switched-capacitor boost (DIPOS-HSCB) converter is proposed which consists of two different kinds of input-parallel-output-series (IPOS) circuits, i.e., inner IPOS circuit and outer IPOS circuit. Two boost modules and one switched-capacitor network build an inner IPOS circuit based IPOS-HSCB converter and two IPOS-HSCB converters develop the outer IPOS circuit based DIPOS-HSCB converter. With the proposed DIPOS-HSCB converter, a high voltage-gain with low component stress and small input current ripple are achieved. Furthermore, an automatic current balancing function for all input inductor currents can be also achieved using a special carrier phase-shifted modulation scheme. A prototype rated at 200 V/120 W has been developed and the maximum efficiency of the proposed DIPOS-HSCB converter is 95% at 120 W. Both steady and dynamic results are presented to validate the effectiveness of the proposed DIPOS-HSCB converter.

Keywords: IPOS, switched-capacitor, boost converter, phase-shifted modulation, automatic current balancing

1 Introduction

Multilevel step-up DC-DC converters have caught increasing interest and been used in many applications, such as wind farms [1-3], solar power generation systems [4-6], large-scale grid-connected fuel cell systems [7-11], high-power charging stations for electric vehicles [12-13], and DC grids [14-16]. In these systems, a multilevel step-up DC-DC converter can be employed to regulate a varying low-level input voltage to a stable high-level voltage and to provide a required DC link voltage for the backend inverter. One of the challenges facing such systems is how to attain a high voltage-gain, low component stresses, and small ripples with a simple topology. Several multilevel step-up DC-DC converters have been proposed during the past decade. As one of the non-isolated multilevel step-up DC-DC converters, the conventional three-level Boost converter was firstly proposed and then adopted to combine with a three-level diode-clamped inverter to achieve a medium voltage and high power output [2-3, 5]. Owing to the interleaved modulation scheme, small input current ripples and low component stresses could be achieved in this kind of multilevel Boost converters. In addition, a flying-capacitor based three-level Boost converter was proposed in Ref. [11] with better dynamic response than the conventional three-level Boost converter. However, similar to the Boost converters previously discussed, the flying-capacitor based three-level Boost converter faces an inherent limitation: the voltage gain is limited to be no more than $1/(1-d)$, where d is the duty cycle. In addition, this converter requires a complicated control scheme to balance the flying-capacitor voltage. Another flying-capacitor based three-level Boost converter with an intrinsic voltage doubler was presented in Refs. [17-18]. In addition to the advantages of the topology in Ref. [11], the two input inductor currents of the converter in Refs. [17-18] could be self-balanced due to the flying-capacitor. Moreover, the voltage gain of this converter is increased to be $2/(1-d)$ instead of $1/(1-d)$ when the duty cycle d is over 0.5. However, the voltage stresses across the output diode and the output capacitor are identical to the output voltage, which is a big disadvantage. Ref. [19] proposed an improved converter by adding one more flying-capacitor and one more diode to form a symmetrical flying-capacitor based topology, which helps decrease voltage stresses across the output diodes by half of its

Manuscript received October 11, 2020; revised November 13, 2020; accepted December 1, 2020. Date of publication December 31, 2020; date of current version December 8, 2020.
* Corresponding Author, E-mail: cjf6221@gmail.com
Digital Object Identifier: 10.23919/CJEE.2020.000027

output voltage. However, one more diode and one more capacitor are necessary; and more importantly, the voltage stresses across the other diodes become higher although the voltage stresses across the output diodes are decreased.

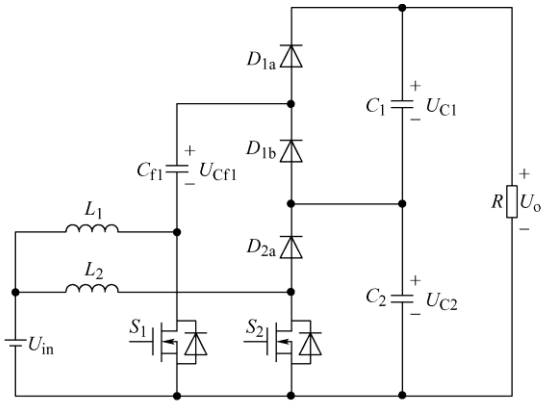
In general, placing several split capacitors connected in series is a good solution to reducing voltage stress across each capacitor. One solution is the application of a diode-capacitor voltage multiplier on the basic Boost converter and it can achieve a high voltage-gain and self-balanced capacitor voltages [6, 20-21]. However, large input current ripples and high current stresses across individual switches are inevitable as interleaved scheme cannot be used in this solution. A series of modular multilevel DC-DC converters were proposed in Refs. [22-27]. They are more suitable for high voltage applications, such as HVDC and high voltage drives as each converter module serves as an active switch in these converters. However, the voltage-gain is not enhanced. For example, a modular multilevel DC-DC converter was proposed in Ref. [27] based on Buck-Boost converter module. The lower-level module output voltage multiplied by $d/(1-d)$ serves as the input voltage of the upper-level module to achieve a high voltage-gain. Thus, it is a multi-stage DC-DC converter where the conversion efficiency can be an issue. Besides, the voltage gain is still limited in the three-level version and many components are required. An alternative three-level DC-DC converter was proposed in Ref. [28] to achieve a high voltage-gain at the expense of using more switches, diodes and a more complex modulation strategy. Two DC-DC converters were proposed in Refs. [29-30] using a coupling inductor technique to obtain high voltage-gain. However, they are two-stage converters resulting in low efficiency and the input current ripples are large. Ref. [31] proposed a quadratic Buck-Boost topology with a high voltage-gain at the expense of large input current ripples.

This paper proposes a new high voltage-gain boost converter with low voltage stress, small input current ripple and automatic current balancing function. The operating principle of the proposed topology and a comprehensive performance analysis are given. The rest of this paper is organized as follows: Sections 2 introduces the proposed topology and its operating principle. Performance analysis is presented in Section 3 and the experimental verifications are given in Section 4, followed by the conclusion drawn in Section 5.

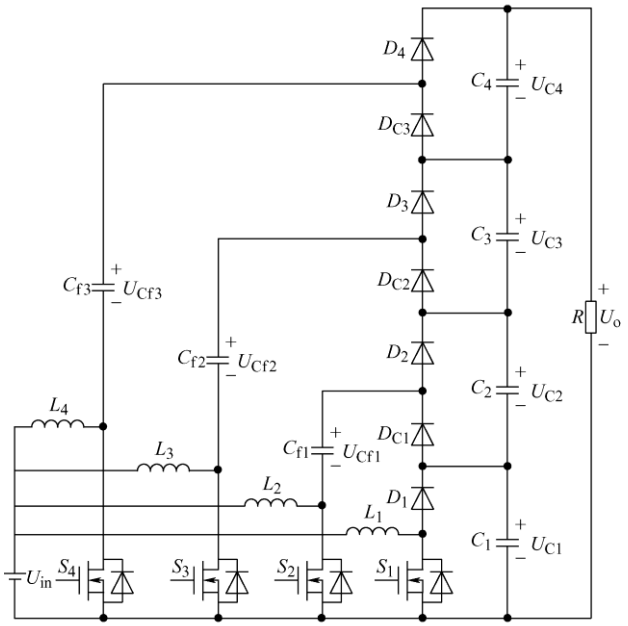
2 Proposed topology

The input-parallel-output-series hybrid switched-capacitor boost (IPOS-HSCB) converter shown in Fig. 1a is an integration of two interleaved boost converters and switched-capacitor technique [32]. L_1, S_1, D_{1a}, and C_1 form the first Boost converter, named as Boost I; L_2, S_2, D_{2a}, and C_2 form the second boost converter, named as Boost II. C_{f1}, D_{1b} and S_1, C_2 consist a switched-capacitor network, which makes the Boost I and Boost II an input-parallel-output-series circuit. With the input-parallel-output-series circuit, the IPOS-HSCB converter has a small input current ripple and a high voltage-gain. Another advantage of the IPOS-HSCB converter is the automatic current balancing function for the two inductor currents within the full duty cycle range. Based on the IPOS-HSCB converter, an extended multilevel Boost topology is proposed in Ref. [33]. Fig. 1b[33] shows that this kind of converter consisting of four Boost modules and three switched-capacitor networks (C_{f1}, D_{1b}, S_1, C_2; C_{f2}, D_{C2}, S_3, C_1, C_2; C_{f3}, D_{C3}, S_4, C_1, C_2, C_3). As two more Boost modules are added on the IPOS-HSCB converter with the help of three switched-capacitor networks, the converter in Fig. 1b has a much higher output voltage-gain and smaller input current ripple than the IPOS-HSCB converter in Fig. 1a. However, the number of flying capacitors is big and the voltage stresses across them are high in this converter.

To address the issue above, this paper proposes a double input-parallel-output-series hybrid switched-capacitor Boost (DIPOS-HSCB) converter, shown in Fig. 2. The new converter consists of two IPOS-HSCB converters (IPOS-HSCB I and IPOS-HSCB II) with their input terminals connected in parallel and output terminals in series. Therefore, one more input-parallel-output-series circuit is developed besides the input-parallel-output-series circuit in the IPOS-HSCB converter I or the IPOS-HSCB converter II. To distinguish the two IPOS circuits, the IPOS circuit in each IPOS-HSCB converter is called the inner IPOS circuit, while the IPOS circuit developed by the two IPOS-HSCB converters is named as the outer IPOS circuit.



(a) The IPOS-HSCB converter



(b) The extended IPOS-HSCB converter

Fig. 1 The IPOS-HSCB converters

The proposed double IPOS configuration enables the proposed DIPOS-HSCB converter to achieve a much higher voltage-gain and much smaller input current ripple than the IPOS-HSCB converter in Ref. [32]. Also, compared to the topology in Ref. [33], the number of flying-capacitors and the voltage stresses across them are reduced. Besides, one diode is reduced in the proposed converter. As shown in Ref. [32], the IPOS-HSCB converter has an automatic current balancing function due to the flying-capacitor C_{f1}. Also, in the extended topology in Ref. [33], the four inductor currents are automatically balanced due to the three flying-capacitors C_{f1}, C_{f2}, and C_{f3}. However, in the proposed DIPOS-HSCB converter, to guarantee the automatic balancing function for the four inductor currents, the gate signals of the four switches S_1, S_2, S_3 and S_4 must be phase shifted of 0° , 180° , 90° , 270° , respectively. As a result, the gate signals of the switches S_1, S_2 are phase shifted of 180° in IPOS-HSCB I and the same as for the gate signals of the switches S_3, S_4 in IPOS-HSCB II. According to Ref. [32], the two inductor currents in each converter module (IPOS-HSCB I or IPOS-HSCB II) can be automatically balanced.

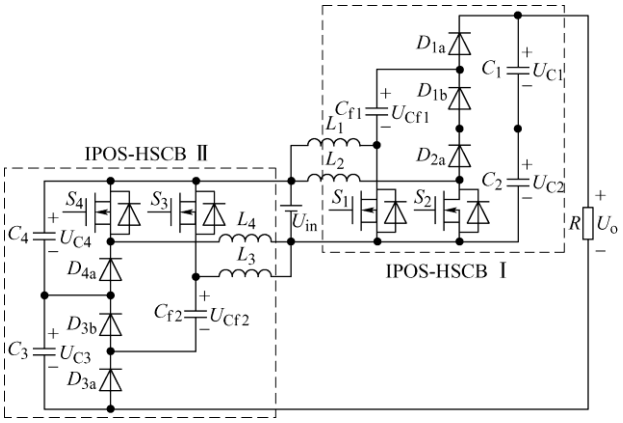


Fig. 2 The proposed DIPOS-HSCB converter

To simplify the steady-state analysis of the proposed DIPOS-HSCB converter, the operating conditions are assumed to be as follows.

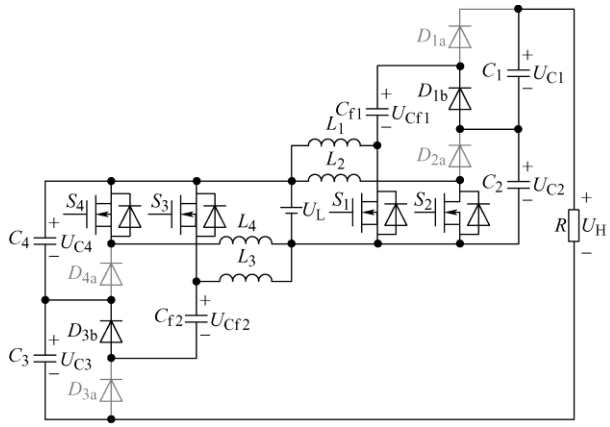
(a) All components in Fig. 2 are assumed to be ideal and the converter operates in continuous conduction mode (CCM).

(b) All the capacitances are large enough that each capacitor voltage is considered constant over each switching period.

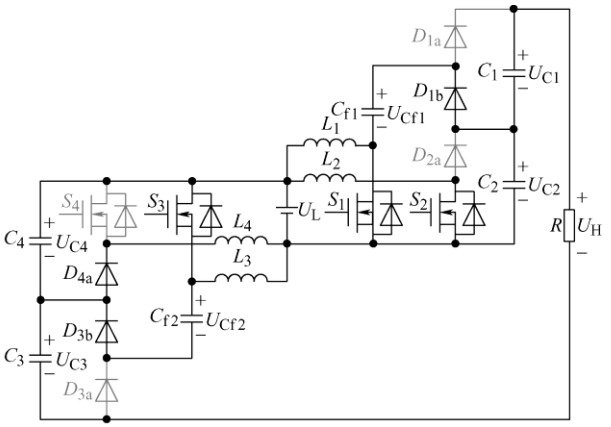
To enable self-balancing of the four inductor currents of the DIPOS-HSCB converter, the gate signals of the four switches S_1, S_2, S_3 and S_4 are driven by a same duty cycle d with phase shifted of 0° , 180° , 90° , 270° . The switching states of the proposed DIPOS-HSCB converter are given in Tab. 1 with the corresponding equivalent circuits presented in Fig. 3, where there are 16 switching states.

Tab. 1 Switching states of the proposed DIPOS-HSCB converter

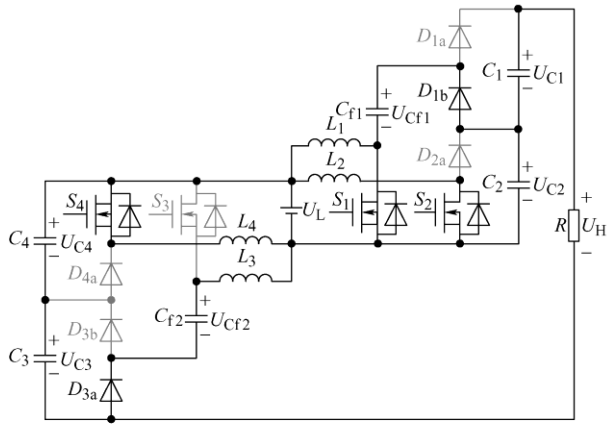
Power switches	Equivalent circuits in Fig. 1															
	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)	(i)	(j)	(k)	(l)	(m)	(n)	(o)	(p)
S_1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
S_2	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
S_3	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
S_4	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0



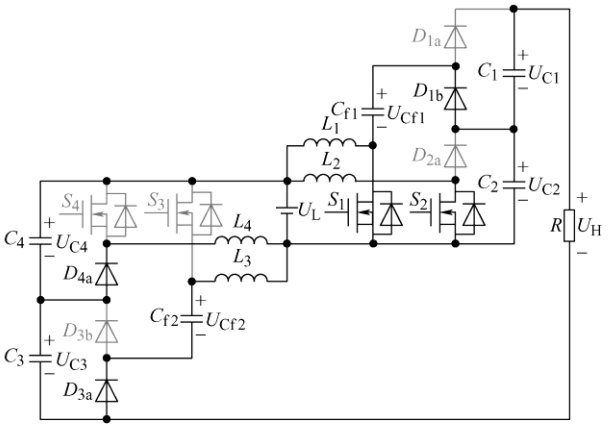
(a) State 1



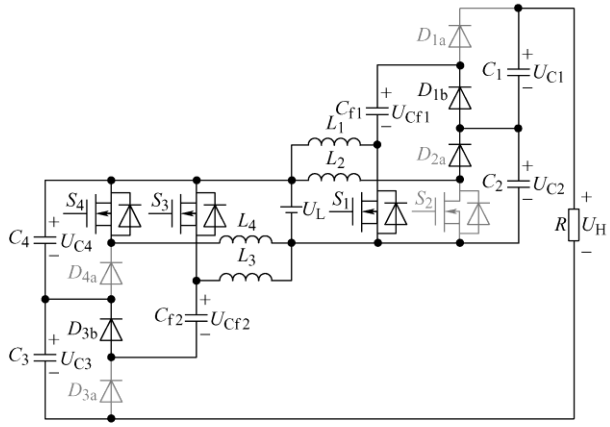
(b) State 2



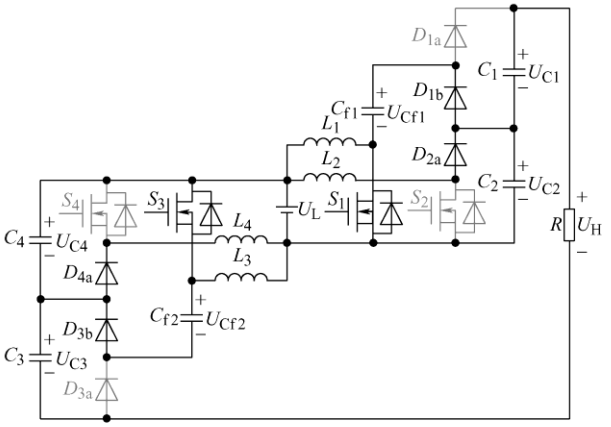
(c) State 3



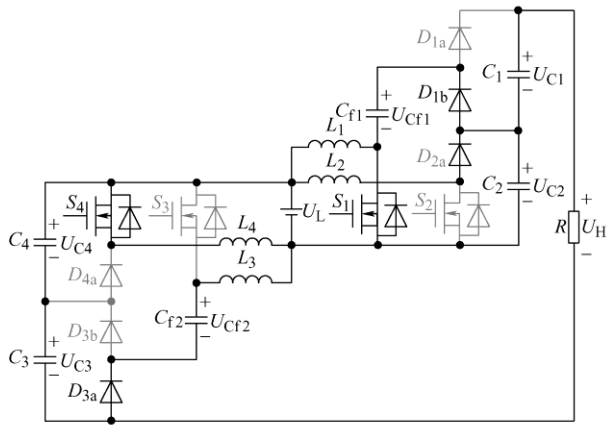
(d) State 4



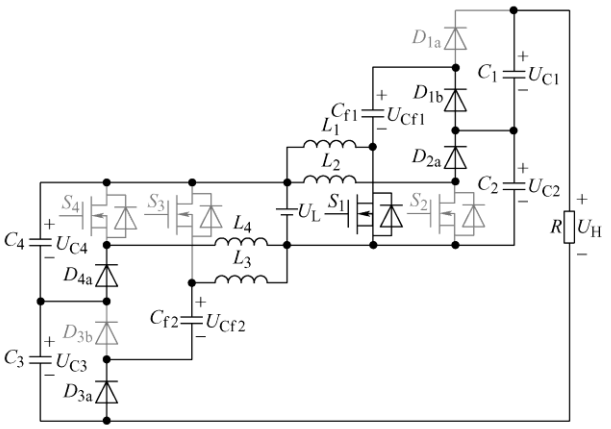
(e) State 5



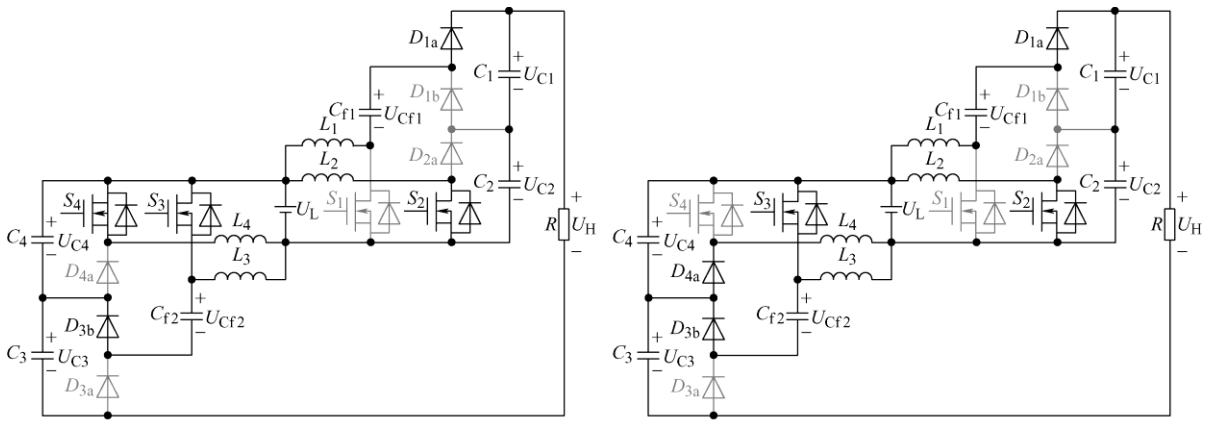
(f) State 6



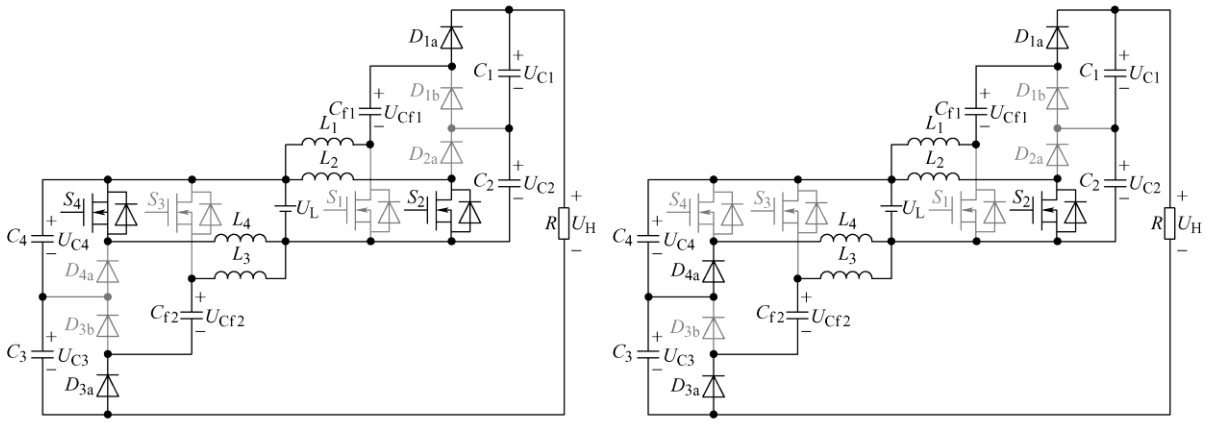
(g) State 7



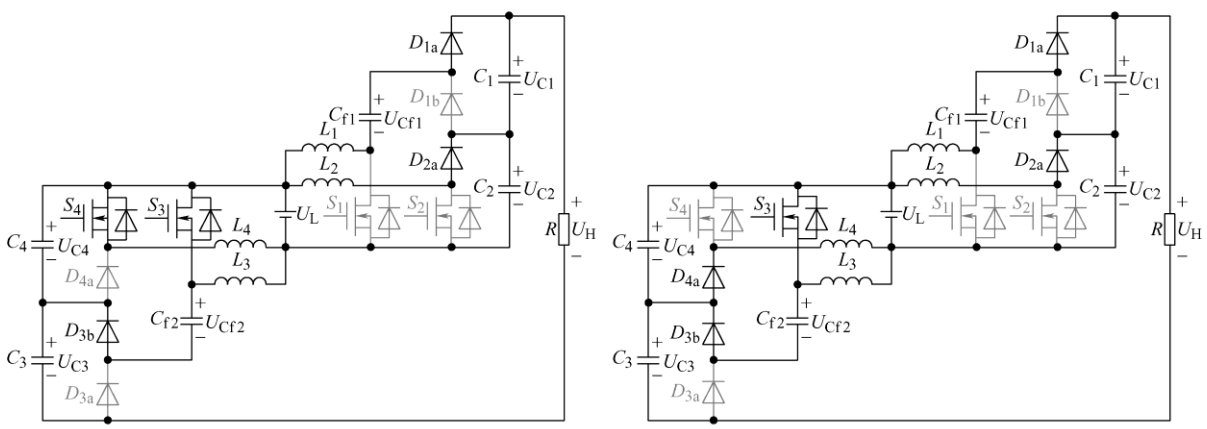
(h) State 8



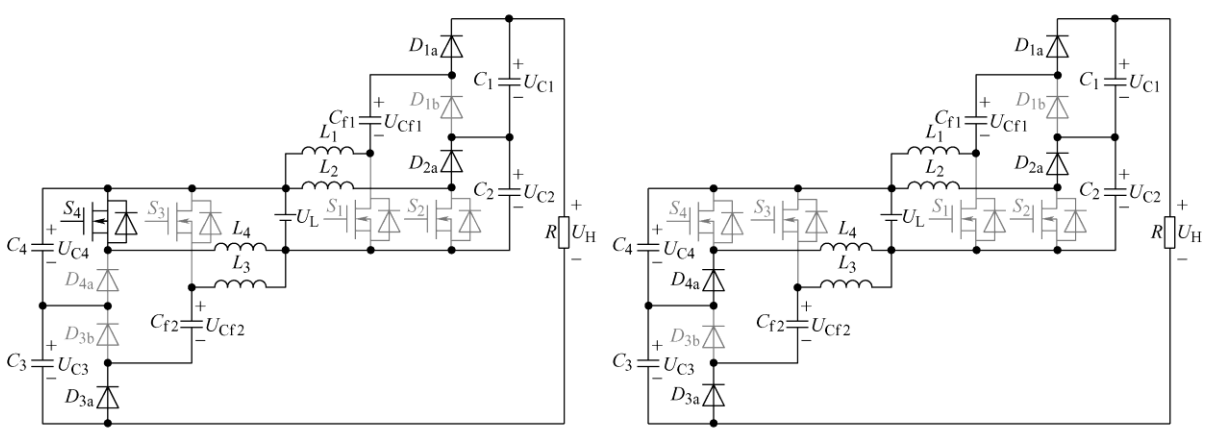
(i) State 9 (j) State 10



(k) State 11 (l) State 12



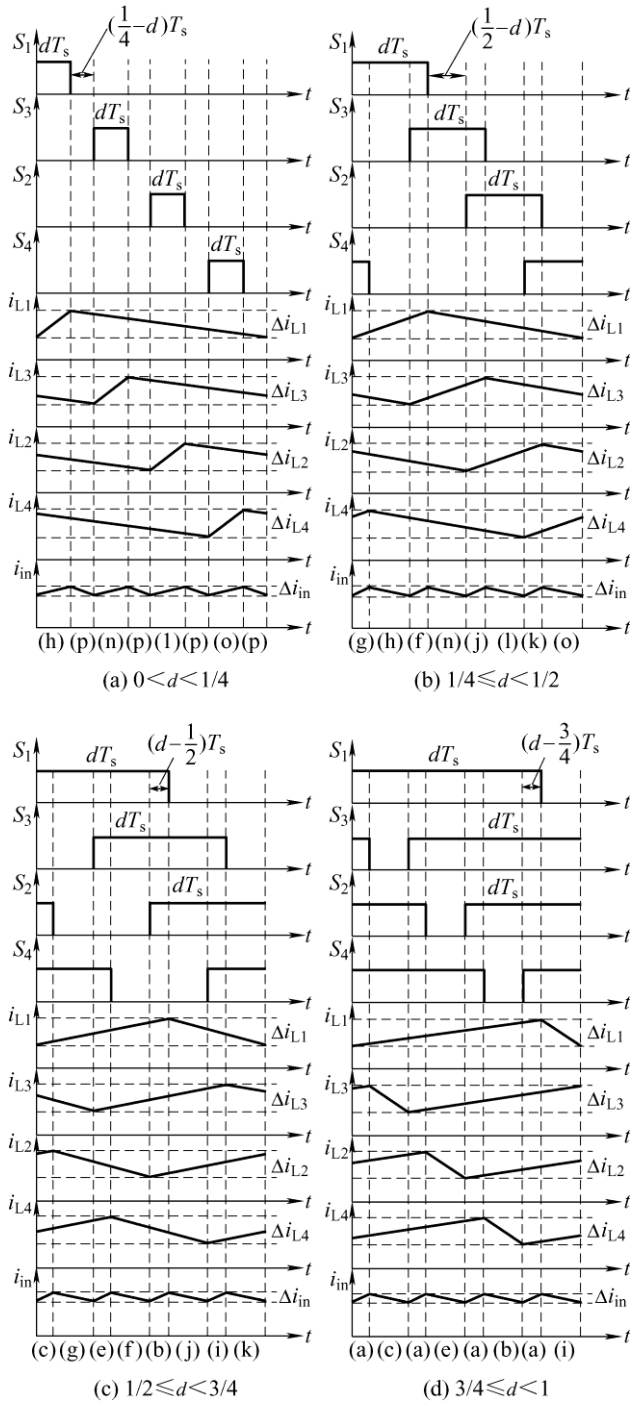
(m) State 13 (n) State 14



(o) State 15 (p) State 16

Fig. 3 Operating states of the proposed DIPOS-HSCB converter

As shown in Fig. 4, there are four different operating modes according to the duty cycle d.



(a) $0<d<1/4$ (b) $1/4\leqslant d<1/2$

(c) $1/2\leqslant d<3/4$ (d) $3/4\leqslant d<1$

Fig. 4 The inductor current ripples of the proposed DIPOS-HSCB converter under different operating modes

(a) As shown in Fig. 4a, when d is smaller than 1/4, the switching states are shown in Fig. 3h, 3p, 3n, 3p, 3l, 3p, 3o and 3p. The switching state in Fig. 3p is repeated.

(b) As shown in Fig. 4b, when d is between 1/4 and 1/2, the switching states are shown in Fig. 3g, 3h, 3f, 3n, 3j, 3l, 3k and 3o.

(c) As shown in Fig. 4c, when d is between 1/2 and 3/4, the switching states are shown in Fig. 3c, 3g, 3e, 3f, 3b, 3j, 3i and 3k.

(d) As shown in Fig. 4d, when d is over 3/4, the switching states are shown in Fig. 3a, 3c, 3a, 3e, 3a, 3b, 3a and 3i. The switching state in Fig. 3a is repeated.

At any switching state, the output voltage of the proposed converter is always expressed by

$$U_{\mathrm{o}}=U_{\mathrm{Cl}}+U_{\mathrm{C2}}+U_{\mathrm{C3}}+U_{\mathrm{C4}}-U_{\mathrm{in}} \tag{1}$$

Four voltage-second balance equations applied on the inductors L_1, L_2, L_3 and L_4 can be expressed by

$$dT_{\mathrm{s}}U_{\mathrm{in}}+(1-d)T_{\mathrm{s}}(U_{\mathrm{in}}+U_{\mathrm{Cf1}}-U_{\mathrm{Cl}}-U_{\mathrm{C2}})=0 \tag{2}$$

$$dT_{\mathrm{s}}U_{\mathrm{in}}+(1-d)T_{\mathrm{s}}(U_{\mathrm{in}}-U_{\mathrm{Cl}})=0 \tag{3}$$

$$dT_{\mathrm{s}}U_{\mathrm{in}}+(1-d)T_{\mathrm{s}}(U_{\mathrm{in}}+U_{\mathrm{Cf2}}-U_{\mathrm{C3}}-U_{\mathrm{C4}})=0 \tag{4}$$

$$dT_{\mathrm{s}}U_{\mathrm{in}}+(1-d)T_{\mathrm{s}}(U_{\mathrm{in}}-U_{\mathrm{C3}})=0 \tag{5}$$

Besides, during the switching states 1-8, the flying capacitor C_{fl} is clamped by the capacitor C_2. Therefore, there is

$$U_{\mathrm{Cf1}}=U_{\mathrm{C2}} \tag{6}$$

During the switching states in Fig. 3a, 3b, 3e, 3f, 3i, 3j, 3m, 3n, the flying capacitor C_{f2} is clamped by the capacitor C_4. Therefore, there is

$$U_{\mathrm{Cf2}}=U_{\mathrm{C4}} \tag{7}$$

According to Eqs. (1)-(7), the output voltage and all the capacitor voltages of proposed converter are

$$U_{\mathrm{o}}=\frac{3+d}{1-d}U_{\mathrm{in}} \tag{8}$$

$$U_{\mathrm{Cl}}=U_{\mathrm{C2}}=U_{\mathrm{C3}}=U_{\mathrm{C4}}=U_{\mathrm{Cf1}}=U_{\mathrm{Cf2}}=\frac{1}{1-d}U_{\mathrm{in}}=\frac{1}{3+d}U_{\mathrm{o}} \tag{9}$$

3 Performance analysis

3.1 Voltage stress

In the proposed converter, the voltage stresses across all switches, diodes, and capacitors are small, which are

$$u_{\mathrm{S}}=u_{\mathrm{D}}=u_{\mathrm{Cf}}=u_{\mathrm{C}}=\frac{1}{1-d}U_{\mathrm{in}}=\frac{1}{3+d}U_{\mathrm{o}} \tag{10}$$

where u_{S}, u_{D}, u_{C}, and u_{Cf} represent the voltage stresses across all the switches, diodes, flying capacitors, and output capacitors. It can be found that the voltage stresses across all these components are $1/(3+d)$ time of the output voltage.

3.2 Automatic current balancing

As described in Section 2, the proposed converter consists of two IPOS-HSCB converters (IPOS-HSCB I and IPOS-HSCB II). The gate signals of the four switches S_1, S_2, S_3 and S_4 have a same duty cycle d with phase shifted of 0°, 180°, 90°, 270°, respectively. It can be found that the two switches S_1 and S_2 in IPOS-HSCB I are phase shifted of 180° and the two switches S_3 and S_4 in IPOS-HSCB II are also phase shifted of 180°.

Taking the IPOS-HSCB I as an example, the equivalent circuits of it are presented in Fig. 5. The average charging current flowing through C_{f1} is the same as the average current flowing through D_{1b} during one switching period T_s. Thus, the increased charges of C_{f1} during one switching period is $I_{D1b}\times T_s$. In addition, when the duty cycle d is over 0.5, the flying-capacitor C_{f1} is only discharged during the switching state II and the average discharging current flowing through C_{f1} is I_{L1} with the discharging time $(1–d)T_s$. When d is smaller than 0.5, the flying-capacitor C_{f1} is discharged during the switching state II and the switching state IV with the average discharging current I_{L1} and the total discharged time $(1–d)T_s$. It can be seen that the decreased charges of C_{f1} during one switching period is $I_{L1}\times(1–d)T_s$ no matter what the duty cycle d is. Therefore, by applying the Ampere-Second Balance Principle on C_{f1} in IPOS-HSCB I, there is

$$I_{D1b}\times T_s = I_{L1}\times(1-d)T_s \tag{11}$$

Similarly, applying the Ampere-Second Balance Principle on the flying capacitor C_{f2} in IPOS-HSCB II, there is

$$I_{D3b}\times T_s = I_{L3}\times(1-d)T_s \tag{12}$$

According to Eqs. (11)-(12), the average currents of inductors L_1 and L_3 are

$$I_{L1} = \frac{1}{1-d} I_{D1b} \tag{13}$$

$$I_{L3} = \frac{1}{1-d} I_{D3b} \tag{14}$$

Additionally, it is easy to obtain the average currents of L_2 and L_4 as below

$$I_{L2} = \frac{1}{1-d} I_{D2a} \tag{15}$$

$$I_{L4} = \frac{1}{1-d} I_{D4a} \tag{16}$$

In the proposed DIPOS-HSCB converter, the average output currents of all diodes are equal as they are connected in series at the output terminal.

$$I_{D1a} = I_{D1b} = I_{D2a} = I_{D3a} = I_{D3b} = I_{D4a} = I_o \tag{17}$$

It can be concluded from Eqs. (11)-(17) that the four inductor currents are automatically balanced.

$$I_{L1} = I_{L2} = I_{L3} = I_{L4} = \frac{1}{1-d} I_o \tag{18}$$

Hence, additional current-sharing control strategies as well as current sensors required for multiple DC-DC converters-based conversion system, are not necessary for the proposed DIPOS-HSCB converter.

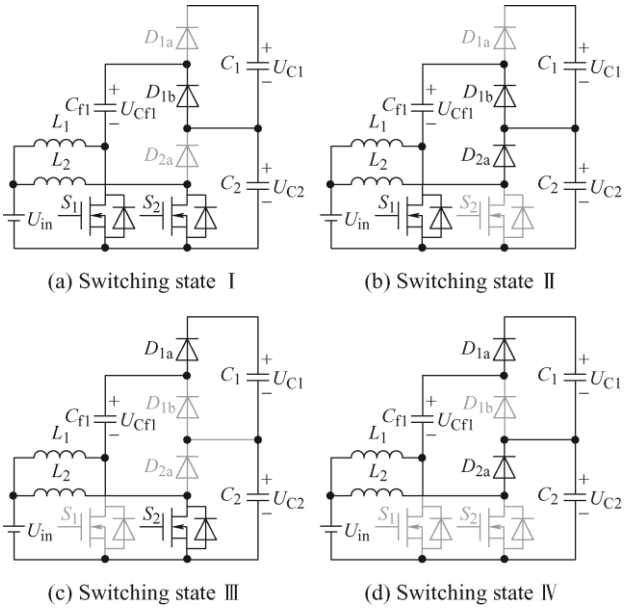


Fig. 5 Equivalent circuits of the IPOS-HSCB I

3.3 Current ripple

In the proposed DIPOS-HSCB converter, the current ripples of all inductors can be obtained by

$$\Delta i_{Lk} = \frac{U_{in}}{L}\frac{d}{f_s} \quad k = 1, 2, 3, 4 \tag{19}$$

At the same time, all the inductor current waveforms under different operating modes are presented in Fig. 4. As for each Boost module, the increasing slope of the inductor current is expressed by

$$k_{in} = \frac{U_{in}}{L} \tag{20}$$

Meanwhile, the decreasing slope of the inductor

current is expressed by

$$k_{de}=\frac{\frac{1}{1-d}U_{in}-U_{in}}{L}=\frac{d}{1-d}\frac{U_{in}}{L} \tag{21}$$

In the operating mode ($0<d\leqslant 1/4$) of Fig. 4a, the operating time for the switching state 16 in Fig. 3p is $(1/4-d)T_s$. During this switching state, all the four inductor currents decrease with the slope of k_{de} and thus the input current ripple is

$$\Delta i_{in}=k_{de}\times(\frac{1}{4}-d)T_s\times 4=\frac{U_{in}}{L}\frac{d(1-4d)}{(1-d)f_s} \qquad 0<d<\frac{1}{4} \tag{22}$$

In the operating mode ($1/4\leqslant d<1/2$) of Fig. 4b, the operating time for the switching states 8, 12, 14 and 15 in Fig. 3 is $(1/2-d)T_s$. During these switching states, three inductor currents decrease with the slope of k_{de} and one inductor current increases with the slope of k_{in}. Thus, the input current ripple is calculated by

$$\Delta i_{in}=(k_{de}\times 3-k_{in})\times(\frac{1}{2}-d)T_s=\frac{U_{in}}{L}\frac{(4d-1)(1-2d)}{2(1-d)f_s} \quad \frac{1}{4}\leqslant d<\frac{1}{2} \tag{23}$$

In the operating mode of Fig. 4c, the operating time for the switching states 2, 3, 5 and 9 in Fig. 3 is achieved by $(d-1/2)T_s$. During these switching states, three inductor currents increase with the slope of k_{in} and one inductor current decreases with the slope of k_{de}. Thus, the input current ripple is calculated by

$$\Delta i_{in}=(k_{in}\times 3-k_{de})\times(d-\frac{1}{2})T_s=\frac{U_{in}}{L}\frac{(3-4d)(2d-1)}{2(1-d)f_s} \quad \frac{1}{2}\leqslant d<\frac{3}{4} \tag{24}$$

In the operating mode of Fig. 4d, the operating time for the switching state (1) in Fig. 3a is $(d-3/4)T_s$. All the four inductor currents increase with the slope of k_{in} and thus the input current ripple is

$$\Delta i_{in}=k_{in}\times(d-\frac{3}{4})T_s\times 4=\frac{U_{in}}{L}\frac{4d-3}{f_s} \qquad \frac{3}{4}\leqslant d<1 \tag{25}$$

Overall, the input current ripple of the proposed DIPOS-HSCB converter can be concluded as follows

$$\Delta i_{in}=\begin{cases}\dfrac{U_{in}}{L}\dfrac{d(1-4d)}{(1-d)f_s} & 0\leqslant d<\dfrac{1}{4}\\ \dfrac{U_{in}}{L}\dfrac{(4d-1)(1-2d)}{2(1-d)f_s} & \dfrac{1}{4}\leqslant d<\dfrac{1}{2}\\ \dfrac{U_{in}}{L}\dfrac{(3-4d)(2d-1)}{2(1-d)f_s} & \dfrac{1}{2}\leqslant d<\dfrac{3}{4}\\ \dfrac{U_{in}}{L}\dfrac{4d-3}{f_s} & \dfrac{3}{4}\leqslant d<1\end{cases} \tag{26}$$

It can be seen from Eq. (26) that when the duty cycle d is 1/4, 1/2 or 3/4, the input current ripple of the proposed DIPOS-HSCB converter should be zero theoretically.

3.4 Comparative analysis

Tab. 2 presents the comparison between the converter in Fig. 1b and the proposed DIPOS-HSCB converter. S, C, and D represent the number of switches, capacitors and diodes, respectively, and G represents the voltage gain. It can be found that the voltage gain of the proposed converter is smaller than the voltage gain of the converter in Fig. 1b only by 1. The proposed converter needs two switched-capacitor networks to realize automatic current balancing function while the converter in Fig. 1b needs three switched-capacitor networks. As a result, the proposed converter saves one flying-capacitor and one diode, and both the flying-capacitors C_{f1} and C_{f2} have the same voltage stress, which is smaller than that of the converter in Fig. 1b. Furthermore, the flying-capacitor C_{f3} with large voltage stress does not exist in the proposed converter. Besides, all the output capacitors (C_1, C_2, C_3, C_4) in the two converters have the same voltage stress.

Tab. 2 Comparison of the IPOS-HSCB converter in Fig. 1b and the proposed DIPOS-HSCB converter

	S	C	D	G	U_{Ck} (k=1, 2, 3, 4)	U_{Cf1}	U_{Cf2}	U_{Cf3}	Switched-capacitor networks	Automatic current balancing
Fig. 1b	4	7	7	$4/(1-d)$	$1/(1-d)U_{in}$	$1/(1-d)U_{in}$	$2/(1-d)U_{in}$	$3/(1-d)U_{in}$	3	Yes
DIPOS-HSCB	4	6	6	$(3+d)/(1-d)$	$1/(1-d)U_{in}$	$1/(1-d)U_{in}$	$1/(1-d)U_{in}$	—	2	Yes

4 Experimental verification

As shown in Fig. 6, a prototype of the proposed DIPOS-HSCB converter at a power rating of 120 W is implemented according to the detailed specifications in Tab. 3. It should be noted that u_{S1}, u_{S2}, u_{S3}, and u_{S4} are defined to describe the voltage difference between the drain terminal and the source terminal of the

switches S_1, S_2, S_3, and S_4, respectively. U_1 means the sum of the average capacitor voltages U_{C1} and U_{C2}. U_2 means the sum of the average capacitor voltages U_{C3} and U_{C4}. u_{D1a}, u_{D1b}, u_{D2a}, u_{D3a}, u_{D3b}, u_{D4a} are defined as the voltage difference between the cathode and the anode of the power diodes D_{1a}, D_{1b}, D_{2a}, D_{3a}, D_{3b}, and D_{4a}, respectively.

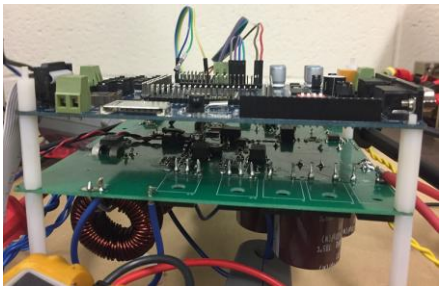


Fig. 6 The experimental prototype

Tab. 3 Specifications of the proposed DIPOS-HSCB converter prototype

Parameter	Value
Input voltage U_{in}/V	12-18
Output voltage U_o/V	200
Output power P/W	120
Switching frequency f_s/kHz	25
Inductors L_1, L_2, L_3, L_4/mH	1
Capacitors C_1, C_2, C_3, C_4, C_{f1}, C_{f2}	470 μF/200 V
Switches S_1, S_2, S_3, S_4	IRFP260NPBF
Optocoupler	SI8711CC-B-IS
Gate driver	IXDI609SI
Diodes D_{1a}, D_{1b}, D_{2a}, D_{3a}, D_{3b}, D_{4a}	APT30S20BG

A voltage loop control strategy shown in Fig. 7 is used to realize the output voltage stabilization and it is implemented based on the digital chip TMS320F28335. A voltage error signal is obtained by taking the referring voltage 200 V to subtract the sampling output voltage U_o, and then passes through a proportional-integral regulator to compare with the four carrier signals V_{carr1}, V_{carr2}, V_{carr3} and V_{carr4} to achieve the driving signals for the four switches S_1, S_2, S_3, and S_4. With the voltage loop control, the steady experimental results of the proposed converter are given in Figs. 8-11.

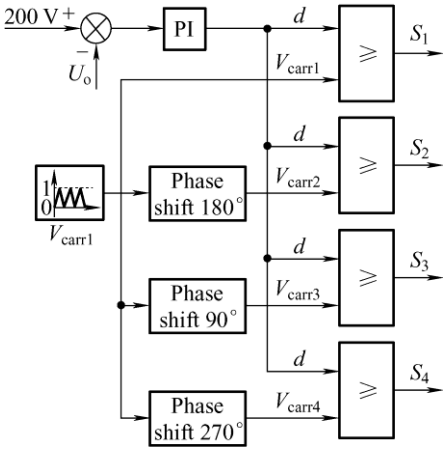
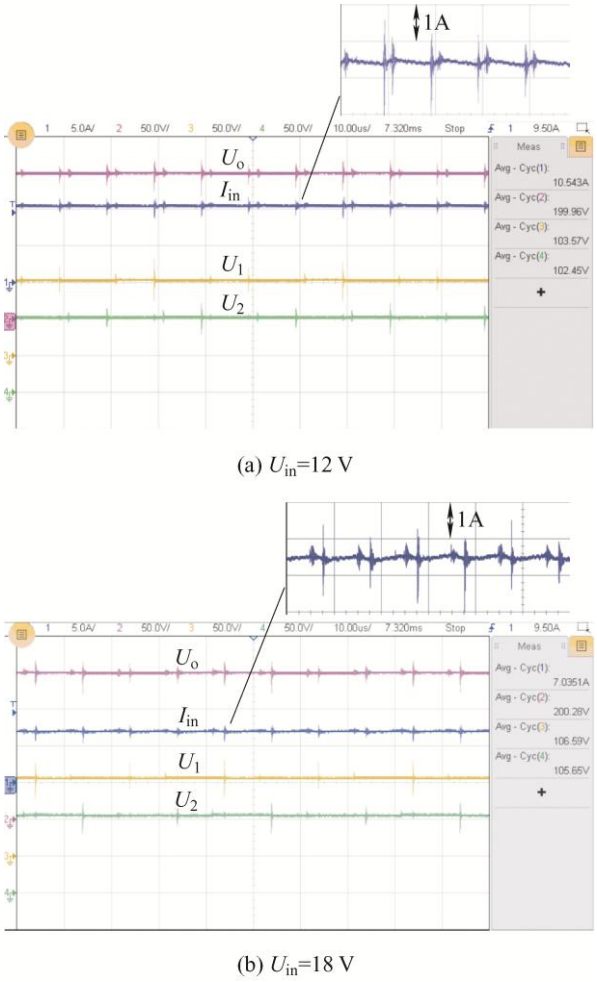


Fig. 7 Closed loop control of the proposed converter



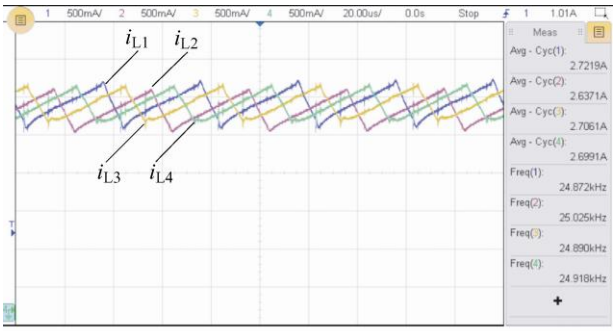
(a) U_{in}=12 V

(b) U_{in}=18 V

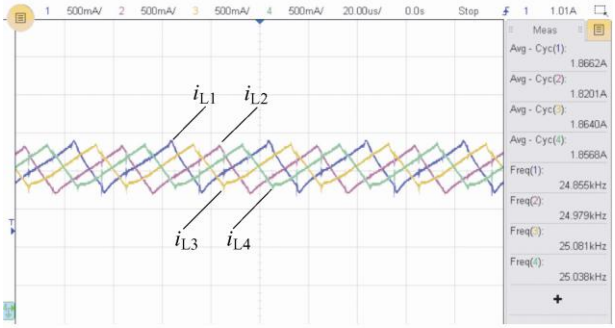
Fig. 8 Voltage waveforms under different input voltages

As shown in Fig. 8, the output voltage of the proposed converter is stable at 200 V at different input voltages of 12 V and 18 V. The input current ripple of the proposed converter is small and its ripple frequency is 100 kHz, which is four times the switching frequency of 25 kHz. Besides, the four inductor currents i_{L1}, i_{L2}, i_{L3}, and i_{L4} are phase shifted by 0° , 180° , 90° , 270° , respectively. This verifies the correctness of the interleaved modulation scheme used for the proposed converter. In addition, it can be seen from Fig. 9 that all the four inductor currents nearly have the same average

value. For example, I_{L1}, I_{L2}, I_{L3}, and I_{L4} have the same average value of 1.8 A when the input voltage is 18 V. This indicates that automatic the same average value. For example, I_{L1}, I_{L2}, I_{L3}, and I_{L4} have the same average value of 1.8 A when the input voltage is 18 V. This indicates that automatic current balancing funciton is achieved. Besides, when the input voltage is 12 V, all the six capacitor voltages shown in Fig. 10 are nearly the same at a value of 52 V. The voltage stresses across all the switches and diodes shown in Fig. 11 are also nearly the same with the value of 54 V or 56 V. These results indicate that the voltage stresses acorss all components are small. Overall, these results verify the effectiveness of the proposed DIPOS-HSCB converter.



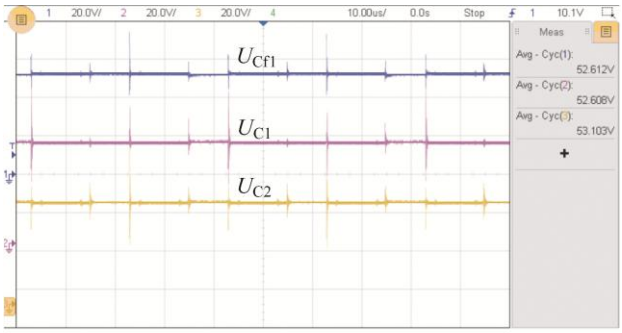
(a) U_{in}=12 V



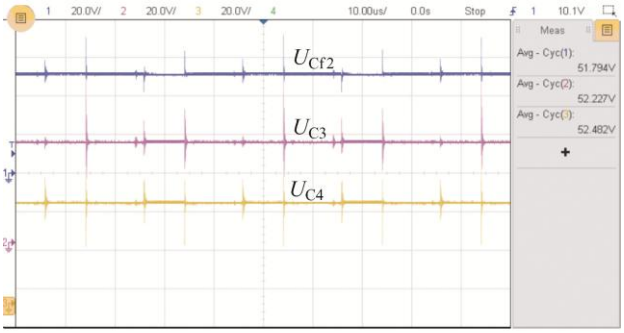
(b) U_{in}=18 V

Fig. 9 Inductor current waveforms under different input voltages

The dynamic results of the proposed converter when the input voltage jumps up from 12 V to 18 V and down from 18 V to 12 V are presented in Fig. 12a and Fig. 12b, respectively. The output voltage and each IPOS-HSCB converter's output voltage stay stable with a short dynamic response time, which is around 150 ms. When the input voltage jumps up from 12 V to 18 V, the input current reduces from 10.5 A to 7.0 A with a smooth transition process. When the input voltage jumps down from 18 V to 12 V, the input current increases from 7.0 A to 10.5 A.

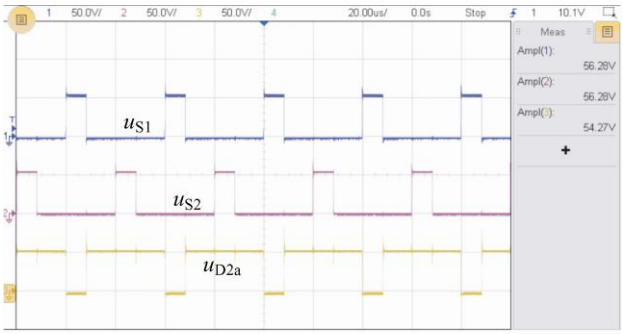


(a) Capacitor voltage waveforms of C_{f1},C_1 and C_2

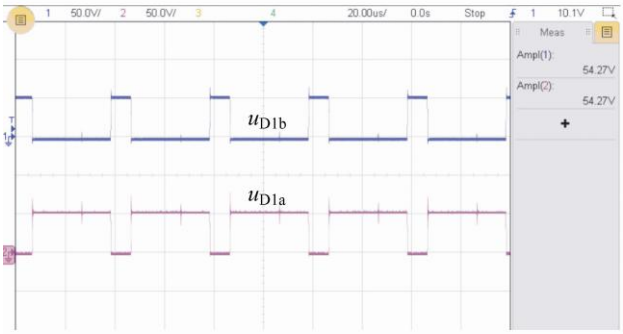


(b) Capacitor voltage waveforms of C_{f2},C_3 and C_4

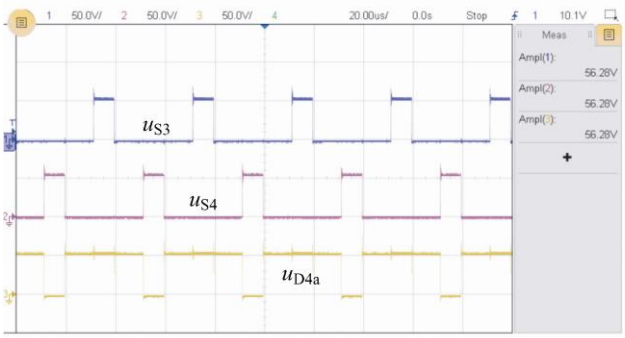
Fig. 10 Capacitor voltage waveforms under an input voltage of 12 V



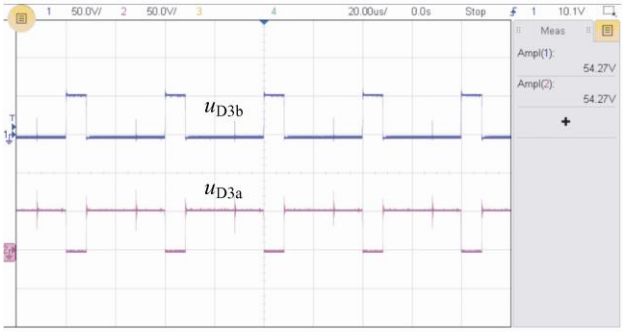
(a) Voltage waveforms of S_1, S_2 and D_{2a}



(b) Voltage waveforms of D_{1b} and D_{1a}

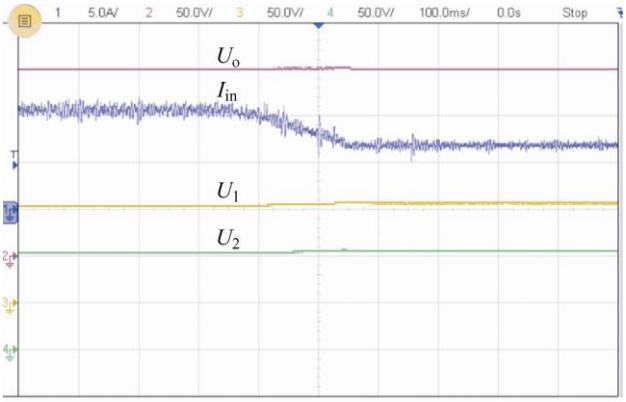


(c) Voltage waveforms of S_3, S_4 and D_{4a}

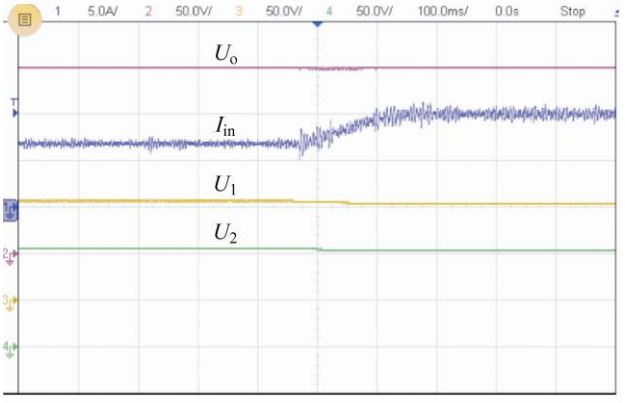


(d) Voltage waveforms of D_{3b} and D_{3a}

Fig. 11 Voltage waveforms of all the switches and diodes under an input voltage of 12 V



(a) Input voltage jumps up from 12 V to 18 V



(b) Input voltage steps down from 18 V to 12 V

Fig. 12 Dynamic results

Also, the conversion efficiency curves versus different output power levels when the DIPOS-HSCB converter operates under the input voltages of 12 V and 18 V are presented in Fig. 13. The conversion efficiency of the DIPOS-HSCB converter at the rated power point 120 W is 94.0% when the input voltage is 12 V and 95.2% when the input voltage is 18 V. The maximum efficiency of the proposed converter is 96.0% when the input voltage is 12 V and 97.2% when the input voltage is 18 V, shown in Fig. 13. It can be observed that as the input voltage decreases, the conversion efficiency of the DIPOS-HSCB converter decreases. Because for the same output power, the input current increases as the input voltage decreases. As a result, the switching losses and the conduction losses of the power semiconductors will rise as well as the conduction losses of the equivalent series resistors in the proposed converter.

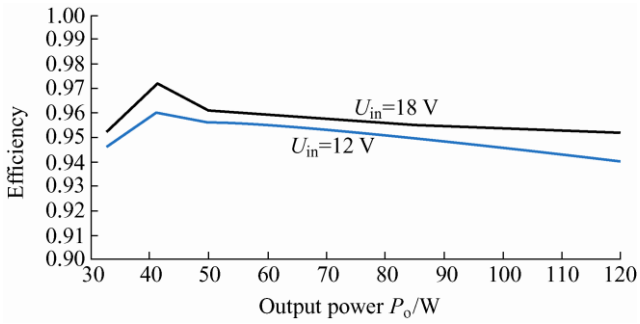


Fig. 13 Efficiency curve of the proposed DIPOS-HSCB converter under different input voltages

5 Conclusion

This paper introduces a double input-parallel-output-series hybrid switched-capacitor boost converter which consists of an inner input-parallel-output-series circuit and an outer input-parallel-output-series circuit. Owing to the double input-parallel-output-series configuration, a high voltage-gain, low component stress, and small input current ripple are achieved. Compared to the existing converters, the number of components and the voltage stresses across them are both reduced. Furthermore, with a special carrier phase-shifted modulation scheme, i.e., the gate signals of switches S_1, S_2, S_3, and S_4 are phase shifted by 0°, 180°, 90°, 270°, the four inductor currents of the proposed converter can be automatically balanced. All of these merits enable it a good alternative for applications where DC/DC

converters with high voltage-gain, small input current ripple and simple configuration are required.

References

[1] V Yaramasu, B Wu, P C Sen, et al. High-power wind energy conversion systems: State-of-the-art and emerging technologies. *Proc. IEEE*, 2015, 103(5): 740-788.

[2] C Xia, X Gu, T Shi, et al. Neutral-point potential balancing of three-level inverters in direct-driven wind energy conversion system. *IEEE Trans. Energy Convers.*, 2011, 26(1): 18-29.

[3] G Estay, L Vattuone, S Kouro, et al. Dual-boost-NPC converter for a dual three-phase PMSG wind energy conversion system. *2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Bangaluru, India, 2012: 1-6.

[4] J Kim, O Yang. Design of a high-efficient grid-connected three-phase three-level T-type PV power system. *Int. J. Control Autom.*, 2014, 7(10): 65-78.

[5] Z Hao, Z Jinghua, H Bing, et al. A new interleaved three-level boost converter and neutral-point potential balancing. *2013 2nd International Symposium on Instrumentation and Measurement, Sensor Network and Automation (IMSNA)*, United States, 2013: 1093-1096.

[6] J C Rosas-Caro, J M Ramirez, F Z Peng, et al. A DC-DC multilevel boost converter. *IET Power Electron.*, 2010, 3(1): 129-137.

[7] K Jin, X Ruan, M Yang, et al. A hybrid fuel cell power system. *IEEE Trans. Ind. Electron.*, 2009, 56(4): 1212-1222.

[8] K A Corzine, S K Majeetha. Analysis of a novel four-level DC-DC boost converter. *Thirty-Fourth IAS Annual Meeting Conference Record of the 1999 IEEE Industry Applications Conference,* Phoenix, AZ, USA, 1999: 1964-1971.

[9] J R Rahul, A Kirubakaran, D Vijayakumar. A new multilevel DC-DC boost converter for fuel cell based power system. *2012 IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS)*, Bhopal, India, 2012: 1-5.

[10] Y R De Novaes, A Rufer, I Barbi. A new quadratic three-level DC-DC converter suitable for fuel cell applications. *2007 Power Conversion Conference, Nagoya*, 2007: 601-607.

[11] K Jin, M Yang, X Ruan, et al. Three-level bidirectional converter for fuel-cell/battery hybrid power system. *IEEE Trans. Ind. Electron.*, 2010, 57(6): 1976-1986.

[12] S Rivera, B Wu, S Kouro, et al. Electric vehicle charging station using a neutral-point clamped converter with bipolar DC bus. *IEEE Trans. Ind. Electron.*, 2015, 62(4): 1999-2009.

[13] L Tan, B Wu, V Yaramasu, et al. Effective voltage balance control for bipolar-DC-bus fed EV charging station with three-level DC-DC fast charger. *IEEE Trans. Ind. Electron.*, 2016, 63(7): 4031-4041.

[14] H Kakigano, Y Miura, T Ise. Low-voltage bipolar-type DC microgrid for super high quality distribution. *IEEE Trans. Power Electron.*, 2010, 25(12): 3066-3075.

[15] H Kakigano, Y Miura, T Ise, et al. DC voltage control of the DC micro-grid for super high quality distribution. 2007 *Power Conversion Conference, Nagoya*, 2007: 518-525.

[16] H Kakigano, Y Miura, T Ise. Distribution voltage control for DC microgrids using fuzzy control and gain-scheduling technique. *IEEE Trans. Power Electron.*, 2013, 28(5): 2246-2258.

[17] Y Jang, M M Jovanovic. Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end. *IEEE Trans. Power Electron.*, 2007, 22(4): 1394-1401.

[18] L W Zhou, B X Zhu, Q M Luo, et al. Interleaved non-isolated high step-up DC-DC converter based on the diode-capacitor multiplier. *IET Power Electron.*, 2014, 7(2): 390-397.

[19] L C Franco, L L Pfitscher, R Gules. A new high static gain nonisolated DC-DC converter. *IEEE 34th Annual Power Electronics Specialist Conference*, Acapulco, Mexico, Mexico, 2003: 1367-1372.

[20] J C Rosas-Caro, J C Mayo-Maldonado, R Salas-Cabrera, et al. A family of DC-DC multiplier converters. *Eng. Lett.*, 2011, 19(1): 57-67.

[21] J C Mayo-Maldonado, R Salas-Cabrera, J C Rosas-Caro, et al. Modelling and control of a DC-DC multilevel boost converter. *IET Power Electron.*, 2011, 4(6): 693-700.

[22] A Parastar, Y C Kang, J K Seok. Multilevel modular DC-DC power converter for high-voltage DC-connected offshore wind energy applications. *IEEE Trans. Ind. Electron.*, 2015, 62(5): 2879-2890.

[23] X Zhang, T C Green. The modular multilevel converter for high step-up ratio DC-DC conversion. *IEEE Trans. Ind. Electron.*, 2015, 62(8): 4925-4936.

[24] J A Ferreira. The multilevel modular DC converter. *IEEE Trans. Power Electron.*, 2013, 28(10): 4460-4465.

[25] X Zhang, T C Green. The new family of high step ratio modular multilevel DC-DC converters. *IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 15-19, 2015, Charlotte, NC, USA, 2015: 1743-1750.

[26] A A Hagar, P W Lehn. Comparative evaluation of a new family of transformerless modular DC-DC converters for high-power applications. *IEEE Trans. Power Deliv.*, 2014, 29(1): 444-452.

[27] K Filsoof, P W Lehn. A bidirectional modular multilevel DC-DC converter of triangular topology. *IEEE Trans. Power Electron.*, 2015, 30(1): 54-64.

[28] Y Zhang, J T Sun, Y F Wang. Hybrid boost three-level DC-DC converter with high voltage gain for photovoltaic generation systems. *IEEE Trans. Power Electron.*, 2013, 28(8): 3659-3664.

[29] N Zhang, D Sutanto, K M Muttaqi, et al. High-voltage-gain quadratic boost converter with voltage multiplier. *IET Power Electron.*, 2015, 8(12): 2511-2519.

[30] A M S S Andrade, M L D S Martins. Quadratic-boost with stacked Zeta converter for high voltage gain applications. *IEEE J. Emerg. Sel. Top. Power Electron.*, 2017, 5(4): 1787-1796.

[31] J C Rosas-Caro, J E Valdez-Resendiz, J C Mayo-Maldonado, et al. Quadratic buck-boost converter with positive output voltage and minimum ripple point design. *IET Power Electron.*, 2018, 11(7): 1306-1313.

[32] J Chen, C Wang, J Li. An input-parallel-output-series switched-capacitor three-level boost converter with a three-loop control strategy. *Energies*, 2018, 11(10): 2631-2656.

[33] J Chen, C Wang, J Li, et al. An input-parallel-output-series multilevel boost converter with a uniform voltage-balance control strategy. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019, 7(4): 2147-2157.

Jianfei Chen received the B.S. degree from the Department of Electronic Information, Science, and Technology, Chongqing Normal University, Chongqing, China, in June 2011, and the Ph.D. degree from School of Electrical Engineering, Chongqing University, Chongqing, China, in June 2016. From January 2015 to March 2016, he served as a visiting Ph.D. student at the Department of Energy Technology, Aalborg University, Aalborg, Denmark. Since October 2016, he has been a postdoctoral researcher at Wayne State University, Detroit, Michigan, USA. His current research interests include hybrid switched-capacitor converter, multilevel converter, motor control, EV charger and wide bandgap device applications.

Kewei Ding received his B.S. degree from Hubei Institute of Automobile Industry. Wuhan, China, in 2017 majoring in electrical engineering, and his M.S. degree from Wayne State University, Detroit, Michigan, USA, in 2019, majoring in electrical engineering. His research interests include multilevel converters, DC-DC converters and DC grid. Now he is working in Shanghai Liang xiang DDG High-tech Company.

Yulin Zhong received the B.S. degree from the School of Electrical Engineering, Xi'an Jiaotong University (XJTU), China, in 1996, and the M.S. and Ph.D. degrees in power electronics from Tsinghua University, China, in 2005 and 2009 respectively. From 1996 to 2002, he worked first as an electrical engineer and later as a software engineer in Guangdong, China. During 2009-2014, he worked as an assistant researcher at the Institute of Electrical Engineering, Chinese Academy of Sciences, China. During 2014-2016 he worked as a post-doctor fellow at Ryerson University, Canada. During 2016-2018, he worked as a research scholar at Kettering University first, and later at University of Michigan Dearborn, USA. Now he is a senior system engineer of power electronics in Broad-Ocean Technologies, USA. His main research interests focus on packaging design for high power semiconductor modules, system-level structural design, circuit design, EMC design, and thermal design for EV-related applications.

Fujin Deng (S'10-M'13) received the B.E. degree in electrical engineering from the China University of Mining and Technology, Jiangsu, China, in 2005, the M.S. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2008, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2012. In 2017, he joined Southeast University, Nanjing, China, where he is currently a professor with the School of Electrical Engineering. From 2013 to 2015 and from 2015 to 2017, he was a postdoctoral researcher and an assistant professor, respectively, with the Department of Energy Technology, Aalborg University. His main research interests include wind power generation, multilevel converters, high-voltage direct-current technology, dc grids, and offshore wind farm power systems dynamics.

Sayed Abulanwar (S'12-M'16) received the B.S. and M.S. degrees in electrical engineering from Mansoura University, Mansoura, Egypt, in 2005 and 2010, respectively, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2016. He is currently an assistant professor of electrical engineering with Mansoura University. His research interests include wind turbine control, high-voltage direct-current systems, and transients in power systems.