A Novel 5-level Flying Capacitor Bridgeless PFC Converter Based on Cost-effective Low-voltage eGaN FETs*

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Abstract: In this study, a type of multilevel flying capacitor bridgeless PFC converter is proposed that permits the use of economical and efficient 100 V GaN transistors. Compared with the popular two-level totem-pole bridgeless PFC converters achieved using the much more expensive 650 V GaN devices, this new design has several distinct advantages: lower component costs, lower dv/dt, lower power losses, and reduced concerns about device reliability. A 1.6 kW, 5-level PFC converter prototype is designed and fabricated with an efficiency of 99.18% and a power factor of 0.99, which are experimentally demonstrated. The operation principle, design considerations, control strategy and experimental results are discussed.

Keywords: Bridgeless PFC converters, flying capacitor, GaN, multilevel, topology

1 Introduction

Power factor correction (PFC) converters are widely used in modern power supplies for computers, data centers, and telecommunication equipment to suppress harmonics and improve power quality [1]. Among various types of PFC topologies, the totem-pole bridgeless PFC (TPBPFC) topology reduces the number of conduction switch components from 3 to 2 compared with the boost PFC topology, thereby significantly reducing the conduction voltage drop and conduction losses. However, the TPBPFC, which uses Si SJ MOSFETs with the inherent reverse recovery of the body diode, cannot operate in the continuous conduction mode (CCM) at a relatively high frequency [2]. Operating the TPBPFC in the discrete conduction mode (DCM) to minimize the adverse impact of the body diode is an effective solution in theory. However, issues such as higher current stress on each switch and higher harmonics in the input current may arise in the DCM operation of a TPBPFC. Moreover, due to the switching frequency of the silicon-based PFC converters, which is limited to below 100 kHz, it is difficult to obtain small magnetic components and achieve a high power density. In recent years, hybrid switches (HyS) based on Si IGBT and SiC MOSFET have been studied [3]. However, the mainstream 400 V PFC design generally adopts a CCM-operated boost topology using 600 V Si SJ MOSFETs instead of the TPBPFC topology.

Wide bandgap (WBG) semiconductors such as gallium nitride (GaN) are poised to revolutionize the next generation of PFC converters. eGaN FETs of 30 to 650 V have been available for commercial use and can operate at extremely high frequencies (>1 MHz). Compared with silicon devices, GaN FETs not only eliminate the issue of reverse recovery, but also have a lower on-resistance and higher switching frequency. Therefore, to achieve a high power density and high efficiency in low-power or medium-power applications such as in PFCs, GaN FETs are considered to be a preferable choice. In recent years, TPBPFCs based on GaN HEMTs have been reported in several studies. Compared with the conventional CCM boost of PFC converters based on silicon SJ MOSFETs, the TPBPFC topology based on 650 V GaN transistors revealed

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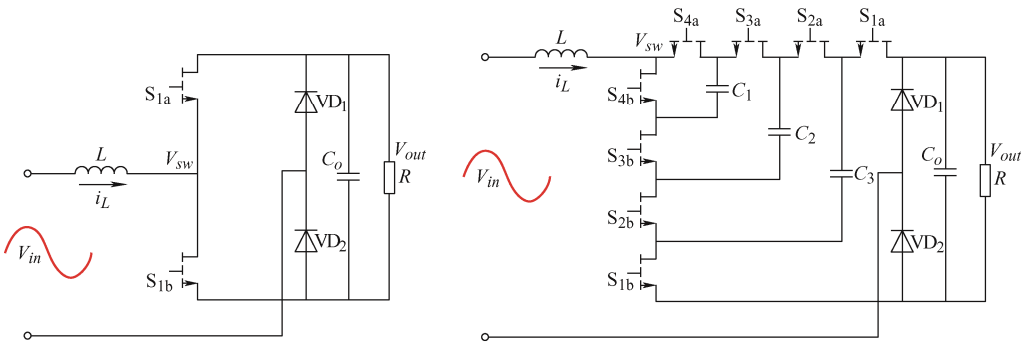
significantly lower conduction and switching losses, and could provide an efficiency of 99% even in a hard-switching design [4-6]. Although the turn-on loss of the GaN FETs is much lower than that of the Si SJ MOSFETs, this still accounts for a vital portion of the total GaN TPBPFC power losses, which restricts the switching frequency and the power density of GaN TPBPFCs [7-8]. To achieve a higher power density, a 5-level flying capacitor bridgeless totem-pole PFC (5L-TPBPFC) converter topology, which achieves a higher switching frequency, is proposed in this study. The new 5L-TPBPFC allows the use of 100 V GaN transistors and it is both economical and efficient while significantly reducing the switching loss, harmonics, and dv/dt. Moreover, the current price of 650 V GaN transistors is 5 to 8 times that of silicon transistors, while the cost of low-voltage (40 V/60 V/100 V/200 V) eGaN FETs is close to that of silicon [9]. The combination of eGaN FETs and flying capacitor technology in bridgeless PFCs also provides the following advantages：① A decrease of the inductor volume. As the level number is increased, the overall frequency of the converter can be greatly increased. Correspondingly, in high-level FC DC-DC converters, the inductor volume can be greatly reduced[10]. ② Improved reliability. The increased number of switches in multilevel converters results in redundant switching states and fault tolerance [11-12]. A reliability analysis of multilevel inverters in Ref. [13] claims that the system availability can be improved compared to 2-level systems, although a higher number of devices is required. ③ Improved EMI. As far as the influence of switching actions is concerned, a faster switching speed will generate higher EMI noise levels in the high frequency range [14]. However, in high-level FCMCs built with low-voltage GaN FETs, the voltage stress on a switch is small, the switching frequency is lower, and the EMI issue can be greatly improved. Therefore, the development of PFC converters using low-cost, low-voltage GaN FETs is highly attractive. This study provides a comprehensive introduction to the operation principles, design considerations, control strategy, and experimental results of a 1.6 kW PFC design based on this concept.

The rest of the paper is organized as follows. Section 2 presents an introduction of the proposed 5L-TPBPFC topology, along with its advantages compared to conventional topologies. Section 3 reveals the control strategy for the proposed 5L-TPBPFC. In section 4, a 1.6 kW hardware prototype is presented along with experimental results to validate our design concept. Finally, the conclusions are provided in section 5.

2 Multilevel flying capacitor TPBPFC topologies

This section compares the proposed 5L-TPBPFC converter and the popular 2L-TPBPFC converter. The specific operation and superior qualities of the 5L-TPBPFC are illustrated.

The schematic topology of the popular TPBFC based on 650 V GaN FETs is shown in Fig. 1a, while Fig. 1b exhibits the proposed 5L-TPBPFC based on 100 V GaN FETs. There is merely one semiconductor device in a traditional bridgeless topology operating at a high frequency, while the others are used in the synchronous mode. Under CCM conditions, the reverse recovery power loss of the high-frequency switch is required to be very low or even zero. The low voltage level series of GaN FETs is available for a power converter with multilevel topology. Tab. 1 compares the performances of the state-of-the-art 100 V and 650 V GaN HFETs. With a smaller figure, a switch can perform better. As shown in Tab. 1, the FOM1 of the GaN FETs represents soft- and hard-switching power losses. These losses dominate the total loss of the GaN-based PFC. The 100 V eGaN FETs have FOM1, which is one-sixteenth of that of the 650 V series. Therefore, the total loss of the PFC will be significantly reduced with the flying capacitor topology. FOM2 denotes the reverse recovery loss, which can be neglected in eGaN FETs. Therefore, via the proposed 5L-TPBPFC topology, the efficiency of this system can reach 99.18% even at high switching frequencies. Tab. 2 presents a comparison of the cost calculations between the 2-level and 5-level topologies.



(a) Conventional 2L-TPBPFC with 650 V GaN FETs

(b) Novel 5L flying capacitor TPBPFC with 100 V eGaN FETs

Fig. 1 Schematic topology of the 2L-TPBPFC and 5L flying capacitor TPBPFC

Tab. 1 Performances of the GaN FETs with different voltage levels

Voltage level	Part number	R_{on}/mΩ (T_j=25℃)	Q_{oss}/nC	FOM1 (R_{on}·Q_{oss})	Q_{rr}/nC	FOM2 (R_{on}·Q_{rr})
100 V eGaN FET	GS61004B [15]	15	11.5	172.5	0	0
	EPC2104 [16]	5	41.0	205.0	0	0
650 V eGaN FET	GS66516B [17]	25	113.0	2 825	0	0
	GS66508T [18]	50	57.0	2 850	0	0
	GS66504B [19]	100	28.3	2 830	0	0
	IGO60R070D1 [20]	70	41.0	2 870	0	0
650 V Cascode GaN FET	TP65H035WSQA [21]	41	178.0	7 298	178	7 298

Tab. 2 Comparison of the cost calculations between the 2-level and 5-level topologies

Voltage level	Part name	Unit price/¥	Quantity	Total cost/¥
2-level	650 V eGaN FETS	249.91	2	499.82
5-level	100 V eGaN FETS	31.30	8	265.40
	UUJ2D470MNQ6MS	5.00	3	

The converter is required to be adaptive to a general line voltage of 90 V to 265 V automatically in a bridgeless PFC, as well as to provide a quasi-regulated DC output-voltage V_o. The switching node voltage V_{sw} and input voltage V_{in} for the popular 2L-TPBPFC are both exhibited in Fig. 2a. As shown in Fig. 2b, the pulse width modulator with the duty cycle is calculated to obtain the control signal S. If $S = 0$, $V_{sw} =$ 0 V, and if $S = 1$, $V_{sw} = V_{DC}$. In the 5L-TPBPFC, the voltages of the flying capacitors C_1-C_3 must be maintained at $3V_o/4$, $2V_o/4$, and $V_o/4$, respectively, such that the electrical stresses on each switch are balanced. Therefore, the voltage drop on each switch is $V_o/4$. Fig. 2c exhibits five different voltage classes in which pulse width modulation (PWM) can be utilized. Consequently, the voltage pulses that are experienced by the inductor are four times less than those of the conventional boost converter. The current loop of the proposed 5L-TPBPFC is the same as that of the 2L-TPBPFC. Switches S_{1a} to S_{4b} in the 2L-TPBPFC topology can be controlled by using the phase-shifted carrier pulse width modulation (PSCPWM) signal in the linear modulation area. In the 5L-TPBPFC topology, however, switches S_1 to S_4 are controlled by the PWM signal with a duty ratio, as exhibited in Fig. 2d. Note that the phase-shifted angle from the adjacent PWM signal is 90° . In this way, the system can naturally reach equilibrium.

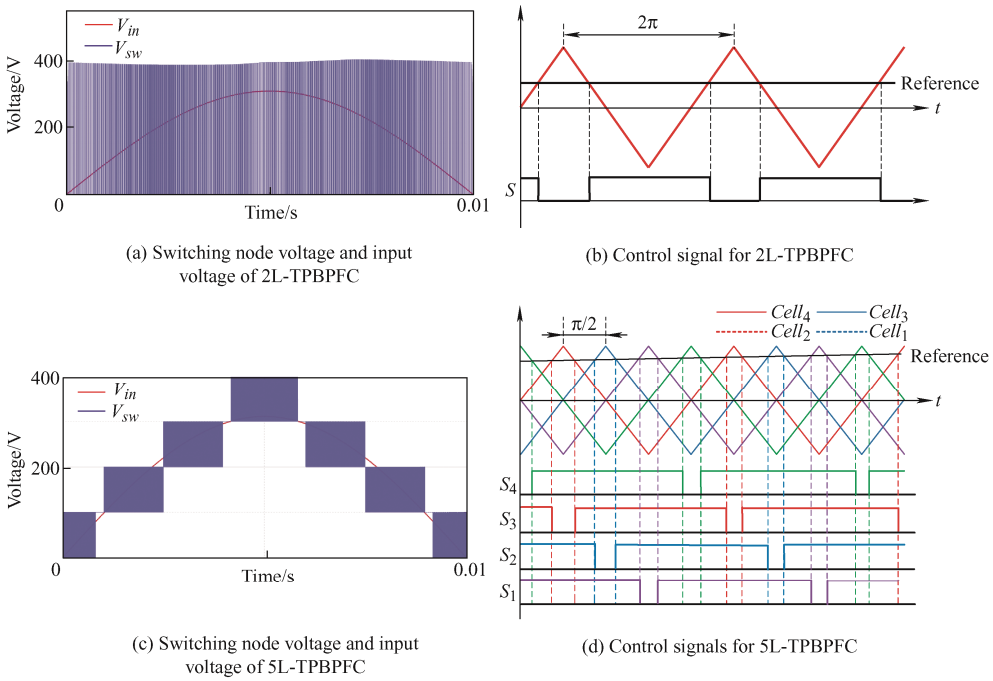
In addition, the 5L-TPBPFC topology can considerably reduce the volume of the main inductor. For a popular 2L-TPBPFC, the value L_{2L} of the main inductor is determined by the specified maximum ripple of inductor current ΔI

$$L_{2L} = \frac{V_L T_L}{\Delta I} \tag{1}$$

where V_L is the voltage drop of inductor and T_L is the

charging time. From Eq. (1), the maximum product of V_L and T_L is required to attain a maximum ΔI. Suppose that V_m represents the peak of the line voltage, I_m indicates the peak of the input current, T represents the switching period, V_o represents the output voltage, P_o represents the output power, and $\%Ripple$ represents the rate of the ripple. The value of L_{2L} can then be expressed as

$$L_{2L}=\left(\frac{1}{\%Ripple}\frac{1}{I_m}\right)V_m(D_mT)=\left(\frac{1}{\%Ripple}\frac{V_m}{2P_o}\right)V_m\left(1-\frac{V_m}{V_o}\right)T \tag{2}$$



(a) Switching node voltage and input voltage of 2L-TPBPFC

(b) Control signal for 2L-TPBPFC

(c) Switching node voltage and input voltage of 5L-TPBPFC

(d) Control signals for 5L-TPBPFC

Fig. 2 Comparison between the 2L-TPBPFC and 5L-TPBPFC topologies

Assuming that $D_m = 1-(V_m/V_o)$ represents the equivalent duty cycle, which corresponds to the peak line voltage. L_{2L} can then be further calculated as

$$L_{2L}=\frac{1}{\%Ripple}\frac{(1-D_m)^2V_o^2}{2P_o}D_mT=A(1-D_m)^2D_m \tag{3}$$

where A represents the coefficient for normalization. With an N-level topology, the voltage ripple experienced by the inductor is reduced by N−1 times and the frequency experienced by the inductor is increased by N−1 times. Therefore, L_{NL} can be expressed as

$$L_{NL}=\begin{cases}A(1-D_m)D_m\left(\dfrac{1}{N-1}-D_m\right) & 0\leqslant D_m<\dfrac{1}{N-1}\\ A(1-D_m)\left(D_m-\dfrac{1}{N-1}\right)\left(\dfrac{2}{N-1}-D_m\right) & \dfrac{1}{N-1}\leqslant D_m<\dfrac{2}{N-1}\\ \vdots & \\ A(1-D_m)\left(D_m-\dfrac{i}{N-1}\right)\left(\dfrac{i+1}{N-1}-D_m\right) & \dfrac{i}{N-1}\leqslant D_m<\dfrac{i+1}{N-1}\\ \vdots & \\ A(1-D_m)\left(D_m-\dfrac{N-2}{N-1}\right)\left(\dfrac{1}{N-1}-D_m\right) & \dfrac{N-2}{N-1}\leqslant D_m<1\end{cases} \tag{4}$$

Fig. 3 shows that the main inductor L_{NL} is determined by the maximum equivalent duty ratio D_m, the coefficient for normalization A, and the circuit level number N, as in 2L-, 3L-, 5L-, and 7L-TPBPFCs. In N-level TPBPFCs, the maximum of L_{NL} always appears in the first interval of Eq. (4), which starts from 0. Therefore, it can be expressed as

$$L_{NL\,\max}=\max[A(1-D_m)D_m(\frac{1}{N-1}-D_m)]\quad 0\leqslant D_m<\frac{1}{N-1} \tag{5}$$

It is known that the multilevel topologies can significantly reduce L_{NL}. Furthermore, the volume of the magnetic components can be reduced while the power density of the system can be significantly increased.

The area product theory [22] can be used to estimate the volume of an inductor. Moreover, the inductor core volume V can be expressed as a function of a constant K and the area product A_p

$$V=KA_p^{0.75}=K\left(\frac{2W(10^4)}{B_mJK_u}\right)^{0.75} \tag{6}$$

where B_m is the flux density, J is the current density, K_u is the window utilization factor, and W is the energy stored in an inductance. W can be expressed as

$$W = 0.5L \times I_m^{\ 2} \tag{7}$$

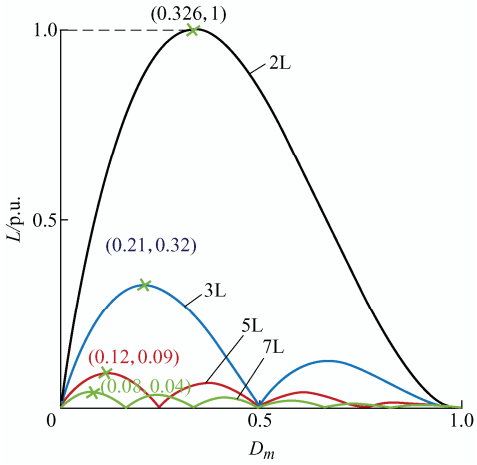


Fig. 3 Relationship between the peak equivalent duty ratio D_m and the main inductance L_{NL} (p.u.) for 2L-, 3L-, 5L- and 7L-TPBPFCs

The inductor core volume V can be estimated by considering the required energy of an inductor, as expressed by Eq. (7). L is the value of the inductance. Furthermore, Eq. (7) can also be expressed for an N-level TPBPFC and 2L-TPBPFC as

$$W_{NL} = 0.5L_{NL} \times I_m^{\ 2} = 0.5L_{2L} \left(\frac{\frac{1}{N-1} - D_m}{1 - D_m} \right) \times I_m^{\ 2} \tag{8}$$

By considering L_{2L} as a reference, the required inductor core volume of an N-level TPBPFC may be expressed as follows

$$\frac{V_{NL}}{V_{2L}} = \left(\frac{1-(N-1)D_m}{(N-1)(1-D_m)} \right)^{0.75} \tag{9}$$

Therefore, the required inductor core volume in an N-level TPBPFC can be reduced compared to the 2L-TPBPFC.

Fig. 4 shows the reduction of the inductor core volumes in the 3L-, 5L-, and 7L-TPBPFCs, which are approximately 65%, 87.5%, and 93.2%, respectively, with respect to the 2L-TPBPFC. The comparison of the inductor volumes between the 2-level and 5-level topologies is shown in Fig. 5. It is obvious that the volume of inductance is significantly reduced as the number of levels is increased.

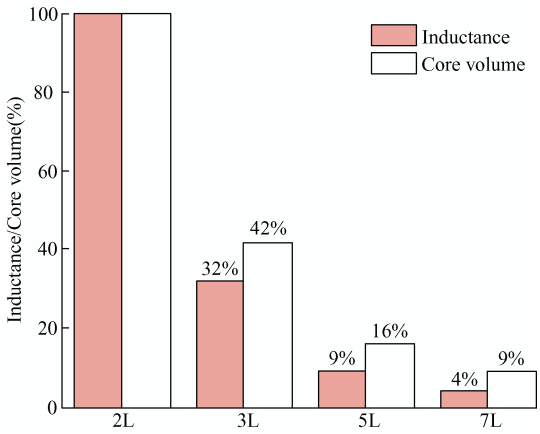


Fig. 4 Reduction of inductance and inductor core volumes in the 3L-, 5L- and 7L-TPBPFCs compared to the 2L-TPBPFC

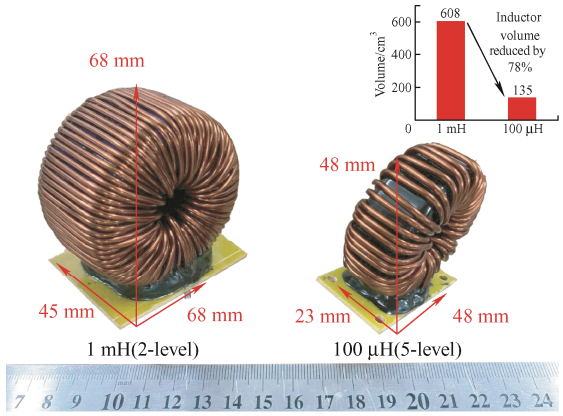


Fig. 5 Comparison of the inductor volumes between the 2-level and 5-level topologies

Therefore, the inductance and core volume of the boost inductor are reduced when a multilevel TPBPFC with a higher number of levels is considered compared to the 2L-TPBPFC. Consequently, the size and weight of the converter is reduced.

3 Control strategy

The 5L-TPBPFC enables improved power density and efficiency, while its distinct characteristics may change the parameters of the PFC. In this section, we will analyze the control performance of the PFC while considering the influence of parameter variations.

The control block diagram of 5L-TPBPFC is shown in Fig. 6. The system specifications are listed in Tab. 2. It is known that the control scheme consists of two control loops that are based on the average current control. The outer loop manages the load voltage by regulating the value of the current reference, while the inner loop is designed to control the inductor current i_L to follow the current reference. The PFC can realize a

close-to-unity power factor and steady load voltage with these two control loops.

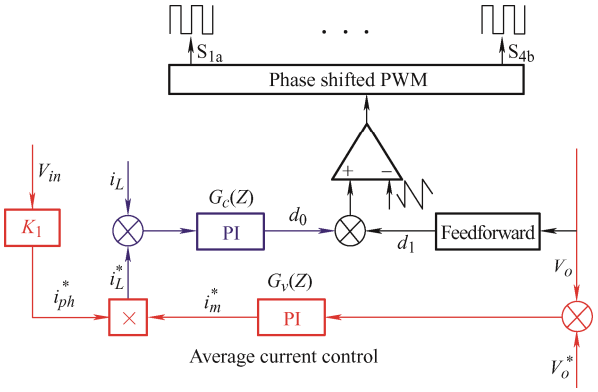


Fig. 6 Control scheme of a 5L-TPBPFC with a double closed-loop

The small signal transfer function from the duty ratio to the inductor current can be calculated as [23]

$$\begin{cases} K=\dfrac{2V_o}{R(1-D)^2}\dfrac{1+\dfrac{sRC}{2}}{1+\dfrac{sL}{R(1-D)^2}+\dfrac{s^2LC}{(1-D)^2}} \\ G_{iLd}=\begin{cases} \dfrac{i_L}{d_{bottom}}=K \quad V_{in}>0 \quad d_{top}=0 \\ \dfrac{-i_L}{d_{top}}=K \quad V_{in}<0 \quad d_{bottom}=0 \end{cases} \end{cases} \tag{10}$$

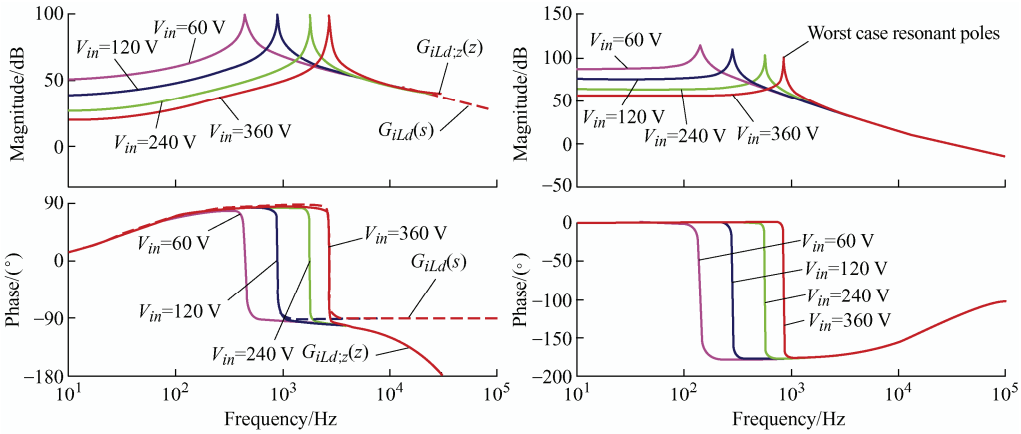
where V_{in} is the input voltage, V_o is the load voltage, R, C and L are the resistance, inductance and capacity in the circuit, respectively. Moreover, d_{top} and d_{bottom} are the duty ratios of the top and bottom switches, respectively.

Eq. (10) is calculated using the system specifications listed in Tab. 3 and shown in Fig. 7a. Due to the digital controller, there is a phase lag, which is shown as $G_{iLd;z}$ in Fig. 7a. Therefore, we will discuss a discrete model $G_{iLd;z}$. A type-II compensator represented as $G_{c;z}$ is adopted in the current loop to improve the feedback loop. The loop gain after compensating is shown in Fig. 7b.

As shown in Fig. 7b, for $G_{iLd;z}$, a pair of resonant poles (f_r) appear near 1 kHz. For a traditional PFC with a boost topology, the main inductor L is usually large (e.g., mH), resulting in a worst case f_r below 50 Hz. Therefore, the gain at the line frequency is not affected. However, for the PFC presented in this study, the main inductor is greatly reduced. Therefore, the worst resonant pole frequency f_r in this case may appear above 50 Hz, leading a significant reduction of the loop gain at the line frequency. Additionally, i_L may undergo a significant phase shift and distortion with respect to V_{in}. To overcome these issues, a type-II compensator is adopted in the inner loop. In this way, the compensated loop gain remains flat on the left side of f_r and the loop gain at the line frequency is above 50 dB. Therefore, the input current may better follow the reference value. Moreover, the disturbance from the input voltage can be effectively rejected with such a high gain [24].

Tab. 3 System specifications

Parameter	Value
Input AC voltage (50 Hz)/V	110, 220
Output DC voltage/V	400
Transistor switching frequency/kHz	100
Effective switching node frequency/kHz	400
Input inductor L/μH	100
Output capacitor C_o/μF	1 500
Power factor	0.99



(a) Uncimoensated inner loop gain $Gud(s)$ and $G_{iLd;z}(z)$ (b) Compensated inner loop gain $G_{c;z(z)}$ $G_{iLd;z}(z)$

Fig. 7 Loop gain of the inner feedback loop

4 Experimental results

To verify our design experimentally, a 5L-TPBPFC prototype was built, as shown in Fig. 8. The system specifications are listed in Tab. 3. The controller is based on an Artix-7 100T AX7102. To analyze the operation characteristics of the 5L-TPBPFC topology, the converter is operated under two kinds of inputs, i.e., 220 Vrms, 50 Hz, and 110 Vrms, at 50 Hz conditions.

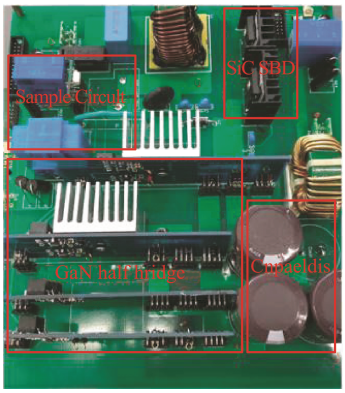


Fig. 8 Hardware circuit of the 5L-TPBPFC converter

Fig. 9 shows the experimental waveforms of system states: V_{in} (input voltage), V_o (output voltage), i_L (input current), and V_{sw} (switching node voltage) under various input AC voltages. As shown in Fig. 9, the output DC voltage is boosted to 400 V and the switching node voltage V_{sw} shows a staircase waveform with 100 V increments and a weak imbalance. Under an input of 220 Vrms and 50 Hz, the V_{sw} transitions through 5 levels from 0 V to 400 V and follows the trajectory of the rectified input voltage V_{in}. Under an input of 110 Vrms and 50 Hz, only 3 levels are available because the peak value of V_{in} is less than that of the third level. Note that in the different half cycles of V_{in}, the power devices in the top or bottom bridge arms alternately operate as the main switch. The switches in the top and bottom bridge arms are therefore complementary. Thus, when V_{in} is in the positive half cycle, V_{sw} is in the negative half cycle. Therefore, a voltage jump occurs when V_{sw} crosses zero.

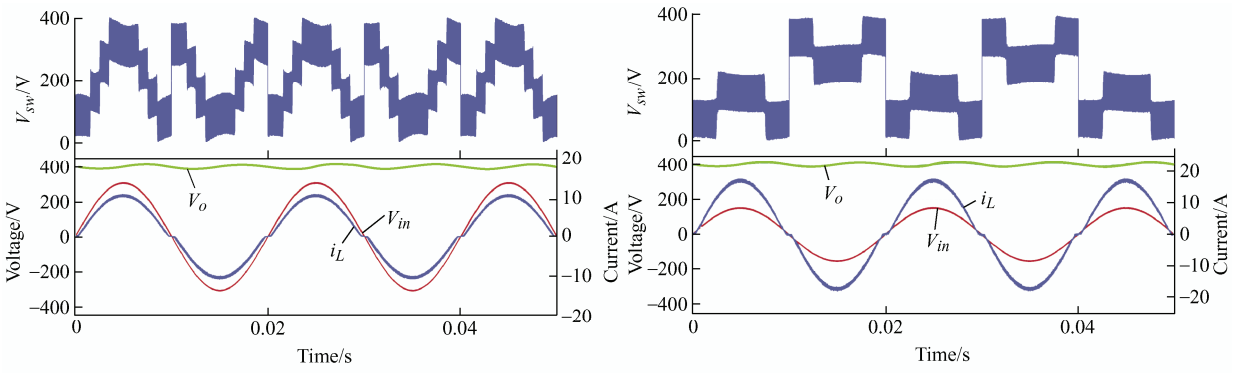


Fig. 9 Measured 5L-TPBPFC prototype waveforms: V_{in} (input AC voltage), V_o (output DC voltage), i_L (inductor current) and V_{sw} (switching node voltage) under different input voltage conditions

Fig. 10 shows the efficiency of the 5L-TPBPFC under high and low input conditions. The power losses consist of the consumptions of the passive components and power switches. Note that the power loss of the driver circuit is neglected. Under high input conditions, a peak efficiency of 99.18% occurs at 1 kW. Under low input conditions, the peak efficiency occurs at 0.6 kW, which is 98.04%.

Fig. 11 shows the PF curve and the input current's THD curve of the 5L-TPBPFC topology under input voltages of 100 V and 220 V, respectively. It can be seen in Fig. 11a that the PF of the converter under a full-load operation is always above 0.99 under the two different voltages. In Fig. 11b, it can be seen that the THD of the converter under a full-load operation is always under 5% under the two different voltages. Furthermore, the minimum values of the THD are 3.2% and 2.5% under 220 and 110 V, respectively. The 5L-TPBPFC design concept is therefore verified by the collected prototype data.

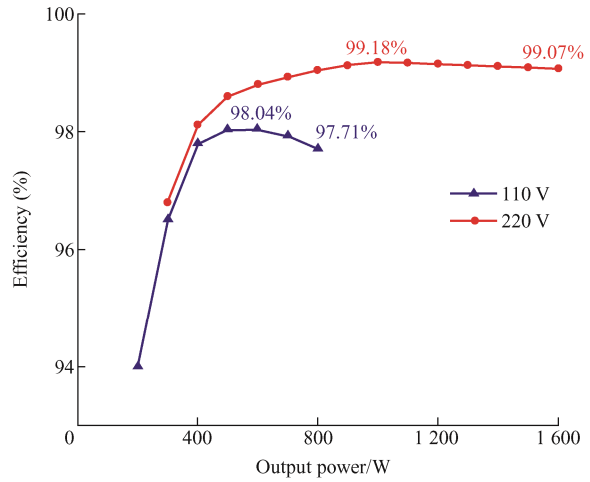
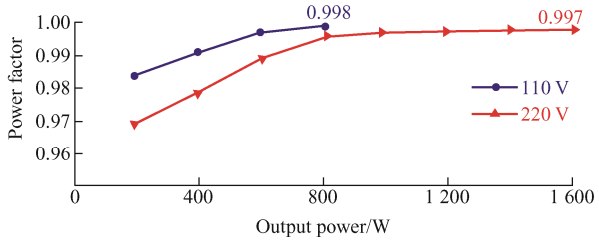
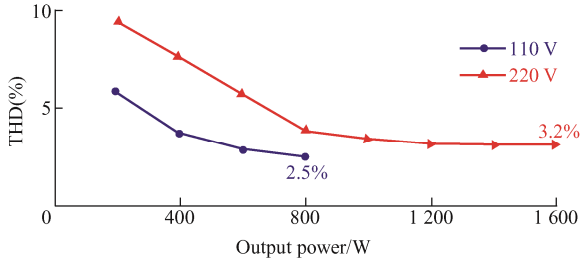


Fig. 10 Efficiency of the 5L-TPBPFC versus the output power under a low input condition (110 V) and high input condition (220 V)



(a) PF curves under input voltages of 100 V and 220 V



(b) THD curves under input voltages of 100 V and 220 V

Fig. 11 PF curve and the input current's THD curve of the 5L-TPBPFC topology under input voltages of 100 V and 220 V

5 Conclusions

This study proposed a type of multilevel flying capacitor bridgeless PFC converter that permits the use of cost-effective 100 V GaN transistors. This new design has several distinct advantages compared with the conventional 2L-TPBPFC converters with 650 V GaN devices, including a reduced dv/dt, reduced component costs, lower power losses, and improved device reliability. A 1.6 kW, 5L-TPBPFC prototype was designed and implemented, and it was experimentally demonstrated to possess a close-to-unity power factor and an efficiency of 99.18%.

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