Implementation of 1.7 kV Silicon Carbide Metal Oxide Semiconductor Field Effect Transistors in Auxiliary Power Supplies for Industrial Applications

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Abstract: An auxiliary power supply (Aux-PS) has become an essential component of electronic equipment for many industrial applications, such as in motor drives, photovoltaic (PV) inverters, uninterruptible power supply (UPS) systems and modular multilevel converters. The introduction of 1 700 V silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) is useful for such applications, providing benefits with respect to a low on-state resistance, smaller package, low switching loss and single-switching implementation. A single end flyback Aux-PS is designed for industrial applications with a wide input voltage range using 1.7 kV SiC MOSFETs. The special design tradeoffs involved in the usage of SiC MOSFETs are discussed in detail, such as those with regard to gate driving voltage selection, isolation transformer design considerations, and clamping circuit design details. A 60 W demonstration hardware is developed and tested under different working conditions. The results verify the higher efficiency and better thermal performance of the proposed hardware relative to those of traditional Si solutions.

Keywords: Silicon carbide, MOSFET, wide input range, auxiliary power supply

1 Introduction

Silicon carbide (SiC) power metal oxide semiconductor field effect transistors (MOSFETs) have emerged as ideal candidates for helping to meet increasing demands for efficiency, power density, reliability, and lower cost in power electronics systems[1]. SiC MOSFETs are unipolar devices and demonstrate a low on-state voltage drop, low terminal capacitance, and dramatically lower switching losses as compared to similarly rated silicon insulated gate bipolar transistors. SiC MOSFETs bring the advantages of high-speed unipolar devices into much higher voltage classes than those achievable with silicon devices. SiC devices have superior performance over Si devices, and provide potential opportunities for high efficiency, high power density, high performance, and low-cost converter systems design.

An auxiliary power supply (Aux-PS) has become an essential part of electronic equipment in many industrial applications, such as motor drives, photovoltaic inverters, uninterruptible power supply systems, and modular multilevel converters. These low-power isolated switched model power supplies convert a high-voltage dc bus to a low voltage (5-48 V) source for powering driving circuits, control circuits, sensing circuits, cooling fans, etc. These power supplies usually operate in a wide input voltage range (typically from 300 V up to 1 000 V), owing to the dc link voltage variation. A simple, low-complexity design is usually required to ensure reliability and low cost simultaneously. A single-switch flyback topology is the most common selection, owing to its simple structure, lowest component count, and low cost. However, there are many challenges in using silicon MOSFETs for Aux-PS applications with high input voltages [2-4]. There are two main drawbacks to the flyback topology. One is that the output voltage will be reflected to the primary side of the transformer and added to the primary switch. Therefore, the flyback topology requires a higher voltage rating for the power

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switching device. Another drawback is that the leakage inductance of the transformer will induce a high voltage spike during device turn-off; a clamping circuit is required to limit the voltage spike. For a 1 000 V DC input maximum input, even 1 500 V-rated Si MOSFETs will have a limited margin for clamping circuit design, and the limited maximum voltage margin also raises reliability concerns [5]. In contrast, 2 000 V and above-rated Si MOSFETs can provide a sufficient margin, but the specific "on" state resistance is much higher than that of lower-voltage MOSFETs, which reduces the converter efficiency and compromises heat management. This may require larger cooling solutions with forced air cooling even for low power conversion applications, compromising the cost, size, and reliability. Meanwhile, the cost of 2 000 V and above rated MOSFET is even higher than SiC MOSFETs, owing to their limited availability. Two-switch flyback and other topologies have been proposed to utilize lower-voltage Si MOSFETs, but the design complexity and converter component counts increase significantly. The introduction of 1 700 V SiC MOSFETs provides a good solution for such applications. The 1 700 V breakdown voltage provides enough voltage margin for the 1 000 V input voltage. The specific "on" resistance of 1 700 V SiC MOSFETs is much lower than that of 2 000 V and above-rated Si MOSFETs, allowing for a smaller die size. Therefore, smaller packages can be used for more compact designs. For the same die size, the on-state resistance is much lower than that of high-voltage Si MOSFETs; therefore, the conduction loss can be reduced. Moreover, SiC MOSFETs also have lower switching losses, which can improve the converter efficiency and reduce the size of the heatsink, or even remove the need for a heatsink, providing cost reduction and reliability improvement[6]. Lower switching losses also provide an option to increase the switching frequency of the Aux-PS to further reduce transformer size and weight. This study presents the design of a single end flyback Aux-PS for industrial applications with a wide input voltage range, using 1.7 kV SiC MOSFETs. The special design tradeoffs involved while using SiC MOSFETs are discussed in detail, such as the gate driving voltage selection, isolation transformer design considerations, and clamping circuit design details. A 60 W demonstration hardware is developed and tested under different working conditions. The results verify the higher efficiency and better thermal performance of the proposed hardware as compared with traditional Si solutions.

2 Converter design summary

The design of a SiC MOSFET-based single-switch flyback converter is similar to the design of a Si MOSFET-based single-switch flyback converter. Key components of the single-switching flyback converter include the primary side SiC MOSFET, transformer (TX), primary side SiC switch, clamping circuit, controller integrated circuit (IC) and its configuration circuits, control power regulation circuit, and output rectification circuits. Fig. 1 presents a schematic of the single-switch flyback converter demonstrated in this study.

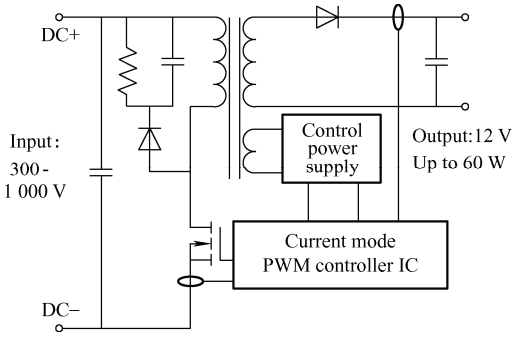


Fig. 1 Single-switch flyback converter

There is a wide selection of IC controllers available for industrial Aux-PS applications. In this study, the TI UCCx8C4x family current mode pulse width modulation (PWM) controller is selected. To select the proper device part number, the under voltage lock out (UVLO) protection level and maximum duty cycle must be calculated. Considering the relatively high gate driving voltage requirements for SiC MOSFETs, a high UVLO protection function is preferred. Meanwhile, the maximum duty cycle of the demo converter can be calculated from the voltage transfer function of a continuous conduction mode (CCM) flyback converter, as follows

$$D_{\max} = \frac{N_{\mathrm{ps}} \times V_{\mathrm{out}}}{V_{\mathrm{in\_min}} + N_{\mathrm{ps}} \times V_{\mathrm{out}}} = 0.336\,9 \tag{1}$$

where $D_{\max}$ is the maximum duty cycle, N_{ps} is the turn

ratio of the primary to secondary side of the transformer, V_{out} is the output voltage, and V_{in_min} is the minimum input voltage. As D_{max} is less than 50%, the UCC28C44 is selected for this evaluation board design. The low switching loss energy and ultra-low gate charge features of SiC MOSFETs allow for a higher switching frequency, for a more compact transformer design. The switching frequency is a key design variable for an Aux-PS. A higher switching frequency will increase the power device switching loss and core loss per volume of the transformer, but can reduce the transformer volume and weight, therefore benefitting the transformer core loss and total system weight. The switching frequency should also be selected in consideration of the converter level electrical magnetic interference (EMI) emissions. Many EMI standards start from 150 kHz. There are certain preferred switching frequencies for simpler EMI filter designs. For this evaluation board, a pre-design is performed, based on simplified circuit simulation models for switching frequencies of 74 kHz, 110 kHz, and 148 kHz. A pareto analysis between converter size and efficiency is performed, and the switching frequency is selected at f_s=110 kHz. A 150 V Si Schottky diode (DSA30C150PB) is selected as the output rectification diode.

There exist some special design considerations that must be made owing to the special features of SiC MOSFETs. SiC MOSFETs require a higher gate-driving voltage than Si MOSFETs. An off-the-shelf controller IC usually cannot provide the recommended gate-driving voltage for SiC MOSFETs, and a proper gate driving voltage selection is required. Moreover, the high switching speed of SiC MOSFETs requires a low primary side to secondary side isolation capacitance, to limit conductive common mode (CM) noise emissions. However, designing for a low isolation capacitance may increase the transformer leakage inductance. A higher leakage inductance will lead to higher energy stored in the leakage inductor. This energy is dissipated in a resistor-capacitor-diode (RCD) clamping circuit. If the transformer leakage inductance is large, the loss on the RCD clamping circuit might be high, and the efficiency might be compromised. The balance of a lower isolation capacitance and lower leakage inductance needs to be considered for transformer design. This paper discusses these special design tradeoffs in detail and also provides experimental test results in the following sections.

3 Driving voltage selection

A 1.7 kV 1 ohm SiC MOSFET has an ultra-low input capacitance; therefore, the gate charge needed for device switching is also very low. The PWM controller IC is capable of driving the 1.7 kV 1 ohm SiC MOSFET directly, without a dedicated gate driver. The maximum driving voltage of the PWM controller IC is usually lower than the recommended 20 V gate-driving voltage for SiC MOSFETs. Driving an SiC MOSFET with a lower gate voltage will slightly increase the on-state resistance, and the on-resistance increase will be less significant at higher temperatures [7-8]. Fig. 2 shows the on-resistance changes with temperature at different gate driving voltages. Compared with the recommended 20 V driving voltage, a 16 V driving voltage will increase the on-state resistance by 30% at 25 ℃, but will only increase the on-state resistance by 10% at 175 ℃. Moreover, a lower driving voltage can also reduce the peak current during a device short circuit. This will significantly improve the device short circuit withstand time; therefore, it can improve the system ruggedness under fault conditions.

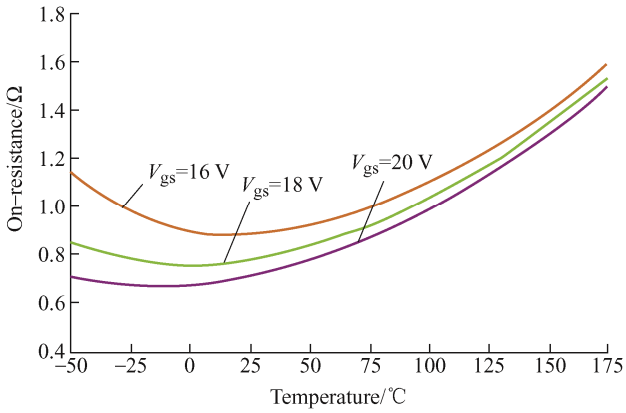


Fig. 2 On-state resistance change with temperature at different gate driving voltages

However, if the driving voltage is too low, the device may saturate at a lower current, and fail to support a high peak current [9]. Fig. 3 shows the measured short circuit performance of the SiC MOSFETs at a 960 V DC voltage under different driving voltages. The results indicate that the

maximum current is more dependent on the driving voltage. A lower driving voltage will limit the maximum power delivery of the flyback converter. Moreover, many controller ICs have overcurrent protection functions, based on sensing a MOSFET's peak current under overload conditions. If the driving voltage is too low, the MOSFET's peak current will be limited. Under overload or short circuit conditions, the peak current may not be able to trigger the protection threshold of the driver IC. This would result in a loss of protection during overload conditions, and the device might be damaged owing to overheating.

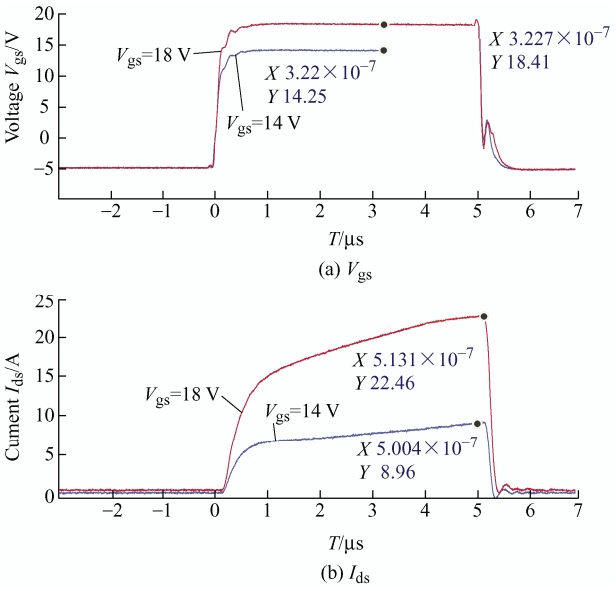


Fig. 3 A 1.7 kV SiC MOSFET at 960 V DC voltage under different driving voltages

SiC MOSFETs have ultra-low gate input capacitances, owing to their small die sizes; the total gate charge of the LSIC1MO170E1000 device is only 15 nC. Even with a 20 V/−5 V driving voltage and 110 kHz switching frequency, the driving loss is less than 45 mW, which is negligible (less than 0.6%) compared with the power device and transformer losses.

The maximum driving voltage limitation of the selected driver IC is 20 V. In consideration of a margin for handling transient voltage changes, an 18 V driving voltage is selected for this evaluation board. Compared with a 20 V driving voltage, an 18 V driving voltage will increase the on-state resistance by 3.5% at 125 ℃. With an 18 V driving voltage, the MOSFET can still support a high peak current, ensuring a high-power delivery and triggering the IC short circuit protection function under overload conditions.

The selection of a suitable gate resistor value is a tradeoff between switching losses, switching speed, and EMI noise emissions. A smaller gate resistance can increase the power MOSFET switching speed and reduce switching loss; conversely, a larger gate resistance can reduce the converter EMI noise emissions. For SiC MOSFETs, the turn-on loss is usually higher than the turn-off loss with the same gate resistance. Therefore, it is recommended to employ different turn-on and turn-off resistances, i.e., a smaller turn-on resistance for turn-on loss reduction, and a larger turn-off resistance to reduce voltage ringing and EMI noise emissions. Considering the internal gate resistance of the SiC MOSFET and the peak output current capability and output impedance of the PWM controller, a 10 ohm turn-on resistance and 20 ohm turn-off resistance are selected. Moreover, it is also very critical to optimize the actual layout of the gate loop. The key design target is to reduce the gate loop inductance and avoid near-field coupling, so as to reduce gate ringing and avoid high peak gate voltages.

4 Transformer and clamping circuit design considerations

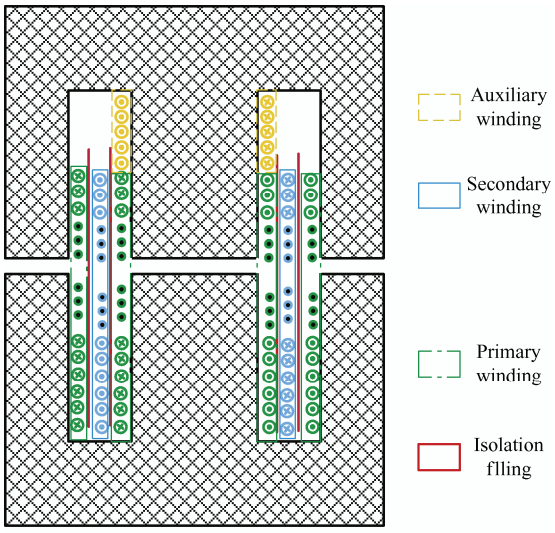
The transformer is the key passive component in the design, for ensuring the proper operation of the entire converter. The core material and winding wire selection determine the power loss and temperature rise of the transformer. The magnetizing inductance will determine the continuous current mode operation region. A larger magnetizing inductance can extend the continuous current mode operation region for a smaller current ripple and lower conduction loss, but will also increase the leakage inductance. Moreover, owing to the high switching speed of the SiC MOSFET, a low primary side to secondary side isolation capacitance is needed to limit CM noise emissions. Designing for a low-isolation capacitance will also increase the transformer leakage inductance. In a flyback converter design, the leakage inductance will influence the voltage ringing and peak voltage on the power MOSFET, and will also determine the power loss in the RCD clamping circuit design. Both the leakage inductance and isolation capacitance are

related to the winding structure of the transformer. The leakage inductance tends to be smaller when all of the windings are closely coupled with each other; thus, concentrically winding is performed around the same core leg, to improve coupling [10-12]. In contrast, the isolation capacitance is a function of the overlapping area and distance between the primary and secondary windings. The isolation capacitance can be reduced when the primary and secondary windings are far away from each other [13-14].

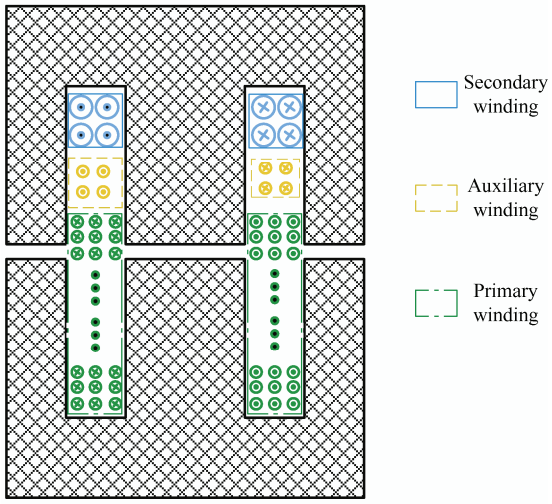
Fig. 4 shows two winding structures for the transformer, to achieve different design targets. Structure 1 separates the primary winding and secondary winding, to ensure a good isolation between them. The distance between the primary and secondary/auxiliary windings is controlled to ensure the insulation. No isolation filling is required with a sufficient airgap. A high potential test was performed to ensure the 2 500 V insulation voltage between windings. This design can reduce the isolation capacitance between the primary side and secondary side. Therefore, it can limit the converter CM EMI emissions. However, the separated winding will result in a large leakage inductance for both the primary and secondary sides. The large leakage inductance will increase the device voltage ringing and CM noise source and will compromise the benefit of the lower isolation capacitance. The large leakage inductance will also increase the energy loss of the RCD clamping circuit, and reduce the converter efficiency.

Structure 2 interleaves the secondary winding and primary winding to minimize the leakage inductance; however, the overlapping between the primary and secondary windings will significantly increase the isolation capacitance. SiC MOSFETs have faster switching speeds, and the higher isolation capacitance of the transformer will increase the CM noise current from the primary side to the secondary side. To reduce this isolation capacitance, an isolation filling layer is recommended, so as to increase the physical distance between the windings.

Two inductors were fabricated with the same 1.2 mH primary-side magnetizing inductance. The isolation capacitances were measured using an impedance analyzer. The results verify that structure 1 has a 61 μH leakage inductance and a 10 pF isolation capacitance. Structure 2 has only a 9.2 μH leakage inductance, but the isolation capacitance is 52 pF, even with the isolation filling layer.



(a) Separated primary winding and secondary winding

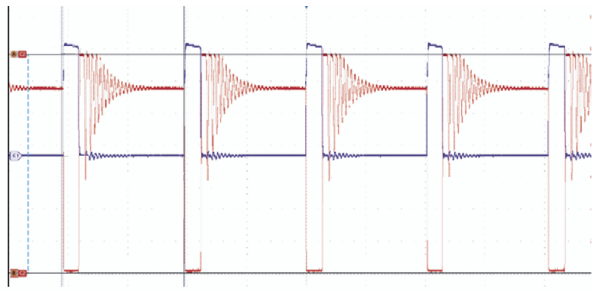


(b) Interleaved secondary winding and primary winding

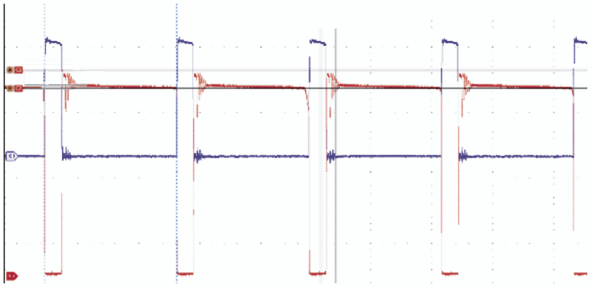
Fig. 4 Two winding structures for the transformer

Fig. 5 presents the switching waveform of the demo hardware at the 1 000 V full-load condition, using the two transformers (with the same clamping circuit parameters V_{gs}=10 V/div, V_{ds}=200 V/div). The MOSFET peak voltage reached 1.368 kV with the structure 1 transformer, i.e., with the high leakage inductance design. By reducing the leakage inductance using structure 2, the MOSFET peak voltage was reduced to 1.214 kV; meanwhile, the drain-to-source voltage ringing was also reduced, and the ringing frequency was shifted. This changed the CM and differential mode (DM) noise source and also changed the system-level EMI filter design. Moreover, the efficiency of the power converter also increased by

using the transformer with the lower leakage inductance. These results are shown in the next section.



(a) Device wavefoms at 1 000 V in full load with structure 1 transformer



(b) Device wavefoms at 1 000 V in full load with structure 2 transformer

Fig. 5 Switching waveform of the demo hardware at the 1 000 V full-load condition using the two transformers

In flyback topology, during the turn-off period, the rise of the primary side voltage charges any circuit capacitance, including the output capacitance of the MOSFET, in a relatively short time. When the primary voltage across the MOSFET exceeds the input voltage plus the reflected output voltage, the secondary side diode conducts, and the voltage across the transformer primary is approximately clamped to the reflected output voltage. However, the turn-off of the MOSFET interrupts current through the leakage inductance of the transformer, causing a voltage spike on the MOSFET. The inductance will resonate with stray circuit capacitances, and produce large-amplitude, high-frequency ringing. This excessive voltage owing to resonance should be suppressed to an acceptable level by an RCD clamping/snubber circuit, as shown in Fig. 1. The RCD snubber circuit absorbs the energy from the leakage inductance resonance by forward biasing the diode when the device drain source voltage is higher than the input voltage plus the reflected output voltage. If the snubber capacitance is large enough, the voltage can be assumed as constant during one switching period.

The simplified MOSFET drain-to-source voltage waveform is shown in Fig. 6. $V_{\text{reflected}}$ is the voltage reflected from the secondary side, and V_{x} is the voltage owing to the energy stored in the snubber capacitor.

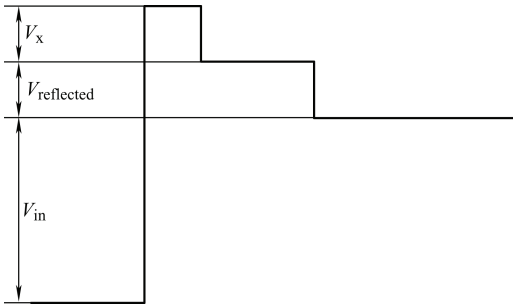


Fig. 6 Simplified V_{ds} waveform with RCD clamping circuit

To design the snubber circuit, the leakage inductance of the transformer needs to be measured. It is recommended to use the leakage inductance measurement result at the switching frequency to estimate the energy stored in the leakage inductance.

$$P_{\text{leak}} = \frac{1}{2} \times L_{\text{leak}} \times I^2{}_{\text{MOS\_max}} \times f_{\text{s}} \tag{2}$$

where P_{leak} is the power loss owing to the leakage inductance, L_{leak} is the leakage inductance, $I_{\text{MOS\_max}}$ is the maximum current through the MOSFET, and f_{s} is the switching frequency. Then, the power dissipated by the RCD clamp components can be calculated as follows

$$P_{\text{clamp}} = P_{\text{leak}} \times \left(1 + \frac{V_{\text{reflected}}}{V_{\text{in\_max}}}\right) \tag{3}$$

where P_{clamp} is the power loss on the clamping circuit, P_{leak} is the power loss owing to the leakage inductance, $V_{\text{reflected}}$ is the reflected voltage, and $V_{\text{in\_max}}$ is the maximum input voltage. SiC MOSFETs provide a higher margin of V_{max}; therefore, using SiC MOSFETs can allow for a lower snubber loss with the same leakage inductance.

The resistor value is critical in determining the peak voltage, as follows

$$R_{\text{clamp}} = \frac{\left(V_{\text{reflected}} + V_{\text{x}}\right)^2}{P_{\text{clamp}}} \tag{4}$$

where R_{clamp} is the clamping resistance, $V_{\text{reflected}}$ is the reflected voltage, V_{x} is the voltage owing to the energy stored in the snubber capacitor, and P_{clamp} is the power loss on the clamping circuit. The actual capacitance value is not critical in the snubber circuit design, but

its value should be large enough to keep a small voltage ripple while absorbing the leakage energy. By considering 10% of the voltage ripple on the snubber capacitor, the capacitance can be calculated as follows

$$C_{\text{clamp}} = \frac{1}{10\%} \times \frac{1}{R_{\text{clamp}} \times f_{\text{s}}} \tag{5}$$

where C_{clamp} is the clamping capacitance, R_{clamp} is the clamping resistance, and f_{s} is the switching frequency.

5 Performance comparison

To verify the proposed design and demonstrate the high performance of the 1 700 V SiC MOSFET, a 60 W single-end Flyback Aux-PS was developed. Fig. 7 presents the demonstration hardware.

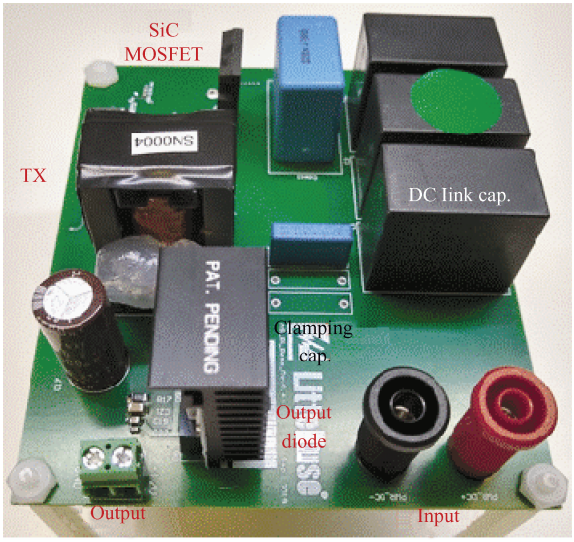
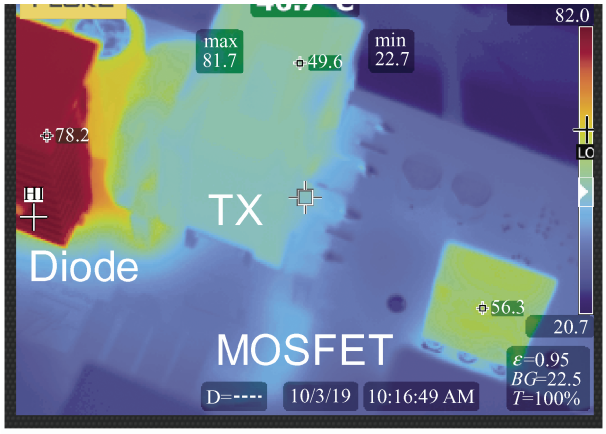


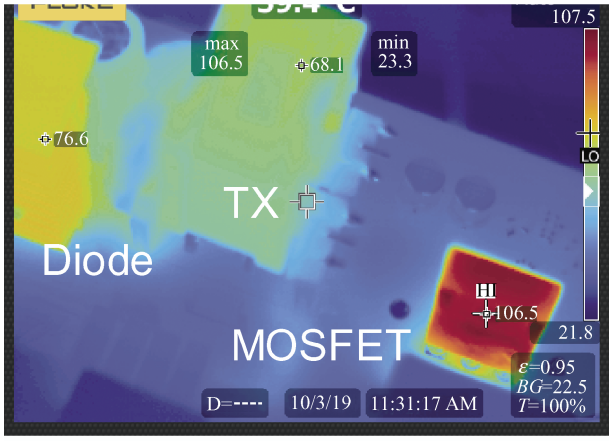
Fig. 7 60 W demonstration hardware

The demonstration hardware was tested with a digitally controlled dc power supply and an electronic load. The test conditions were as follows: input voltage V_{in} = 300-1 000 V, output load P_{load} = 5-60 W. The efficiency of the power converter was monitored by using a power analyzer to measure the input and output voltage and current. The temperatures of key components were measured using a thermal camera.

Figs. 8a and 8b present the thermal performance of the designed hardware under a full load with different input voltages. The highest temperature of the SiC MOSFET is measured at 1 000 V input voltage. The temperature is only 106.5 ℃ with natural convection cooling and with no heatsink attached to the MOSFET, indicating that the converter is capable of handling more power if a heatsink is attached. Fig. 9 summarizes the temperature changes with different input voltages under a full load. The transformer temperature rise is only 60 ℃ and is not sensitive to the input voltage, as the wingding loss reduction compensates for the core loss increase when the input voltage increases. The output diode temperature rise increases with an input voltage increase, but it is less dependent thereon, as there is a heatsink attached to the output diode. The maximum temperature is above 78 ℃. This can be further reduced by using a Si MOSFET with a synchronous rectifier controller IC.



(a) Thermal image at V_{in}=300 V, 100% load



(b) Thermal image at V_{in}=1 000 V, 100% load

Fig. 8 Thermal performance of the designed hardware under a full load with different input voltages

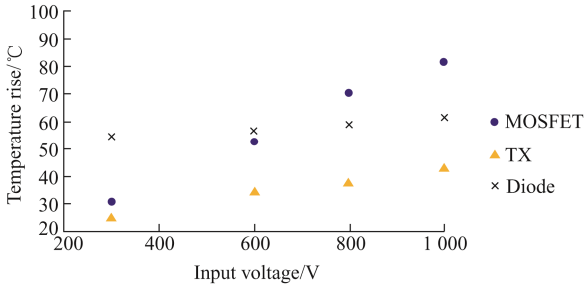
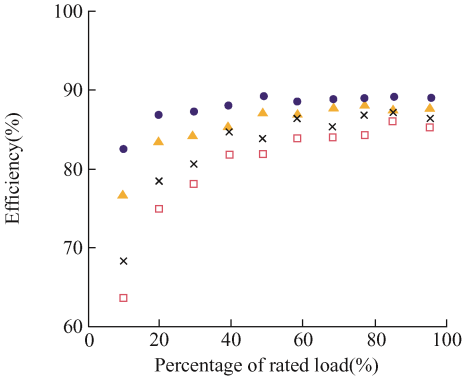


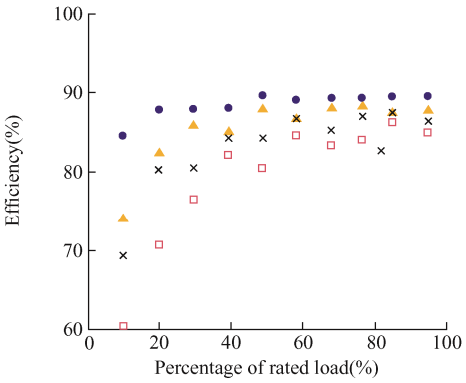
Fig. 9 Temperature rise vs. input voltage under full load

Figs. 10a and 10b present efficiency measurements

under different loads and different input voltage, with two different transformers. The converter efficiency is more than 80% above a 40% load for all input voltage conditions. A peak efficiency of 90.1% is achieved at a 300 V input voltage and 50% load. The platform was also tested with a 1 500 V 5 Ω N-channel Si MOSFET. Without a heatsink, the Si MOSFET could not deliver full power, owing to device overheating. The Si MOSFET reaches 150 ℃ at 30 W within 5 mins, and the measured efficiency is only 73%. With a heatsink and forced air-cooling added, the Si MOSFET can deliver 60 W of power, but the efficiency is only 70%, and the device temperature is over 110 ℃. These results verify the higher efficiency and better thermal performance of the proposed hardware as compared to traditional Si solutions.



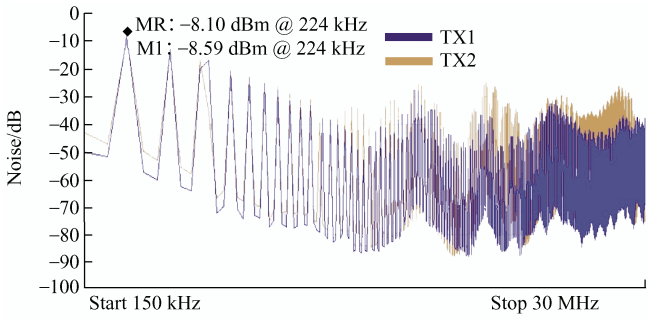
(a) Efficiency with structure 1 transformer



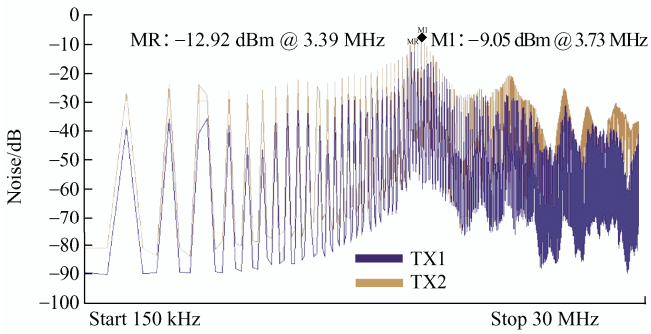
(b) Efficiency with structure 2 transformer

Fig. 10 Efficiency measurements under different loads and different input voltage with two different transformers

Meanwhile, the results also indicate that the low leakage transformer design can achieve 3% higher efficiency as compared with the low-isolation capacitance design, owing to the lower loss at the RCD clamping circuit. The output conductive EMI noise between 150 kHz and 30 MHz was also measured. Fig. 11a presents the DM noise as measured at the output port, and Fig. 11b presents the CM noise. The results indicate that both CM and DM noises will increase when using the structure 2 transformer with the reduced leakage inductance and increased isolation capacitance. However, the peak noise difference is approximately 3 dB for CM noise, and only 0.5 dB for DM noise. Nevertheless, the larger isolation capacitance will increase the broad-spectrum conductive noise. This is especially true for high frequencies, as the propagation path impedance is lower.



(a) DM noise measured at output port



(b) CM noise measured at output port

Fig. 11 DM noise and CM noise as measured at the output ports

The demonstration platform was also tested with different 1.7 kV SiC MOSFETs from different vendors. Fig. 12 presents an efficiency comparison at a 1 000 V input voltage. The results indicate that the efficiency difference is negligible at a 50% load and above, and the performances are all improved over high-voltage Si MOSFET solutions. Under a lighter load, the efficiency has some differences, owing to the design differences in different SiC MOSFETs. However, the actual loss difference is still very small, as the total power is low.

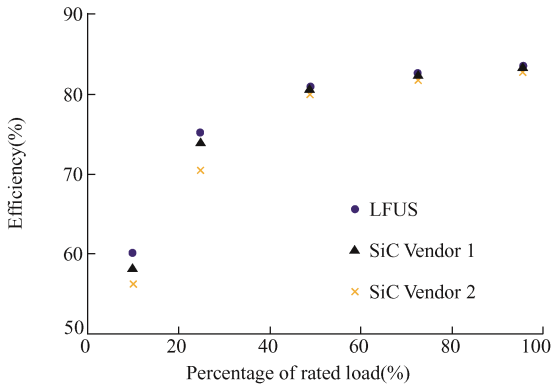


Fig. 12 Efficiency comparison at 1 000 V input voltage with different 1.7 kV SiC MOSFETs

6 Conclusions

This paper presents a design of a single-end flyback Aux-PS with a wide input voltage range using 1.7 kV SiC MOSFETs, for industrial applications. The special design tradeoffs needed for using SIC MOSFETs are discussed in detail, such as gate driving voltage selection and isolation transformer design considerations. The maximum driving voltage of a PWM controller IC is usually lower than the recommended 20 V gate-driving voltage of SiC MOSFETs. Driving an SiC MOSFET with a lower gate resistor will only increase the on-state resistance slightly, and the on-state resistance increase will be less significant at higher temperatures. Moreover, the lower driving voltage can reduce the peak current during device short circuits and improve the system ruggedness under fault conditions. However, the driving voltage cannot be too low, as the device may saturate at a lower current and fail to support a high peak current. The transformer design is a tradeoff between converter loss and EMI emissions. An interleaved winding structure transformer can effectively increase the converter efficiency, but will increase converter EMI noise emissions. A 60 W demonstration hardware was developed and tested in different working conditions. The results verify the higher efficiency and better thermal performance of the proposed system relative to traditional Si solutions.

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