Review of Power Module Automatic Layout Optimization Methods in Electric Vehicle Applications*

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Abstract: The layout of power modules is a crucial design consideration, especially for silicon carbide devices. For electrical layout, optimizing the parasitic parameters can improving switching loss and dynamic behavior. For thermal layout, reducing the thermal resistance and controlling thermal capacitance can reduce the local hot point. Conventional layout design iterations are based on human knowledge and experience. But the major drawback of manual design methods is a limited choice of candidates, large time consumption and also the lack of consistency. With the introduce of automatic layout design, these challenges can be overcome which in the meanwhile alleviates current and temperature imbalance. By reviewing element representation, placement, routing, fitness evaluation, and the optimization algorithm approaches, a state-of-the-art power module layout design method for electric vehicle applications is introduced.

Keywords: Automatic layout design, power modules, optimization method

1 Introduction

In an electric vehicle (EV), the motor drive is a core power conversion component, which requires high speed switching and low on-resistance power devices. The performance requirements and cost constraints promote the development of Si and SiC devices, as well as module packaging layout and design methods [1-2].

Momentous power module layouts for different power ratings have been proposed [3]. Several of these power module layouts exhibit appropriate electrical, thermal, and mechanical performance and are sufficiently compact to fit in the limited space in motor drives. Hence, research focus is not only on inventing new layouts and structures, but also on developing novel layout optimization methods. With the super calculation abilities of computers, layout optimization can be faster, more reasonable, and meet all types of requirements.

From the electrical layout standpoint, parasitic parameters in a power module adversely affect switching loss and dynamic behavior [4]. Smaller parasitics can mitigate voltage overshoot, lower device voltage rating, and reduce device switching losses. In the compact power module for EV applications, high integration reduces space and distance, which may increase coupling between different current paths. To ensure high efficiency and high performance, effort is required to reduce parasitics and maintain balance between paralleled devices [5-6].

From the thermal layout standpoint, the switching frequency enlarges the distribution unbalance of the junction temperature [7]. By reducing the thermal resistance and controlling thermal capacitance, the magnitude of the local hot point can be reduced. Furthermore, the thermal resistance between paralleled devices needs to be balanced as it contributes to both equal current distribution and temperature uniformity, enhancing the performance of the entire module.

Recently, to further reduce parasitic parameters and enhance thermal management, numerous advanced packaging structures have been designed and developed

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for products. Most of these packaging use planar structures, in which the device topside is interconnected directly to copper traces, a copper strip, or flexible conductors. Simultaneously, layout optimization methods for these planar packages have been invented and reported [5].

Over the last two decades, SiC devices have emerged as an attractive alternative to Si devices, possessing various electrical and thermal advantages [8]. For EV applications, 900-1 700 V SiC MOSFET chips and SiC SBD chips have been successfully developed, and they demonstrate high switching frequencies and high-temperature capabilities [9-10].

However, the current rating for a 1 200 V SiC die is usually limited to 100 A at 150 ℃, considering the current manufacturing capability and cost [11]. A regular 1 200 V/600 A hybrid pack drive module requires a minimum of 36 SiC MOSFETs. For enhanced performance, an additional 36 SiC diodes would be added to the module. Careful layout design and optimization are required to balance current sharing and junction temperature [4].

Conventional layout design iterations are based on human knowledge and experience. In most of these designs, the devices, power terminals, copper traces, and wire bonds are set as the basic elements. Elements are purposely placed, following all constraints, using a trial-and-error procedure. In some cases, the routing processes are also implemented via the placement processes. In other cases, routing and placement are two distinct processes, with only dies and terminals placed initially, followed by interconnecting with copper traces or wire bonds. Subsequently, using finite element analysis (FEA) or other calculation methods, the electrical parasitic parameters and thermal performance of the designed candidate is evaluated [12-13]. With similar steps and iterations, after comparing several candidates, the best candidate in the group is selected for further study.

In most of the relevant studies in the literature, manual designs are based on an enumeration algorithm, and the number of design candidates is seldom over 30. There is still no figure of merit that can determine the best layout design with a limited trial number. Therefore, the major drawback of manual design methods is a limited choice of candidates and large time consumption. Furthermore, human-experience-based design lacks consistency [3, 11].

To overcome these challenges, over the past two decades, automatic layout design methods have been proffered and studied. These can be classified as semi-automatic or fully automatic methods. For semi-automatic methods, either the element positions are fixed and the routing is designed by a computer, or each element has a one-dimensional variable and can move only horizontally or vertically. In these designs, layout variations are less flexible, and the layout optimization space cannot be thoroughly searched.

In a fully automatic layout design, all element positions are unfixed, and they do not need to follow any predefined path. In some methods, human experience can be incorporated in the design as a constraint. The design space can be further reduced by following manufacturability rules and cost limits.

Several automatic layout design methods became mature in the last five years and have already achieved crucial cost savings in power module design. They can automatically perform advanced model abstraction, electrical parasitic extraction, and thermal analysis and automatically generate design candidates using geometry-dependent optimization models. Several concepts have been proposed to provide solutions to automatic design challenges, such as symbolic systems, layout languages and virtual grids. With degradations and simplifications, it becomes a problem of minimizing or maximizing the fitness of a complicated arrangement of several objects in constrained and aligned planes [14].

This review introduces the main procedures and concepts in automatic layout design. In section 2, the core optimization aspects are reviewed. Element representation is reviewed in section 3, element placement in section 4, and routing in section 5. Fitness evaluation and optimization algorithms are reviewed in sections 6 and 7, respectively, and future perspectives are discussed in section 8.

2 Core optimization aspects

An optimization problem involves three primary aspects: important design variables, fitness evaluation and constraints. The important design variables (also called decision variables) can be selected by a human or a computer for each design candidate and can be chosen arbitrarily under certain constraints. In the layout design of a power module, the

three-dimensional (3D) physical variables are usually simplified and mapped onto a two-dimensional (2D) model to reduce complexity.

Conversely, constraints are restrictive conditions that must be satisfied to accomplish an acceptable design. The constraints may be geometrical, electrical, thermal, manufacturability related, or cost related. In power module design, e.g., very large scale integration (VLSI) design, the procedures of placement and routing are also required, with special evaluation steps [15]. The requirements for each aspect of optimization are listed in Tab. 1.

Tab. 1 Requirements for optimization aspects

Aspect	Requirement
Component representation	Easy coding and decoding, unique representation, and group of components simplified as one element.
Constraints	Easily implemented in the design
Placement method	Fast and reasonable
Routing method	Fast and reasonable
Evaluation method	Fast evaluation speed with specific levels of accuracy.
Optimization method	Thoroughly search the design space in a short time.

Building a layout design with 3D components while limiting geometric configurations is time consuming. To address these issues, element representation is required to handle 3D geometrical complexity using a regular 2D plane optimization approach. In the element representation step, a special DNA string can be formed and coded under the guidance of representation rules. These DNA strings should be easily usable in the placement, routing, and optimization steps.

All common technology constraints should be determined at the very beginning, e.g., minimum width, minimum spacing, minimum enclosure, and minimum extension. There may be many user-defined reliability constraints, such as terminal position, voltage dependent spacing, and current dependent trace width. These should be easy to implement in the design model.

The placement usually includes a coding and decoding procedure for interpreting the DNA string into a physical layout. Before element placement, layer information, namely layout area, element dimensions, material properties, ambient temperature, and switching frequency, should be used as input to facilitate coding and decoding [15].

However, element placement does not consider the connection possibility for each electrical net. Therefore, an iterative checking process must be passed in the routing step. In some complicated layout cases, more than 85% of the placement solutions are immediately eliminated by routing failures [16]. Both placement and routing steps need to find reasonable solutions in a short time.

A fitness evaluation can be functions or simulations that provide the criterion for further optimization. For power module design, fitness is typically related to electrical performance, thermal performance, weight, cost, volume, efficiency, or a combination of two or more desirable attributes. In the fitness evaluation step, accuracy can be sacrificed slightly in some circumstances to expedite the process.

The optimization method is the algorithm that finds the conditions providing the maximum or minimum value for a special objective [17]. Furthermore, the optimization can be based on a single objective or multiple objectives. The basic requirement for an optimization algorithm is to thoroughly examine the design space in a short time, without sinking into the local optimum early in the process.

3 Element modeling

3.1 Element representation

In the literature, the optimization procedure predominantly involves only the main elements of the power module, and the important design variables regularly employ a simplified encoded mapping (Tab. 2). For EV applications, partial discharge is not considered in most designs.

Tab. 2 The simplification of elements

Item	Simplification method in element representation process
Power switch	Rectangle or point, in placement step
Diode	Rectangle or point, in placement step
Terminal	Rectangle or point, in placement step
Wire bond/metal strap	Line/area, or as part of the power device and transfer area, in placement step and/or in routing step
Direct bonding copper	Line/area, in placement step and/or in routing step
Baseplate	Omitted in the design
Encapsulant	Omitted in the design
Housing	Omitted in the design
Decoupling capacitor	Rectangle or point, in placement step

Because the shapes of devices and terminals are square or rectangular, the positions of devices can be

interpreted via a matrix representing a grid layout region. The positions can then be transformed into single-dimensional vectors and expressed as integers.

A study by Mouawad et al. [10] presents a physical-design-based simplification that retains flexibility and generates relatively detailed routing, as shown in Fig. 1. In the simplification, each component is represented as a single-type rectangle. It can represent all heterogeneous elements, with no limitation to the number of elements. Sherwani [18] and Nakaya et al. [19] employ a similar idea.

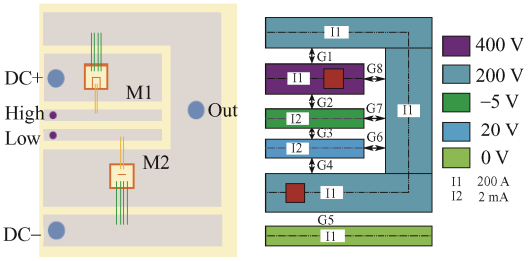


Fig. 1 Physical-design-based simplification

However, the DNA interpretations in these studies become very complicated when the number of dies in the power module is large (n>25). To expedite the placement and routing procedures, several studies use only three types of element: switches, diodes and power terminals [20].

In a wire bond package, wire bonds contribute to the largest impedance. They connect the top pads to the nearest copper traces. Therefore, the shortest and most feasible wire bonds are commonly used. Detailed wire bond connections do not require a special description in the DNA string. Instead, these details are considered in the subsequent evaluation step.

In a study by Ning et al. [3], a combination of die, wire bond, and adjacently connected copper trace region was degraded and treated as one element, as shown in Fig. 2. In this simplification, pads of the device are extended as fringe terminals of the 2D element. This degradation significantly reduces placement and routing times [21].

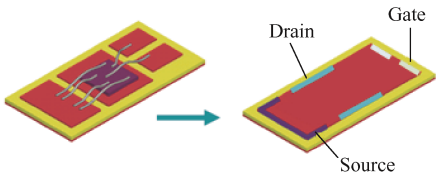


Fig. 2 Combined element

In a study by Hingora et al. [22], typical devices were degraded and depicted for both wire bond package and planar package, as shown in Fig. 3. Subsequently, the positioning procedure speed was increased.

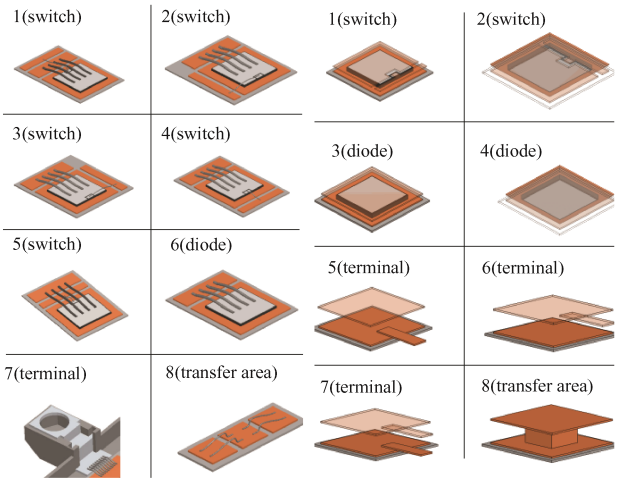


Fig. 3 Typical element representation

Shook et al. [5] provided a symbolic layout model (Fig. 4), which has three basic elements: lines, points and rectangles. Lines represent bond wires and copper traces. Points represent power devices, leads and terminals. Rectangles represent traces that span multiple traces vertically or horizontally, with topological definition. However, this model requires an additional complex coding procedure to generate DNA strings for further optimization.

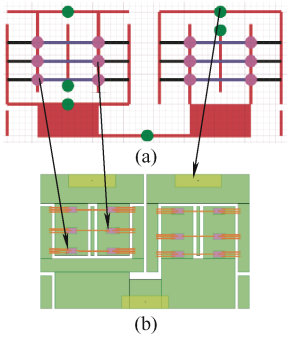


Fig. 4 Symbolic layout model

3.2 Orientation

As shown in Fig. 5, pads on the die may not be in the center but may be on the edge or corner. Asymmetrically distributed pads restrict the direction of an interconnection, which is limited by the wire bond or copper trace fabrication process. In most cases, the orientation of interconnections is critical to parasitic reduction and parameter balancing. Therefore, the orientation

needs to be included to the DNA strings. In the study by Ning et al. [3], the orientation of a die was represented by binary strings (00, 01, 10, 11), as depicted in Fig. 5.

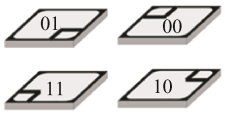


Fig. 5 Orientation definition

To expedite placement and routing, combined element orientations for a wire bond package and a planar package were depicted in a study by Hingora et al. [22], as shown in Fig. 6. In a planar package module, elements can be described using z axis orientation to indicate the upward and downward facing directions.

When considering the product style of a power module in EV applications, the orientation of the power terminal always faces outward from the edge. Thus, the terminal orientations in a 2D layout plane can be reduced from four to one. The transfer area can be formed in the subsequent routing step, if required. With these simplifications, the orientation string of a planar module is reduced to $i+3j+k$, for i power terminals, j switches and k diodes.

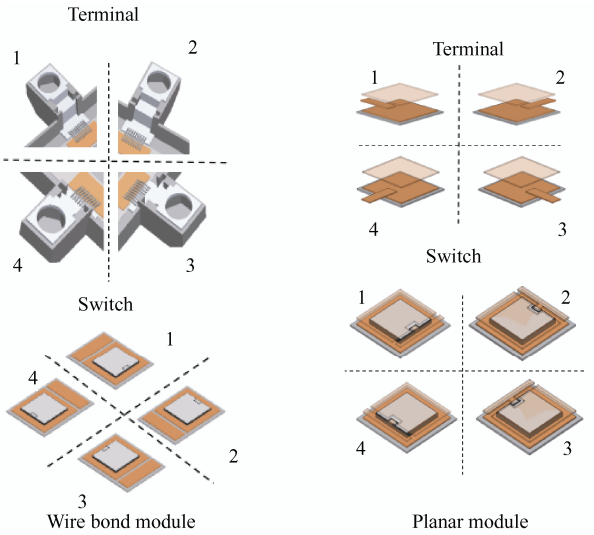


Fig. 6 Combined element orientation

4 Element placement

The element placement step generates an abstract layout representation (symbolic layout). This symbolic layout usually consists of points, lines, or blocks, representing chips, terminals and traces. Typically, the layout coordinates are normalized. Subsequently, each component is stamped into a vector sequence or DNA string, with the representation rules introduced in section 3, which effectively update the trace dimensions and component locations in the optimization process. A placement example is presented in Fig. 7.

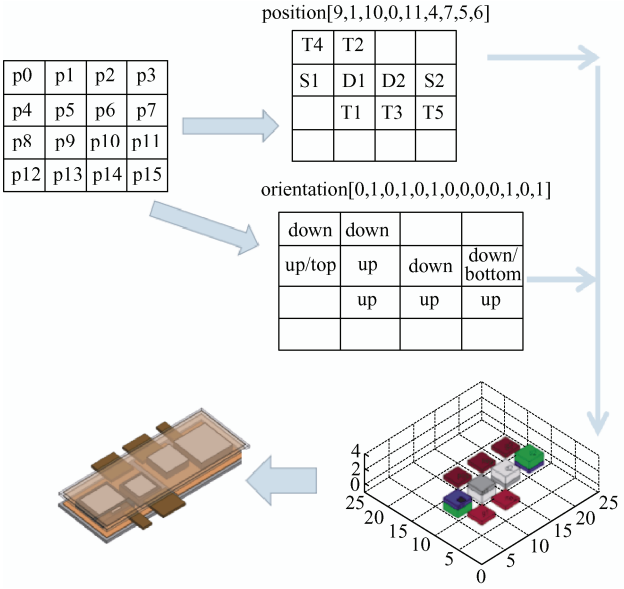


Fig. 7 Example of placement

The placement step in power module layout design is resembles the floor plan step in VLSI layout design. To expedite the design procedure and reduce the datum size, a placement is a data structure capturing relative positions rather than fixed coordinates. A placement can be interpreted as a non-overlapping arrangement in the plane, by deciding the position of each component relative to the position of others [15]. It is thus desirable to develop an efficient, effective, and flexible coding and decoding method to describe the geometric relationship between elements in placement designs.

There are basically two categories in placement: slicing-based and packing-based [19]. The slicing-based floor plan repetitively subdivides rectangles vertically or horizontally into smaller rectangles, thereby representing each rectangle as an element in the power module. The packing-based methods use compacted structures to emulate the packing procedure in a fabric [23]. In a packing-based placement, first, one element is fixed to a corner of a layout region, e.g., the bottom-left corner, and other modules can be shifted further to the top or right. These methods can model only partial topological information. Module dimensions, orientation, and distance need to be added

to the DNA strings to construct an exact placement.

Compared with packing-based methods, the size of each rectangle in the slicing-based methods cannot be controlled easily. In power modules, the numbers and types of elements are much smaller than in VLSI designs. Because the dimension of each type of element is determined at the beginning, slicing-based methods are rarely used in power module layout design [15, 18-19].

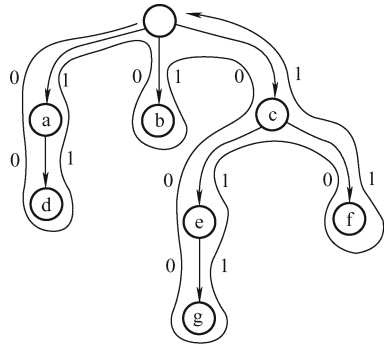
4.1 Relative position

In the layout optimization iterations for power modules, the representations of elements are the most critical key to effectively solving a problem. In a regular data structure for packing-based placement, let $B=[b_1, b_2, \cdots, b_m]$ be a set of m rectangles, with width, height, and orientation denoted by w_i, h_i, and r_i respectively; $1 \leqslant I \leqslant m$. Let (x_i, y_i) denote the coordinates of the bottom-left corner of rectangle b_i; $1 \leqslant i \leqslant m$. A placement representation P is an assignment of (x_i, y_i) for each b_i, such that no two modules overlap.

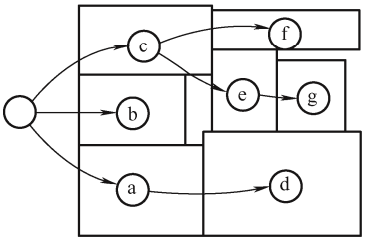
The most commonly used compacted placement representations in power module layouts are O-tree, B-tree, sequence pair (SP), and adjacent constraint graph (ACG) [5]. Other methods, such as corner sequence (CS), bounded slice line grid (BSG), transitive closure graph (TCG), and transitive closure graph with a sequence (TCG-S), have their unique benefits and are awaiting further research [24-25].

An O-tree is a root ordered tree structure, and each node has several branches. An O-tree can be horizontal or vertical, and they use similar definition. In a horizontal O-tree, the root represents the left boundary of the placement. The children are placed adjacent to their parent on the right, with their y coordinate equal to that of the parent. The children are placed adjacent to their siblings at the top, with their x coordinate equal to that of the siblings. In the branching structure, 0 represents a traversal that descends an edge, and 1 means the traverse subsequently ascends that edge in the tree. An example is depicted in Fig. 8, with the branching (00110100011011, adbcegf) presented in Fig. 8a and the decoded placement in Fig. 8b.

B-trees were proposed by Zhu et al. [16] and are based on ordered binary trees and admissible placements. The root in a B-tree corresponds to the elements at the bottom-left corner. The left child is placed adjacent to the parent on the right, with its y coordinate equal to that of the parent. The right child represents the lowest element, which is located above, and its x coordinate is equal to that of the parent. An example is depicted in Fig. 9, with the branching presented in Fig. 9a and the decoded placement in Fig. 9b.

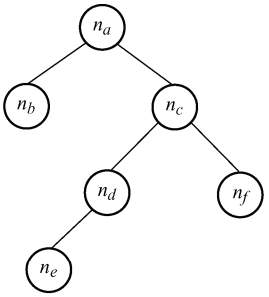


(a) O-tree branching

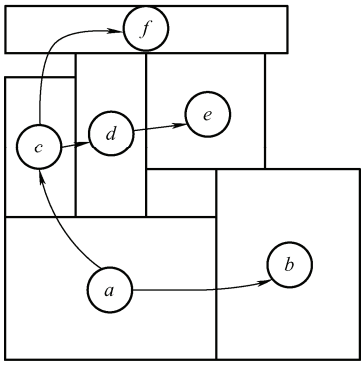


(b) Decoded placement from O-tree

Fig. 8 Example of O-tree



(a) B-tree branching



(b) Decoded placement from B-tree

Fig. 9 Example of a B-tree

Hatta et al. [23] proposed the SP method, which is particularly suitable for stochastic algorithms, e.g., genetic

algorithms (GAs). The SP is a pair of sequences comprising n component names used to indicate the relative positions of n components (Fig. 10). For each pair of components, an SP imposes a horizontal/vertical (H/V) constraint. If two components have the same sequence in the horizontal and vertical sequences, the first component is to the left of the second component. If the horizontal and vertical sequences of the two components are different, the first component of the horizontal sequence is above the second component. An example is depicted in Fig. 10.

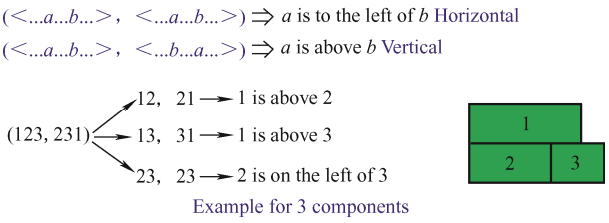


Fig. 10 Example of a sequence pair

For power module layouts, Al et al. [26] expanded the data structure of corner stitching using the ACG. The corner stitching structure has solid and vacant elements, which is obtained by partitioning the layout area into horizontally maximal rectangular tiles. Each tile contains four pointers to preserve neighboring information, with two top-right and two bottom-left corner position pointers [27].

In a constraint graph, the nodes represent elements, the edges of the horizontal graph represent the relation "left of", and the edges of the vertical graph represent the relation "below". The adjacent graph is an undirected graph and has one edge between each pair of adjacent elements. An ACG is a combination of a constraint graph and an adjacent graph, as shown in Fig. 11.

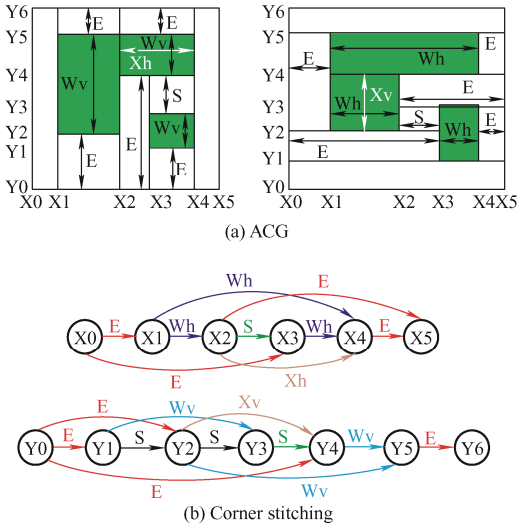


Fig. 11 Example of corner stitching and an ACG

With an ACG, the placement area and element positions can simply be found using longest path computations. Furthermore, it is unnecessary to add extra data in the DNA string for white space.

4.2 White space considerations

Minimizing area is a conventional key objective of power module layout design. However, it is insufficient for the fitness evaluation step. In a power module, the placement must contain some white space (empty room) to mitigate impossible routing issues [28]. If there is plenty of white space within the layout area, a reasonable and high-quality routing solution can be expected.

In most packing-based placement, gaps are added between elements to retain sufficient white space. Wu et al. [2] define the gap as the distance from the bottom-left corner of a component to the left or bottom boundary. To reduce infinite layout candidates, a minimum distance between elements must be set, e.g., 1 mm, 0.5 mm, or 0.1 mm. The gaps between elements are usually represented by decimal strings and binary strings (Fig. 12). In the example in Fig. 12, the horizontal gap is five, and the vertical gap is three, all represented by 3-bit binaries.

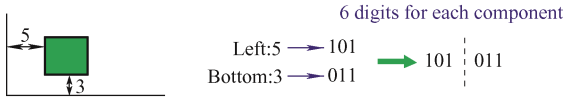


Fig. 12 Gap representation example

5 Routing method

The routing step connects elements using wire bonds, copper traces, and copper straps under certain constraints. Typical constraints include: following the electrical topology connection of the power module, avoiding meandering paths, and minimizing the lengths of critical nets.

Power module routing methods usually operate in a two-phase mode [3]. At the beginning, a coarse routing is performed to match the electrical topology. A punishment is directly assigned to the fitness if a placement data set cannot be routed at all. In the second phase, based on the coarse rouging result and enlargement methods, a detailed routing is performed in which the final interconnection is formed among the elements.

Two routing phases can use the same grain grid

structure. This grain grid can borrow from placement and can be further used in electrical evaluation and thermal evaluation. Interconnection in routing is assumed to have widths that meet the design rules and are adequately separated from adjacent connections and elements.

An example is presented in Fig. 13. After element representation, the routing problem is reduced to a two-dimensional copper wire connection problem. A 1×1 mm grid was used in this example to substitute the routing area. 1 represents a local copper trace and 0 represents the absence of a copper trace. A one-dimensional binary string was used to expedite subsequent crossover and mutation operations in a subsequent GA.

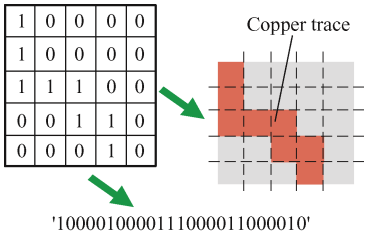


Fig. 13 Routing plane example

5.1 Single net routing

The most widely used routing methods in single net circuits are the mazing and line search methods. They are introduced first for two-terminal routing and then used for coarse routing. Recently, they have been developed for multiple terminal connections and detailed routing.

For automatic wire routing, the mazing algorithm proposed by Lee is one of the earliest routing algorithms. The basic algorithm uses a uniform grid to operate on a single terminal network. In the grid, there are some device cells indicated as blockages.

An example is presented in Fig. 14. First, a wavefront is expanded from one of the elements, and neighboring cells of the element are labeled as 1. Then, at each step, the unlabeled neighbors of the cells labeled L are labeled as L+1. This process continues until the wavefront reaches the target element. Once the target is found, the shortest path is constructed using a backtracking method.

As an enhancement, the wavefront from both elements can be simultaneously expanded until two wavefronts meet, reducing routing time by approximately 30%-45%.

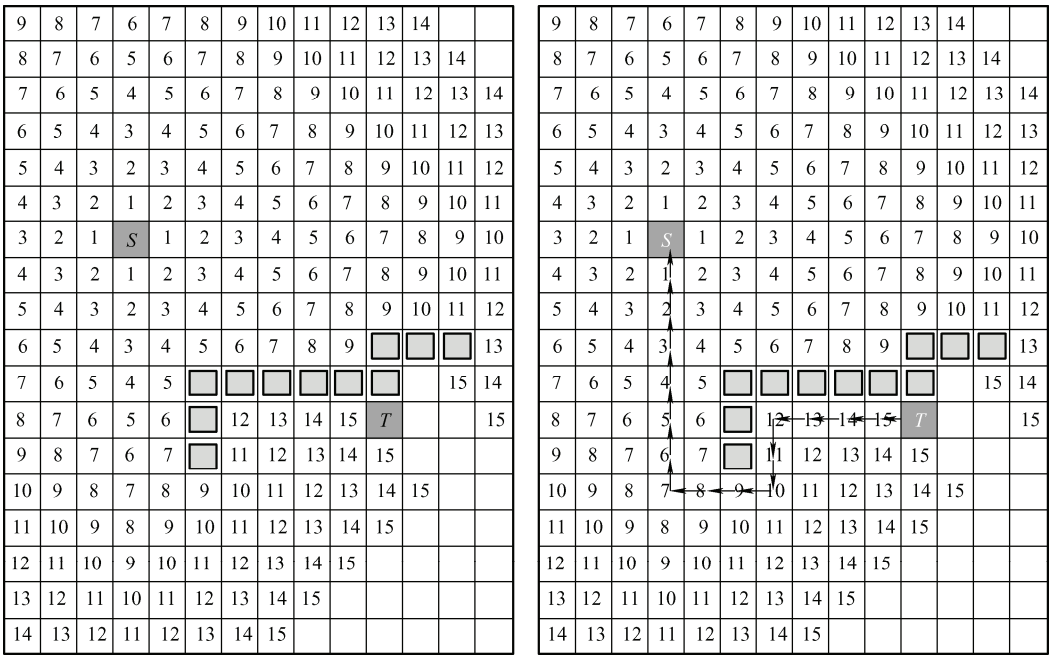


Fig. 14 Mazing routing algorithm example

The first line search algorithms were proposed by Ulutal and Isliev [29]. As shown in Fig. 15, initially, the algorithm expands one horizontal and one vertical line segment for every source and target point. Then the process continues iteratively until one source point line segment intersects with one target point line segment. Once they meet, the path is constructed by backtracking from the intersection point to the source and target points [29].

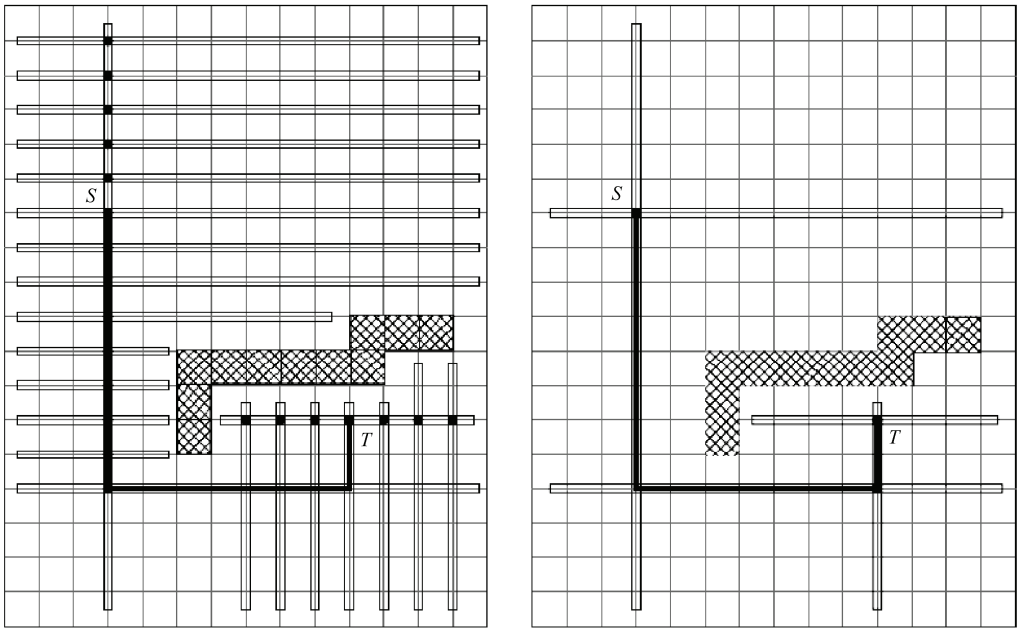


Fig. 15 Line searching routing algorithm example

Multiple terminal routing is an upgraded version of two-terminal routing. A practical approach is to apply the routing algorithm iteratively. Typically, wave expansion starts from a source terminal until a target terminal is reached. Subsequently, the route between these two terminals is regarded as a new source of the wave expansion. When all terminals in the net are routed, this process ends.

After a coarse routing, a detailed routing can be conducted by filling the empty grid. The filling procedure can be a random generation with further checking [30], or growing from coarse routing with certain rules and limits [31]. In a study by Wong et al. [32], nearly 10% of the nets were routed using pure coarse routing, and the rest were executed with detailed routing. However, approximately 73% of the routing time was spent on coarse routing.

5.2 Multiple net routing

Phase-leg modules and multi-phase modules require routing multiple nets concurrently, and the routing solution for one net may potentially impact other nets. The routing methods for multiple nets can be divided into two categories: sequential routing and concurrent routing.

Sequential routing is a straightforward approach, but nets routed in the later iterations may be forced to form relatively low-quality connections. With this approach, selection of the routing order is very sensitive. To solve this problem, the order selection is built into DNA strings in some optimizations.

Concurrent routing can be formulated as a multi-commodity flow problem. A flow network can be modeled based on the layout condition, with each edge in this network having a specific flow capacity and cost. A commodity transports over this network corresponding to each net. The multi-commodity flow problem can be solved as finding a flow for each commodity, while satisfying all flow capacity constraints from the edges in the network.

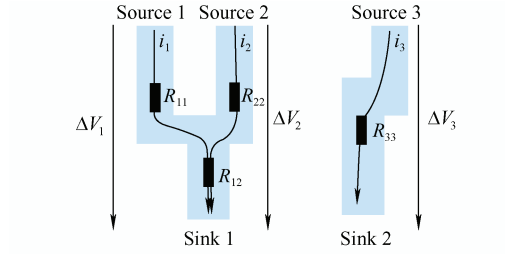
6 Fitness evaluation method

All fitness evaluation methods must provide a high prediction accuracy with an acceptable computational speed. For power modules in EV applications, most evaluations in layout design are focused on electrical and thermal performance. Mechanical evaluations are typically from a package material and module structure standpoint.

6.1 Electrical evaluation

In the early layout design method, design candidates are evaluated using finite element method (FEM) software, such as Ansys. It can achieve high accuracy, but needs to update the geometry for each candidate [33]. Another drawback is the simulation speed; it will take approximately three years for one million candidates in a regular layout optimization [34].

Another commonly used method is the partial element equivalent circuit, which has slightly more simulation error, but can reduce the simulation time considerably. Xia et al. [1] introduced a method for calculating the parasitic resistance matrix based on the voltages and currents. An example is presented in Fig. 16 [28].



$$\begin{bmatrix}\Delta V_1\\ \Delta V_2\\ \Delta V_3\end{bmatrix}=\begin{bmatrix}R_{11}+R_{12}+R_{13} & R_{12} & R_{13}\\ R_{12} & R_{12}+R_{22}+R_{23} & R_{23}\\ R_{13} & R_{23} & R_{12}+R_{13}+R_{33}\end{bmatrix}\begin{bmatrix}i_1\\ i_2\\ i_3\end{bmatrix}$$

Fig. 16 Method for calculating the parasitic resistance matrix

where R_{11}, R_{22} and R_{33} are the self-resistance of each current path, R_{12}, R_{13} and R_{23} are the mutual resistance. In the next step, the magnetic vector potential is calculated based on the current of each element, which is given by

$$\boldsymbol{A}=\frac{\mu_0}{4\pi}\sum_V\frac{J}{r} \tag{1}$$

where $\boldsymbol{A}$ is the magnetic vector potential; J is the current density, i.e., the current value in the element area; μ_0 is the vacuum permeability. The inductance matrix can be calculated as

$$\boldsymbol{L}_{ij}=\sum_{V_i}\boldsymbol{A}\cdot J_j \tag{2}$$

where i and j are current paths. Thus, the primary parasitic resistance and inductance are calculated.

To increase the simulation speed, layouts can be divided into lumped elements. Each element is then approximated by micro-strip transmission line equations. Fig. 17 presents an example of element division in which the network was evaluated by traversing each trace segment.

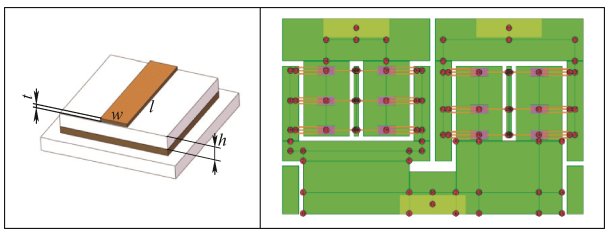


Fig. 17 Micro-strip transmission line approximation

The length of each graph edge is measured and the segment trace width is used as the input of the transmission line equations [5].

In the study by Zhang et al. [35], the evaluation is focused primarily on the commutation path. A straight line connecting the terminals facilitates the commutation path forming a closed loop. In the design, mutual inductance is neglected, considering only self-inductance. The primary optimization objective is to control the commutation loop size, and its inductance is expressed as

$$\lambda=C\cdot\ln(S)-l\cdot\left[\ln(2l)-1\right] \tag{3}$$

where l (mm) is the length of the conductor, C is the perimeter of the loop, and S (mm^2) is the area of the loop.

To further increase the optimization speed, the surrounding areas can be used to represent the inductance of the commutation path. Zhang et al. [35] introduced a planar module case. The 3D commutation area was first divided into n triangles. The inductance is the addition of individual areas. If the corner point of a 3D triangle is $A(x_1, y_1, z_1)$, $B(x_2, y_2, z_2)$ and $C(x_3, y_3, z_3)$, the area of the triangles is then computed as

$$S=\frac{1}{2}\sqrt{\begin{vmatrix}y_2-y_1 & z_2-z_1\\ y_3-y_1 & z_3-z_1\end{vmatrix}^2+\begin{vmatrix}z_2-z_1 & x_2-x_1\\ z_2-z_1 & x_3-x_1\end{vmatrix}^2+\begin{vmatrix}x_2-x_1 & y_2-y_1\\ x_2-x_1 & y_3-y_1\end{vmatrix}^2} \tag{4}$$

6.2 Thermal evaluation

The conventional method for evaluating the thermal performance of a layout candidate is the finite volume method (FVM) using computation fluid dynamics (CFD) software. Resembling FEM in electrical simulations, FVM takes a long time to evaluate candidates. Particularly, when considering convection performance, the Stokes' theorem equation needs to be solved.

In a study by Zhong et al. [8], a modified partial differential equation was introduced to solve thermal equations for a power module with a pin-fin or plate-fin heat sink in less time. Eqs. (5) and (6) present the discretization formulas.

$$C_v\Delta x\Delta y\Delta z\frac{T}{t}-k\frac{T_{i+1,j,k}-2T_{i,j,k}+T_{i-1,j,k}}{\Delta x^2}-k\frac{T_{i,j+1,k}-2T_{i,j,k}+T_{i,j-1,k}}{\Delta x^2}-k\frac{T_{i,j,k+1}-2T_{i,j,k}+T_{i,j,k-1}}{\Delta x^2}=\dot{q}\Delta x\Delta y\Delta z \tag{5}$$

$$C_v\Delta x\Delta y\Delta z\frac{T}{t}-k_{xx}\frac{T_{i+1,j,k}-2T_{i,j,k}+T_{i-1,j,k}}{\Delta x^2}-k_{yy}\frac{T_{i,j+1,k}-2T_{i,j,k}+T_{i,j-1,k}}{\Delta y^2}-$$
$$k_{zz}\frac{T_{i,j,k+1}-2T_{i,j,k}+T_{i,j,k-1}}{\Delta z^2}+C_v u_y\Delta A_y(T_{S2}-T_{S1})=\dot{q}\Delta x\Delta y\Delta z \tag{6}$$

where T is the temperature of the control volume; k is the thermal conductivity of the material; $\dot{q}$ is the volumetric heat generation rate inside the volume; C_v is the volumetric specific heat of the material; (i, j, k) is the location of the node in the thermal grid; k_{xx}, k_{yy}, and k_{zz} are the conductivity of the fluid; u_y is the average velocity of the fluid flowing through the cell in the y direction; ΔA_y is area of the fluid cell in y direction; T_{S2} and T_{S1} are the surface temperatures of the back and front faces, respectively. With further simplification and calculation, a 3D thermal impedance network is obtained, which can be used to evaluate multi-chip modules [36].

To increase the simulation speed, Zhu et al. [37] used stacked thermal block simplification. As shown in Fig. 18, the block emulates a die and is set as the heat source. a and b are the length and width, respectively, of the heat source, c is the length, d is the width of the block, and h is the thickness of the block.

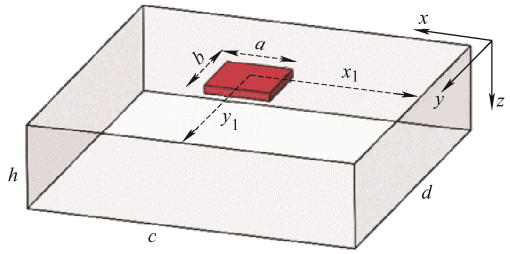


Fig. 18 Stacked thermal block

The calculation equation is presented as Eq. (7)

$$\begin{cases}T(x,y,z)=A_0+B_0z+\sum_{m=1}^{\infty}\cos(\lambda_m x)[A_1\cosh(\lambda_m z)+B_1\sinh(\lambda_m z)]+\\ \sum_{n=1}^{\infty}\cos(\delta_n y)[A_2\cosh(\delta_n z)+B_2\sinh(\delta_n z)]+\\ \sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\cos(\lambda_m x)\cos(\delta_n y)[A_3\cosh(\beta_{mn}z)+B_3\sinh(\beta_{mn}z)]\\ m,n=1,2,3,\cdots\\ \lambda_m=\frac{m\pi}{d}\quad \delta_n=\frac{n\pi}{c}\quad \beta_{mn}=\sqrt{\lambda_m^2+\delta_n^2}\end{cases} \tag{7}$$

where A_j and B_j are coefficients determined by the material and layers. When there are multiple heat sources, the temperature can be calculated as

$$T(x,y,z)=\sum_{i=1}^{n}T_i(x,y,z) \tag{8}$$

To expedite these equations for power modules with numerous dies, a further simplified thermal evaluation method was proposed by Zhu et al. [37] (Fig. 19).

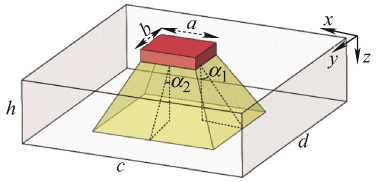


Fig. 19 Cone model for thermal evaluation

$$R_{th}=\frac{1}{h_k}\int_0^h\frac{\mathrm{d}z}{(a+2z\tan\alpha_1)(b+2z\tan\alpha_2)} \tag{9}$$

$$C_{th}=\rho c_v\int_0^h(a+2z\tan\alpha_1)(b+2z\tan\alpha_2)\mathrm{d}z \tag{10}$$

$$\alpha=\begin{cases}5.86\ln(\lambda)+40.4 & \lambda\leqslant 1\\ 46.45-6.048\lambda^{-0.969} & \lambda>1\end{cases} \tag{11}$$

$$\lambda=\frac{h}{a} \tag{12}$$

where R_{th} is the thermal resistance, C_{th} is the thermal capacitance, a and b are the length and width, respectively, of the heat source, d is the width of the block, h_k is the thermal conductivity of the baseplate, α_1 and α_2 are the angles in the lengthwise direction and the widthwise direction, respectively, ρ is the density of the baseplate, c_v is the specific capacitance of the baseplate, and h is the thickness of baseplate.

7 Optimization algorithm

In the layout literature, several optimization methods are proposed. Some of these methods are based on classical methods, such as the sequential unconstrained minimization method, the augmented Lagrangian method, the Newton-Raphson method, and the successive quadratic programming algorithm method.

However, these methods do not appropriately solve complex layout optimization problems. As the complexity of the problem increases (especially when position and connection are not fixed), more complicated optimization techniques are required [38]. Metaheuristic methods emerged and have been developed to solve these issues.

There are two categories of metaheuristic optimization methods: trajectory-based and population-based. The main difference is the number of tentative solutions used in each step of the iteration. A

trajectory-based method majorly consists of hill climbing, tabu search, simulated annealing, and other explorative local search methods. They usually start with an initial solution, and the solution of each step is replaced by the best solution found around it. Trajectory-based methods take a longer time to find the global optimum but are not easily trapped in local optimal solutions. Due to the speed consideration, only a few power module layout optimizations use these methods.

Population-based metaheuristic algorithms (PMA) primarily include evolutionary algorithms, swarm intelligence, and neural networks. They use a set of solutions in each iteration step. The initial population is randomly generated and then enhanced through subsequent iterations. For each step, some members in the population are replaced by newly created individuals. Most of the time, the characteristics of new individuals have a relationship with old ones and have better fitness. Population-based methods show better performance than global optimization and have attracted significant attention in recent years. Tab. 3 outlines the studies that have used these classical methods and metaheuristic algorithms.

Tab. 3 Metaheuristic optimization methods

Method		Option		Literature References
Classical method		—		[39-42]
Metaheuristic algorithm	Trajectory-based	—	—	[37, 43-44]
	Population-based	Evolutionary algorithm	Genetic algorithm	[45-46]
			Immune algorithm	[47]
			Clonal selection	[48]
		Swarm intelligence	Particle swarm	[49-52]
			Ant colony	[53-54]
			Bacterial foraging	[55-56]
		Hybrid algorithm	Social spider optimization	[57-58]

7.1 Genetic algorithm

GAs are based on natural genetics and are a special evolutionary algorithm that utilizes techniques inspired by evolutionary biological mechanisms, such as inheritance, mutation, selection, and crossover. The GA is a stochastic search method that deals with population solutions, and each individual is generally encoded in a problem-independent representation.

As shown in Fig. 20, Ning et al. [3] proposed a two-loops-based GA method. The outer loop is the element placement loop, and the inner loop is the routing loop. The element sequences of the first generation are randomly generated without overlap. Further, the DNA strings evolve to form a new generation [11] through crossover and mutation operations. When the optimization criteria are met, the algorithm terminates.

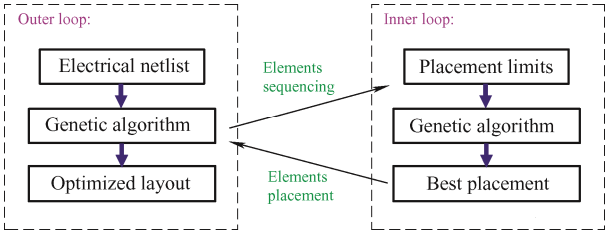


Fig. 20 Two-loop genetic algorithm

Crossover and mutation are the most important operations in the GA process. Conventional crossover and conventional mutation can be used in most cases. If the SP method is used in the element placement, a special operation is required, i.e., a common topology preserving crossover (CTPX). In a CTPX, the longest common subsequences (LCSs) of the parent SP are first determined. Then, elements in the LCSs are preserved in the same sequence, while other elements are exchanged, such that sequences of children are the same as parents. An example is presented in Fig. 21.

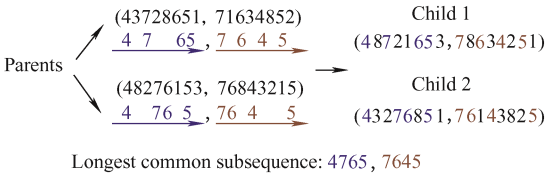


Fig. 21 Example of common topology preserving crossover

In the study by Ning et al. [3], the optimized layout is obtained after 50 outer-loop iterations and a total of 3 982 inner-loop iterations, and the electrical performance is at least 30% better than that of other design candidates in the design procedure. In a study by Shen et al. [59], a 15% thermal performance improvement was obtained after 100 generations of GA optimization.

7.2 Particle swarm optimization

Particle swarm optimization (PSO) is a

population stochastic optimization algorithm first developed by Eberhart and Kennedy [60], which is inspired by the behavior of birds. It has been used to solve numerous optimization problems for electrical engineering, e.g., parameter identification, maximum power point tracking of photovoltaic systems, and parameter optimization of hybrid electric vehicles. Some researchers have begun to use them in layout design [61].

In PSO, all particles follow the optimal particle to fly through the problem space. In each iteration, each particle accelerates toward its own best solution that it has found so far, and simultaneously, it accelerates toward the global best solution found so far by any particle in the group. When a particle discovers a promising new solution, all the other particles move closer to it, exploring the region more thoroughly. Through these steps, the global optimum can be determined, and local optimization traps are avoided.

During each iteration, each particle in the swarm is updated using a velocity update formula and a position update formula. Therefore, almost all the placement and routing methods can fit this algorithm without any special modification. In a study by Maharana and Mohanty [52], a PSO method was compared with a simulated annealing technique for layout area efficiency, area size and layout speed. The PSO shows absolute advantages in five group competitions [52].

7.3 Hybrid algorithm

In a PMA, each individual has to decide whether to explore unknown positions or to exploit and improve tested positions. Pure exploration increases the capacity to find new potential solutions. However, pure exploitation may drive to local optimal solutions because it allows for refining existent solutions. Therefore, the capacity of a PMA to maintain a suitable balance between exploitation and exploration determines its ultimate performance. To meet this requirement, some hybrid algorithms have been introduced and used in electronic design. They possess the operations and benefits of both an evolutionary algorithm and a swarm-based algorithm [62].

Among these hybrid algorithms, the social spider optimization (SSO) algorithm is a typical algorithm. Its members are divided in two categories: males and females. Individuals with different genders are conducted by a set of different evolutionary operators, which mimic the different cooperative behaviors. In the colony, each member does cooperative activities, e.g., maintain the communal web, prey capture, mating, and social contact. Mating is modified from GAs, and similarly, an SSO algorithm has crossover and mutation operations. Based on the division of the entire population into different categories and the selective use of specialized operators, it is possible to improve the balance between exploitation and exploration. The main differences between a genetic algorithm and a spider colony are listed in Tab. 4.

Tab. 4 Comparison of genetic algorithm and spider colony

Features	GAs	SSO
Individual modification	Non	Selectively changing
Individual vanish	In crossover step	Anytime
Population size	Fixed or increase	Fixed/increase/decrease
Mating selection	Stochastically	Emulate the colony selection process
Gender	Unisex	Can be male/female

The SSO algorithm was applied to 19 functions and compared with PSO by Hu et al. [54] and Debnath et al. [45]. SSO delivered better results than PSO for all functions.

8 Future perspectives

The trend of using automatic optimization methods in power module layout design is related to the progress of the metaheuristic algorithm theory, progress in power device development, and EV application requirements. With the developments in optimization theory and computer technology, automatic optimization methods have come to florescence in electrical specializations such as VLSI design, circuit components selection, and control variable determination. They have been proved and have demonstrated fruitful results in power electronics. However, the power module layout design research domain is still relatively young and is a fast-growing area of research.

Multi-objective optimization (MOO) is a pivotal approach to fully exploiting the potential of automatic layout design. A power module layout needs to be

evaluated for electrical performance, thermal performance, weight, and volume. Most studies use cost functions, including electrical and thermal metrics, to generate a Pareto front for further selection. However, some studies experimentally demonstrate that the use of simple fitness aggregation methods with fixed weights does not yield satisfactory results [26]. In the near future, dynamic weight-based fitness aggregation methods will be required for MOO.

Another pivotal approach is the thermo-mechanical reliability analysis, which is a fast evaluation method that has been adopted in automatic design. In the early days of reliability optimization, it was majorly a purely statistical approach, like other component evaluations in the automotive industry [63]. However, it has shifted to a more physical-based approach that involves physical modeling and predicting failures. Cataliotti et al. [64] and Lu et al. [65] provide analytical methods for evaluating simple rectangle direct bonded copper (DBC). In the near future, mechanical formulas will be fully extended and applied in complex module design [64-65].

Another important issue is heterogeneous components such as the capacitor, bus-bar, gate drivers, and EMI filters. Automatic layout design in power modules can be extended to explore a converter system solution space with enhanced searching ability and flexibility. The representation of these heterogeneous components should consider 3D models, flexible rotation, and convex joints. The converter system or power assembly should be optimized with power modules simultaneously, thereby mitigating individual optimization weaknesses such as determining the positions of terminals, plugs, and sockets [66].

9 Conclusions

To better utilize advanced power devices in EV applications, this study reviews the layout methods for power modules. With thorough optimization, packages can have lower parasitic parameters and lower thermal resistance, and both allow a comprehensive exploration of the actual capacity of a power module.

The core layout optimization aspects, element representation, placement, routing, evaluation, and optimization algorithm are introduced and discussed. Some practical considerations for different optimization aspects are also presented. The promising optimization results predict the prevalence of these layout methods and related software in the near future. The proven high performance of layout design will ensure the speedy development of power modules in EV applications.

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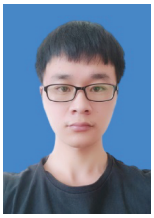

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