Letters

Monitoring of SiC MOSFET Junction Temperature with On-state Voltage at High Currents^{*}

Dan Zheng¹, Yuhui Kang¹, Han Cao^{1, 2}, Xiaoguang Chai^{1, 2}, Tao Fan^{1, 2} and Puqi Ning^{1, 2*}
(1. Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing 100190, China;
2. University of Chinese Academy of Sciences, Beijing 100049, China)

Abstract: A junction temperature monitoring method has been presented based on the on-state voltage at high currents. With a simplified physical model, this method mapped the relationship between junction temperature and on-state voltage. The tough calibration and signal sensing issues are solved. Verified by body-diode voltage detecting method, the presented method shows a good performance and high accuracy, in the meantime, it would not change the modulation strategy and topology of the converter.

Keywords: Junction temperature monitoring, SiC MOSFET, conduction voltage

1 Introduction

In the last two decades, with the demonstration of electrical and thermal advantages, silicon carbide (SiC) devices have exhibited attractive benefits, and were believed to be an alternative for conventional silicon (Si) devices. However, due to limitations such as technology status and production volume, the performance of SiC devices is still far away from their theoretical value, their price is five to eight times of regular Si devices ^[1-2].

To make better use of SiC devices, junction temperature monitoring can assure the normal operation of a power device under the thermal limit. In several applications, the working condition of converters may have unpredictable changes. Junction temperature monitoring will provide additional protection apart from over-current sensing and over-voltage sensing. Furthermore, because SiC dies have lower current rating compared with Si dies, it needs to contain more dies in a power module. The current sharing imbalance will generate several hotspots with higher temperatures. Junction supervise temperature monitoring this can phenomenon, improve the reliability of the power module, increase the capacity of inverter, and further enhance the power density ^[3-5]. The difficulties and drawbacks of junction temperature monitoring methods are presented in Tab. 1.

According to Ref. [9], the junction temperature monitoring method can be classified into four categories, namely conduction contact-based method, electro-thermal model-based method, optical methods, and temperature sensitive electrical parameters (TSEPs)-based methods^[9]. Ref. [17] analyzed the benefits and drawbacks of each category considering various aspects such as accuracy, control strategy invasion, and hardware invasion. Because of the existing flaws in the state-of-the-art SiC wafers, electrons may be trapped after the high current conduction. This issue brings the random change of static parameters and unstable measurement. It baffles engineers to monitor the SiC metal-oxide-semiconductor field-effect transistor (MOSFET) through the same method used by Si insulated gate bipolar transistor (IGBT). A few previously presented junction temperature measurement

Manuscript received July 22, 2020; revised August 12, 2020; accepted August 26, 2020. Date of publication September 30, 2020; date of current version August 29, 2020.

^{*} Corresponding Author, E-mail: npq@mail.iee.ac.cn

^{*} Supported by the National Key Research and Development Program of China (2016YFB0100600) and the Key Program of Bureau of Frontier Sciences and Education, Chinese Academy of Sciences (QYZDBSSW-JSC044).

Digital Object Identifier: 10.23919/CJEE.2020.000014

Category	Method	Difficulties and drawbacks		
Conduction contact-based	Thermistor/ Opto-coupler	Far away from dies, the discrepancy is large.	[6]	
	On chip censor	Interfered with high voltage switching. Although good enough for protection, not good for monitoring.	[0]	
Electro-thermal model-based	3-D thermal network	Difficult to calibrate under working condition, hard to modify when module aged.		
Optical methods	Infrared camera-based	Need to remove the encapsulant and paint the rest black.	[7-9]	
	Optical fiber-based	Need to embed several optical fibers for each die.		
Temperature sensitive electrical parameters (TSEPs)	Threshold voltage-based	With the flaws in wafer, the value randomly changes due to trapped electrons.	[10]	
	Turn-off delay time-based	The resolution is low, difficult to capture.	[11-12]	
	On-state voltage at low current-based	With the flaws in wafer, the value randomly changes due to trapped electrons.	[13-15]	
	Body-diode voltage-based	Can only be applied to SiC MOSFETs without body diodes, cannot be used for on-line monitoring.		
	On-state voltage at high current-based	Calibration without heating up dies. Accurate measurement while blocking high voltage.	[14, 17-19]	

Tab. 1 Difficulties and drawbacks of junction temperature monitoring methods

methods are listed in Tab. 1, and the difficulties and drawbacks have been introduced. Ref. [16] presents a body-diode voltage detection-based method in which a negative voltage is applied to the gate-source terminal of the SiC MOSFET. Since, it can only measure the junction temperature of SiC MOSFET without any additional anti-paralleled diode, this method cannot be used for on-line monitoring ^[16].

From Tab. 1, on-state voltage method is the most feasible method for on-line junction temperature monitoring of SiC. However, there are two issues that have to be resolved before applying this method in a real-world application. The first one is the calibration of the temperature-voltage relationship without heating up the dies at a high current. The second one is the accuracy of the low voltage measurement circuit which can also bear high voltage switching.

This paper presents an accurate and feasible temperature monitoring method, which completely solves the abovementioned issues. A simplified physical model was presented to describe the relationship between temperature and on-state voltage. With the introduction of a reasonable on-state voltage measurement circuit and some practical considerations, the temperature monitoring method was developed and verified by the body-diode based method with a cautious experimental design.

2 Relationship between conduction voltage and junction temperature

The on-resistance in the MOSFET consists of eight parts^[15], namely, the drain contact resistance ($R_{\rm CD}$), substrate resistance ($R_{\rm S}$), drift zone resistance ($R_{\rm D}$), JFET zone resistance ($R_{\rm JFET}$), cumulative resistance ($R_{\rm A}$), channel resistance ($R_{\rm CH}$), N+zone resistance ($R_{\rm N+}$) and the source base resistance ($R_{\rm CS}$), which are depicted in Fig. 1.



Fig. 1 Cross-section of a MOSFET cell

 R_{CH} , R_{JFET} and R_{D} play a key role and account for approximately 90% of the on-resistance of the entire MOSFET, which can be expressed as

$$R_{\rm ON} \approx R_{\rm D} + R_{\rm JFET} + R_{\rm CH} \tag{1}$$

 $R_{\rm D}$ can be calculated as

$$R_{\rm D} = \frac{1}{2Zq\mu_{\rm D}N_{\rm D}}\ln\left(\frac{a+2t}{a}\right) \tag{2}$$

where Z is the cell length, q is the unit charge, μ_D is the

carrier mobility in the drift region, N_D is the doping concentration, *a* and *t* are the relevant parameters of the semiconductor structure depicted in Fig. 1.

 $R_{\rm JFET}$ can be calculated as^[20]

$$R_{\rm JFET} = \frac{x_{\rm JP}}{Zq\,\mu_{\rm n}N_{\rm D}(W_{\rm G} - 2x_{\rm JP} - 2W_{\rm 0})} \tag{3}$$

where μ_n and N_D are the carrier mobility and doping concentration in the JFET region, respectively; x_{JP} , W_G and W_0 are the relevant parameters of the semiconductor structure depicted in Fig. 1.

 $R_{\rm CH}$ can be expressed as^[21]

$$R_{\rm CH} = \frac{L_{\rm CH}}{Z \,\mu_{\rm ni} C_{\rm OX} (V_{\rm G} - V_{\rm TH})} \tag{4}$$

where L_{CH} is the channel length, μ_{ni} is the inversion laminar carrier mobility, C_{OX} is the gate oxide capacitance, V_{G} is the gate drive voltage, V_{TH} is the MOSFET threshold voltage^[22].

In all the abovementioned equations, μ_{ni} , μ_{D} , μ_{n} and V_{TH} are the temperature related parameters.

The inversion laminar carrier mobility can be expressed as

$$\mu_{\rm ni} = 1 \ 140 \left(\frac{T}{300}\right)^{-2.7} \tag{5}$$

where T is the temperature (in Fahrenheit) of the MOSFET.

The MOSFET JFET region is also located in the drift region. To simplify the calculation, μ_D and μ_n can be expressed by μ_a

$$\mu_{\rm a} = \mu_{\rm a0} \left(\frac{T}{300} \right)^{-k} \tag{6}$$

where μ_{a0} can be μ_{D0} or μ_{n0} , which is an equivalent mobility at 300 K; *k* is the coefficient related to the concentration of doping.

MOSFET threshold voltage can be expressed as

$$V_{\rm TH} = \frac{\sqrt{4\varepsilon_{\rm SiC}KTN_{\rm A}\ln(N_{\rm A}/n_{\rm i})}}{C_{\rm OX}} + \frac{2KT}{q}\ln\left(\frac{N_{\rm A}}{n_{\rm i}}\right) (7)$$

where ε_{SiC} is the dielectric constant of the SiC material, *K* is the Boltzmann coefficient, N_A is the doping concentration in the drift region, n_i is the intrinsic carrier concentration.

With simplification, all parameters in the on-resistance of SiC MOSFET can be divided into two categories: temperature-sensitive parameters and structure-related constants which can be expressed as

$$R_{\rm ON} = \frac{A_{\rm I}}{\mu_{\rm ni}(V_{\rm G} - V_{\rm TH})} + \frac{A_{\rm 2}}{\mu_{\rm a}}$$
(8)

$$\mu_{\rm a} = \mu_{\rm a0} \left(\frac{T}{300} \right)^{-A_3} \tag{9}$$

where A_1 , A_2 , and A_3 are structure-related constants. A_1 is the semiconductor parameter related to channel resistance, A_2 is the semiconductor parameter related to the resistance of the JFET and drift regions, A_3 is the semiconductor parameter related to comprehensive mobility. A_1 , A_2 , and A_3 obtained through the experimental data can ascertain the relationship between R_{ON} and junction temperature, and thereafter the I_{D} - T_{J} - V_{DSon} relationship can be characterized.

The temperature-voltage relationship can be approximated by polynomial equations. With cautious calibration and mapping, a thermo-electrical coupling model can be established and used for monitoring.

3 On-state voltage measurement and junction temperature monitoring

3.1 On-state voltage measurement

In a feasible on-state voltage measuring circuit, high accuracy (mV-range), high blocking capability (kV-range) and rapid dynamic responses (us-range) are required simultaneously. Because of the transition between the switch-on and switch-off states, an active control method (as depicted in Fig. 2) was used in this study. To simplify the circuit, the measurement circuit and the driving circuit shared the same power supply. During the on-time of the device under test (DUT), the on-state voltage was measured by injecting the bias current. During the off-time of the DUT, $V_{\rm DS}$ rises to the DC link voltage (hundreds volts), and the diode D_1 can block the DC link voltage and protect the measurement circuit. Diode D_2 was used to compensate the measurement error caused by D_1 . The anti-paralleled diode D_3 functions to eliminate the reverse voltage of D_2 , and thus protects the amplifier. D_1 , D_2 and D_3 are the same type of rapid recovery diode STTH112UFY. An adjustable voltage regulator LM317 was used to generate the bias current for D_1 and D₂. Signal MOSFET BSS138N was adopted to filter invalid measurement data when the DUT is in off-state and to provide a discharge loop for $I_{\text{Bias.}}$ To improve the sampling accuracy, a second-order

low-pass filter circuit was added to filter the high-frequency noise generated during the switching process. Thereafter, a proportional amplifier circuit adjusted the measured signal to fit the isolation transformer and analog to digital converter (ADC). Finally, the analog signal is transmitted to the ADC of the processor through a compact capacitive isolation op amp.



Fig. 2 On-state voltage measurement circuit

The calibration circuit that indicates the temperature-voltage relationship is depicted in Fig. 3. This approach uses a half bridge module and a single pulse generator. The load is a fixed value power resistor, which can quickly set up and cut off the current. The amplitude of the pulse current can be controlled by a single pulse and DC voltage. Similar to other single pulse test circuits, a DC bus capacitor having a large value was required. A heater was used to control the junction temperature of the DUT.



Fig. 5 $I_{\rm J}$ - $V_{\rm DS}$ - $I_{\rm D}$ canonation schematic

Because the switching process of SiC MOSFET is rapid, high current oscillations will be noticed when turned on, which are affected by the parasitic parameters. A necessary delay (a few μ s) is required to mitigate the oscillations. But a long delay will cause die self-heating and affect the calibration result. From a thermodynamic model, the influence of self-heating within 100 μ s could be ignored. Therefore, the sampling time in this study was chosen to be in the range of 10-100 μ s. A house packaged SiC module rated at 1 200 V/300 A was tested, and the hardware is depicted in Fig. 4. The three-dimensional relationship of $I_{\rm D}$ - $T_{\rm J}$ - $V_{\rm DSon}$ was mapped, as depicted in Fig. 5. It is necessary to align the current value and on-state voltage.



Fig. 4 Photograph of the calibration



Fig. 5 Waveform obtained during the calibration

Fig. 6 depicts the temperature-voltage relationship with varying currents. The SiC MOSFET module maintains a good linearity and high resolution at high currents. With a relatively large resolution (approximately 10 mV/°C), it is very suitable for on-line temperature monitoring. In the case of a fixed current, the application of the first-order polynomial fitting can satisfy engineering applications, as shown in Eq. (10)

$$T_{\rm J}\left(V_{\rm DS}, I=I_0\right) = k \cdot V_{\rm DS} + b \tag{10}$$



Fig. 6 Temperature-voltage relationship with varying currents

3.2 Junction temperature monitoring and verification

To demonstrate the junction temperature monitoring ability and accuracy, a comparison and verification test was conducted, as depicted in Fig. 7. The body-diode voltage detecting-based method was used for verification. By comparing the predicted junction temperature, the feasibility of the presented method could be verified. Thus, there are two sets of temperature measurement circuits in Fig. 7. One is the on-state voltage measuring part for the conduction mode of SiC MOSFET (based on Fig. 2), which uses the same power supply as that of the DUT driver. The other circuit is the body-diode voltage measuring part with a low current injection when SiC MOSFET is shut down using a negative gate voltage. Because the body-diode requires the injection of a low reverse current, this part of the circuit requires another isolated power supply. $I_{\rm H}$ is the high current source. When S2 cuts off the high current flowing through the DUT, it is necessary to turn on S1 in advance to provide a freewheeling loop for $I_{\rm H}$. $I_{\rm Bias}$ is the bias current injected into the MOSFET, $I_{\rm L}$ is the low current injected into the body diode, these two currents are controlled by MOSFET S4 and S5.



Fig. 7 Test circuit and control sequence

At the beginning, the auxiliary switch S2 was turned on, the DUT S3 was turned on, and the adjustable current source feds a fixed large current. DUT S3 heats itself and was water cooled to prevent it from reaching excessive temperature levels. During this step, the on-state voltage was recorded to predict the junction temperature. Thereafter, the freewheeling loop was turned on at time point 1, and S1 was turned off at time point 2 to cut off the high current. After the high conduction current is cut off, the gate signal of SiC MOFSET was closed by a negative voltage at time point 3. Finally, a low current I_L was injected into the body-diode. After time point 4, the body-diode voltage was recorded to detect the junction temperature. Fig. 8 depicts test waveform with physical quantities and scales marked in it. Because the DUT was shut down in a short time (100 μ s in Fig. 8), the junction temperature changes slightly. Thus, the junction temperature measured by the two methods are comparable.



to low current

The body-diode voltage of DUT was then calibrated as depicted in Fig. 9. $I_{\rm L}$ is a low constant current source, which is injected to the body-diode of the DUT, and its power loss can be ignored. During the calibration step, the junction temperature of the DUT was controlled using a heater, and the DUT was to be triggered off by a negative gate voltage. The calibrated temperature-voltage approximation line at different constant currents is depicted in Fig. 10. The curve also maintains a good linearity. However, the resolution is relatively small (approximately $-2 \mu V/^{\circ}C$).



Fig. 9 $T_{\rm J}$ - $V_{\rm F}$ calibration schematic

The comparison of measurement results is listed in Tab. 2. When the current level is high (greater than or equal to 50% $I_{D, \text{ continuous}}$), both the methods agree well with each other, and the error is less than 6%. Thus, the presented on-state voltage at a high current indicates the potential of this approach and can be used in the monitoring of junction temperature.



Tab. 2 Comparison of temperature monitoring

	V _{DS(HC)} /V	Relationship at high current T _J =kV _{DS} +b		$T_{\rm J(HC)}/$ °C	$T_{J(LC \text{ in diode})} / ^{\circ}C$
$I_{\rm D}/{\rm A}$					
		k	b		
100	0.49 375	288.90	-87.89	54.75	49.90
200	1.08 125	145.90	-92.40	65.35	68.30
250	1.63 750	115.20	-91.19	97.45	102.40
300	2.46 250	93.83	-88.96	142.09	150.96

4 Conclusions

This study established a temperature-voltage model, and presented anti-interference, reliable and stable signal acquisition circuits for on-state voltage-based junction temperature monitoring method. By determining a reasonable sampling time, the trading-off between self-heating and accuracy was mitigated during the calibration stage. Verified by the on-state voltage via body-diode, the capability of temperature monitoring was demonstrated. This resulted in the considerable achievement of enhancing the power density and reliability of converter systems.

References

- [1] B Mouawad, A Hussein, A Castellazzi. A 3.3 kV SiC MOSFET half-bridge power module. 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, 2018: 463-466.
- [2] J D Vanwyk, F C Lee, Z Liang, et al. Integrating active, passive and emi-filter functions in power electronics systems: A case study of some technologies. *IEEE Transactions on Power Electronics*, 2005, 20(3): 523-36.

- [3] B Lu, W Dong, Q Zhao, et al. Performance evaluation of CoolMOS[™] and SiC diode for single-phase power factor correction applications. *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition*, 2003. Miami Beach, FL, USA, APEC'03, 2003(2): 651-657.
- [4] Q Chen, Y Xu, J Liu, et al. Practical design considerations for IPEM-based PFC converter employing CoolMOS and SiC diode. *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition*, 2006, Dallas, TX, APEC' 06, 2006: 1-6.
- [5] B W Shook, A Nizam, Z Gong, et al. Multi-objective layout optimization for multi-chip power modules considering electrical parasitics and thermal performance. 2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL), 2013, Salt Lake City, UT, COMPEL2013, 2013: 1-4.
- [6] P Q Ning, T Yuan, Y Kang, et al. Review of Si IGBT and SiC MOSFET based on hybrid switch. *Chinese Journal of Electrical Engineering*, 2019, 5(3): 20-29.
- [7] K Li, G Y Tian, L Cheng, et al. State detection of bond wires in IGBT modules using eddy current pulsed thermography. *IEEE Transactions on Power Electronics*, 2014, 29(9): 5000-5009.
- [8] X Perpina, X Jorda, M Vellvehi, et al. Long-term reliability of railway power inverters cooled by heat-pipe-based systems. *IEEE Transactions on Industrial Electronics*, 2011, 58(7): 2662-2672.
- [9] Y Avenas, L Dupont, Z Khatir. Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters: A review. *IEEE Transactions on Power Electronics*, 2012, 27(6): 3081-3092.
- [10] S Yang, A Bryant, P Mawby, et al. An industry-based survey of reliability in power electronic converters. *IEEE Transactions on Industry Applications*, 2011, 47(3): 1441-1451.
- [11] H Luo, Y Chen, P Sun, et al. Junction temperature extraction approach with turn-off delay time for high-voltage high-power IGBT modules. *IEEE Transactions on Power Electronics*, 2015: 5122-5132.
- [12] Z Zhang, F Wang, D J Costinett, et al. Online junction temperature monitoring using turn-off delay time for silicon carbide power devices. 2016 IEEE Energy Conversion Congress and Exposition (ECCE), 2016, Milwaukee, WI, ECCE2016, 2016: 1-7.

- [13] M H M Sathik, J Pou, S Prasanth, et al. Comparison of IGBT junction temperature measurement and estimation methods: A review. 2017 Asian Conference on Energy, Power and Transportation Electrification (ACEPT), 2017, Singapore, ACEPT2017, 2017: 1-8.
- [14] A Griffo, J Wang, K Colombage, et al. Real-time measurement of temperature sensitive electrical parameters in SiC power MOSFETs. *IEEE Transactions on Industrial Electronics*, 2018, 65(3): 2663-2671.
- [15] H Mhiesan, J Umuhoza, K Mordi, et al. Evaluation of 1.2 kV SiC MOSFETs in multilevel cascaded H-bridge three-phase inverter for medium-voltage grid applications. *Chinese Journal of Electrical Engineering*, 2019, 5(2): 1-13.
- [16] C Herold, J Sun, P Seidel, et al. Power cycling methods for SiC MOSFETs. 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD), 2017, Sapporo, 2017: 367-370.
- [17] N Baker, M Liserre, L Dupont, et al. Improved reliability of power modules: A review of online junction temperature measurement methods. *IEEE Industrial Electronics Magazine*, 2014, 8(3): 17-27.
- [18] J Wu, L Zhou, X Du, et al. Junction temperature prediction of IGBT power module based on BP neural network. *Journal of Electrical Engineering and Technology*, 2014, 9(3): 970-977.
- [19] N Baker, S Munk-Nielsen, F Iannuzzo, et al. Online junction temperature measurement using peak gate current. 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), 2015, Charlotte, NC, APEC2015, 2015: 1270-1275.
- [20] J L Hudgins, G S Simin, E Santi, et al. An experimental study on estimating dynamic junction temperature of SiC MOSFET. *IEEE Transactions on Power Electronics*, 2003, 18(3): 907-914.
- [21] S Fukunaga, T Funaki, S Harada, et al. An experimental study on dynamic junction temperature estimation of SiC MOSFET with built-in SBD. *IEICE Electronics Express*, 2019, 16(17): 1-3.
- [22] D Schweitzer, H Pape, L Chen, et al. Transient dual interface measurement: A new JEDEC standard for the measurement of the junction-to-case thermal resistance. *Annual IEEE Semiconductor Thermal Measurement & Management Symposium*, 2011, 9(1): 222-229.