Simplified Analytical Model for Estimation of Switching Loss of Cascode GaN HEMTs in Totem-pole PFC Converters*

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Abstract: A practical analytical model to calculate the switching loss of cascode gallium nitride high electron mobility transistors (GaN HEMTs) is proposed. To facilitate analysis and application, the transmission delays introduced by Si MOSFET and interconnection inductances are ignored in modeling. Meanwhile, the nonlinear junction capacitances of the device and circuit stray inductances are also incorporated to increase the accuracy of the model. The turn-on and turn-off switching processes are described in detail and the simplified equations can be easily solved by using mathematical tools. Based on the analytical model, loss evaluation of totem-pole PFC converter is introduced briefly. Finally, the accuracy of the model is validated by comparing the calculated loss and converter's efficiency with experiment results. Peak efficiency of 99.26% is achieved for a 3.6 kW single phase CCM Totem-Pole PFC AC/DC converter switching at 50 kHz based on 650 V cascode GaN HEMTs.

Keywords: Analytical model, cascode GaN HEMTs, totem-pole PFC, efficiency evaluation

1 Introduction

Wide bandgap power semiconductor devices, especially GaN HEMTs, are showing superior material properties. Compared with traditional silicon-based devices, the higher electric breakdown field, higher electron mobility, and larger energy gap of GaN enable them to be applied in higher switching frequency, with less switching loss, and lower on-resistance. In recent years, a large number of GaN devices have been manufactured and used in a variety of applications. The employment of GaN devices will significantly expedite the improvements in power converters performances [1-5].

To estimate the converter total power loss and improve the conversion efficiency under hard-switching conditions, several circuit simulation models have been proposed in Refs. [6-7]. Unfortunately, building these simulation models is quite time-consuming, and the simulation results are not always directly applicable to converter design. Compared with simulation models, analytical modeling is a useful approach to achieving a design with optimal performance. Analytical switching loss models use several mathematical equations to describe each mode during turn-on and turn-off. Piecewise linear method and equivalent circuit are often used to simplify the calculation process.

The most popular analytical switching loss models are the piecewise linear model presented in Refs. [8-9]. Typically, the model can roughly describe the switching process and estimates the switching loss due to its simplicity and good performance, so it is referred to as the conventional model. However, the main drawback is that it neglects the parasitic inductances and the nonlinearity of the junction capacitances, for which the estimation of switching loss is nearly in the same magnitude as the experimental result. More comprehensive analytical switching loss models that include such parasitical parameters are presented in Refs. [10-12]. The nonlinear junction capacitances and the parasitic inductance are taken into consideration, especially the common source inductance is included. These analytical switching loss models are applied to the high-frequency low-voltage buck converter and the results match the experiment results very well.

However, all of these analytical switching loss models are devised to estimate the power loss of Si MOSFET. Limited by manufacturing technique, most

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of the GaN devices available today are lateral heterojunction field-effect transistors (HFETs) on a commercial level, also known as HEMTs. A layer of high-mobility electrons called "two-dimensional electron gas" (2DEG) that benefits from the unique structure forms a native channel between the source and drain of the device. Because of the native 2DEG channel, the fundamental GaN HEMTs are inherently depletion-mode devices. Several methods have been used to fabricate enhancement-mode GaN HEMTs [13-15], and analytical circuit models of E-mode devices that combine the circuit parameters are developed [16-18].

A normally-off GaN device can also be fabricated by cascode structure, requiring packaging of the high-voltage depletion-mode GaN HEMT with a low-voltage enhancement-mode Si MOSFET [19-21]. To understand the static and dynamic behavior of cascode GaN HEMTs static and dynamic behavior, an analytical loss model of high voltage GaN HEMT in cascode configuration has been proposed in Ref. [22]. The novel analytical model considers the package and PCB parasitic inductances, as well as the nonlinearity of the junction capacitors and the transconductance of the cascode GaN HEMTs. Even the package bonding and terminal lead parasitic inductors are all taken into considerations, which is shown in Fig. 1. The model is easy to understand and provides a deep insight into the switching process. But the model is too complicated as it needs a special proprietary tool for parameter extraction in the package, which is very difficult to perform for many researchers and engineers.

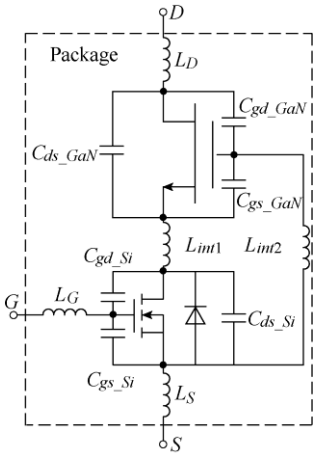

Fig. 1 Structure of cascode GaN transistor considering package parasitic parameters

In this paper, a simplified analytical loss model is used to calculate the switching losses of the cascode GaN HEMTs. In order to guarantee the superior precision of the cascode GaN HEMTs, all parasitic inductors and capacitors are taken into account except for the parameters in the package. It should be noted that the model requires only data available in the datasheet provided by manufacturers. The basis of the model is given in Section 2. The transition process is analyzed in Section 3. Section 4 presents the simulation and experimental validation of the model. Eventually, Section 5 is devoted to drawing conclusions.

2 Basis of the model

A totem-pole PFC converter based on cascade GaN HEMTs is illustrated in Fig. 2. Two kinds of stray inductances are taken into account in a totem-pole PFC converter, including the device terminal lead and printed circuit board (PCB) traces parasitic inductances. It is reasonable to neglect the package interconnection inductances, because the bonding inductances are small enough based on the current packaging technology and it is hard to extract for the vast majority of designers. Fig. 3 shows the equivalent circuit of the totem-pole PFC converter for cascode GaN HEMTs with consideration of the parasitic inductances and capacitances. L_D, L_G, and L_S represent the sum of the terminal lead and PCB traces loop parasitic inductances. Particularly the L_S is called the common source inductance, which is inductance that is common to the power and driver loop. These parameters can be easily obtained through measurement or simulation results.

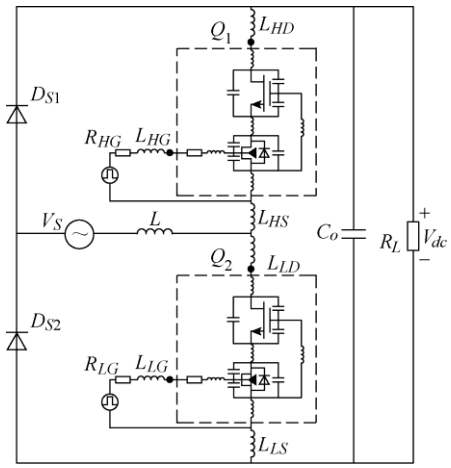

Fig. 2 Schematic diagram of cascode GaN-based totem-pole PFC converter

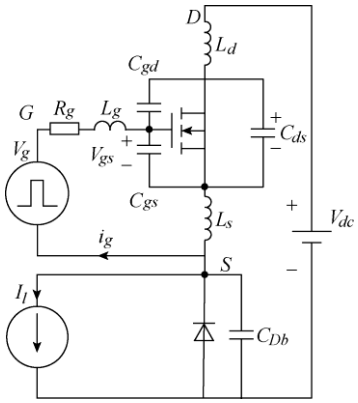

Fig. 3 Simplified equivalent circuit of totem-pole PFC converter to analyze cascode GaN HEMTs

All the features of the cascode GaN HEMTs, such as the curves of transconductance and junction capacitances, can be found in device datasheets provided by manufacturers. Piecewise linear functions are used to fit these curves to realize quick parameter extraction for off-the-shelf components. For example, the equivalent transconductance

$$g_m(V_{gs})=\begin{cases} a_1 & (V_{gs}<V_{th1}) \\ a_2 & (V_{th1}\leqslant V_{gs}<V_{th2}) \\ a_3 & (V_{th2}\leqslant V_{gs}) \end{cases} \tag{1}$$

can be obtained from the drain-source current IDS versus the gate-source voltage V_{gs} curve as shown in Fig. 4a. Coefficients a_1, a_2 and a_3 can be extracted directly from the slope of the piecewise linear fitting curve. The behavior of cascode GaN HEMTs as a current source controlled by the gate voltage is described by

$$I_{channel}=g_m(V_{gs}-V_{th}) \tag{2}$$

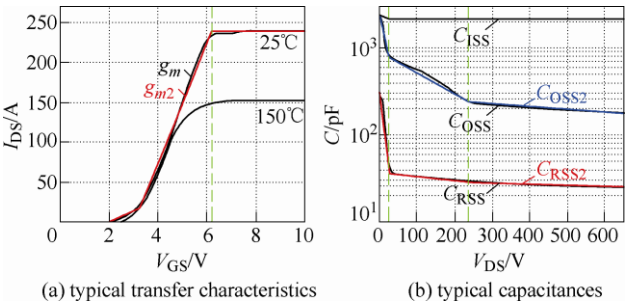

Fig. 4 Data available in device datasheets and curve fitting

The expressions of the junction capacitance can be also obtained by the same method as above, including C_{ISS}, C_{RSS} and C_{OSS} data available in device datasheets in Fig. 4b. The capacitance is given by

$$C(V_{ds})=\begin{cases} b_1V_{ds}-V_1 & (V_{ds}<V_{ds1}) \\ b_2V_{ds}-V_2 & (V_{ds1}\leqslant V_{ds}<V_{ds2}) \\ b_3V_{ds}-V_3 & (V_{ds2}\leqslant V_{ds}) \end{cases} \tag{3}$$

where coefficients b_1, b_2, b_3 and V_1, V_2, V_3 can be respectively obtained from the slope and the intercept of the piecewise linear fitting curve.

According to the test method of the device, C_{gs}, C_{gd} and C_{ds} can be given by

$$\begin{cases} C_{gs}=C_{ISS}-C_{RSS} \\ C_{ds}=C_{OSS}-C_{RSS} \\ C_{gd}=C_{RSS} \end{cases} \tag{4}$$

It is noteworthy that nonlinear parameter models complicate mathematic calculation. So the transistor parameters are calculated off-line and look-up table method is used to reduce the computation complexity.

3 Analysis of hard-switching transients

The modeling approach of cascode GaN HEMTs is based on the silicon-based MOSFETs analytical loss models proposed in Refs. [7-9]. Moreover both the transconductance and the nonlinearity of junction capacitance are considered, and the bottom switch reverse recovery process is analyzed in detail. The turn-on transient process could be divided into four stages as follow: 1) delay period, 2) drain-source current rising and bottom switch reverse recovery, 3) drain-source voltage falling, 4) ringing stages. And the turn-off transient process could be divided into three stages: 1) delay period, 2) drain-source current decreasing and voltage rising, 3) remaining charging, a detailed analysis of this circuit describes in the following sections as follow.

3.1 Turn-on transition

The Equivalent circuits for hard-switching turn-on transition are shown in Fig. 5. Before the cascode GaN HEMTs turn on, the dc-link voltage V_{dc} is applied to the cascode GaN HEMTs, and the inductor current I_l flows through freewheeling diode D_b. The initial conditions of cascode GaN HEMTs for the electrical variable before turn-on transition are

$$\begin{cases} V_g=0 \\ V_{ds}=V_{dc} \\ I_l=I_L \end{cases} \tag{5}$$

(1) Stage I: Delay period.

After the gate voltage V_g is applied, the gate current charges the transistor input capacitors C_{gs} and C_{gd}. The transistor drain current is zero and the drain-source voltage is equal to the dc-link voltage. From the circuit in Fig. 5 Stage I, the following equations are obtained

$$V_g = V_{gs} + R_g i_g + \left(L_g + L_s\right)\frac{\mathrm{d}i_g}{\mathrm{d}t} \tag{6}$$

$$i_g = \left(C_{gs} + C_{gd}\right)\frac{\mathrm{d}V_{gs}}{\mathrm{d}t} \tag{7}$$

$$V_{gs} = V_{gd} + V_{ds} \tag{8}$$

The current i_g can be obtained from equations (6)-(8), and this current is used to calculate the initial current for the following stage. As the channel is not activated, there is no power loss during this period except the loss of the gate driver. The delay period is the time required for V_{gs} to reach V_{th} from 0 V.

(2) Stage II: Drain-source current rising.

The transistor channel starts conducting and will be directly controlled by the gate voltage V_{gs}. The junction capacitors C_{gd} and C_{ds} are discharged slowly by channel current. It should be note that the drain-source voltage V_{ds} decreases in this stage because of the voltage drop across L_s and L_d induced by channel current rising as shown in the following equation

$$V_g = V_{gs} + R_g i_g + \left(L_g + L_s\right)\frac{\mathrm{d}i_g}{\mathrm{d}t} + L_s\frac{\mathrm{d}i_{Ld}}{\mathrm{d}t} \tag{9}$$

$$V_{dc} = V_{ds} + \left(L_s + L_d\right)\frac{\mathrm{d}i_{Ld}}{\mathrm{d}t} \tag{10}$$

$$i_{Ld} = i_{ch} + C_{ds}\frac{\mathrm{d}V_{ds}}{\mathrm{d}t} + C_{gd}\frac{\mathrm{d}V_{ds}}{\mathrm{d}t} \tag{11}$$

$$i_{ch} = g_m\left(V_{gs} - V_{th}\right) \tag{12}$$

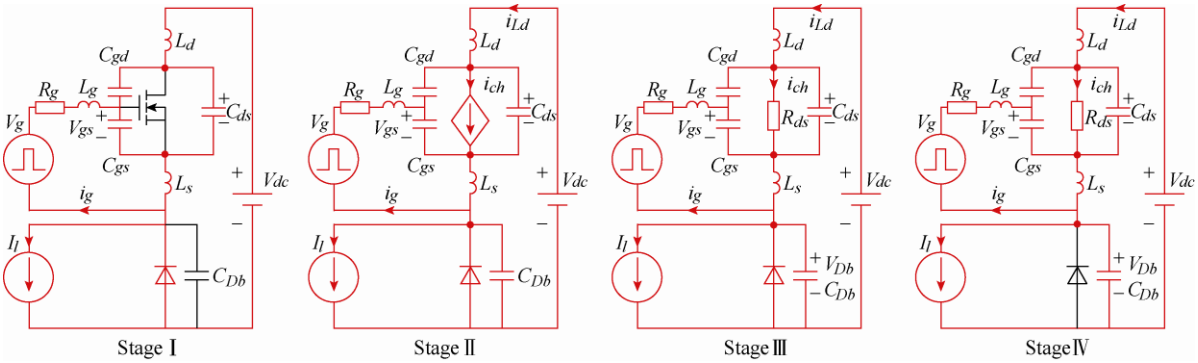

Fig. 5 Equivalent circuits for hard-switching turn-on transition corresponding to the totem-pole PFC converter

The drain-source current consists of two parts: the channel current and the junctions capacitors discharge current. When i_{Ld} reaches the inductor current I_l, this period ends and the bottom switch reverse recovery period begins.

(3) Stage III: Reverse recovery current spike and drain-source voltage falling.

Since the bottom cascode structure switch contains a low-voltage Si MOSFET, the reverse recovery losses are inevitable. In this period, the bottom switch is unable to go from freewheeling mode to reverse blocking state rapidly until a large amount of charge has been removed. The top cascode GaN HEMTs current i_{Ld} rises to the maximum with the charge of reverse recovery current, so the top switch current spikes goes high with the same magnitude of the bottom switch.

There're some assumptions before analyses of the bottom switch reverse recovery loss: 1) the total reverse recovery current I_{rrm} is positively correlated with the initial current I_l which flows through the bottom switch; 2) the reverse recovery current rising slope magnitude $\Delta i_{Ld} / \Delta t$ is equal to the initial rise rate of the top switch. Consequently, the simplified reverse recovery process is shown in Fig. 6 and the I_{rrm} could be expressed by

$$I_{rrm} = \frac{I_{rrm0}}{I_{s0}} I_l \tag{13}$$

where I_{rrm} is the present reverse recovery current, I_{rrm0} and I_{s0} are the test results of reverse recovery current provided by the device datasheets. The cascode GaN HEMTs current i_{Ld}, during t_s period, could be expressed by

$$i_{Ld}(t) = I_l + \frac{\Delta i_{Ld}}{\Delta t} t \tag{14}$$

before the i_{Ld} reaches the maximum in this subperiod, where the following equation is satisfied

$$i_{ch}R_{ds}+L_s\frac{\mathrm{d}i_g}{\mathrm{d}t}+\left(L_d+L_s\right)\frac{\mathrm{d}i_{Ld}}{\mathrm{d}t}=V_{dc} \tag{15}$$

When the reverse blocking ends, a part of the current i_{Ld} provides the inductor current I_l, and the others charge the junctions capacitors of the bottom switch. This subperiod ends until the current that flows through the top switch decreases to I_l. The equivalent circuit is shown in Fig. 5 Stage III, and key equations are given by

$$i_{Ld}=i_g+I_l+C_{Db}\frac{\mathrm{d}V_{Db}}{\mathrm{d}t} \tag{16}$$

$$V_{dc}=i_{ch}R_{ds}+L_s\frac{\mathrm{d}i_g}{\mathrm{d}t}+\left(L_d+L_s\right)\frac{\mathrm{d}i_{Ld}}{\mathrm{d}t}+V_{Db} \tag{17}$$

(4) Stage IV: Ringing period.

The ending sign of Stage III is that $i_{Ld} = I_l$, with no restrictions on the value of V_{ds}. In other words, there are two cases for V_{ds} at the end of Stage III in fact. The first case is that the top switch drain-source voltage decreases to 0 V before the i_{Ld} decreases to I_l. The other case is that the top switch drain-source voltage does not decrease to 0 V before the i_{Ld} decreases to I_l. The equations in this stage are as same as the second subperiod of Stage III. During this stage, the top switch is fully turned on until the following conditions are satisfied

$$\begin{cases} i_{Ld}=I_l \\ V_{ds}=I_lR_{ds} \\ V_{gs}=V_g \end{cases} \tag{18}$$

The losses of the turn-on transition are concentrated in the last three stages, and can be calculated as

$$P_{loss\_on}\left(t\right)=\int_{t_{\mathrm{II}}}^{t_{\mathrm{IV}}}V_{ds}\left(t\right)\cdot i_{ch}\left(t\right)\mathrm{d}t \tag{19}$$

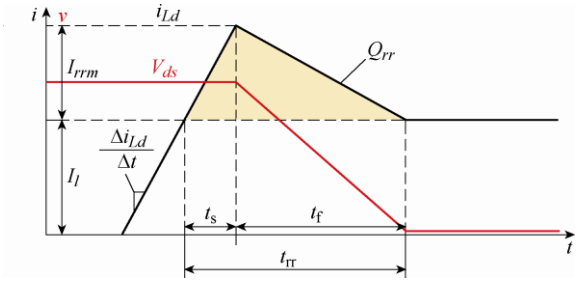

Fig. 6 Simplified recovery waveform in Stage III

3.2 Turn-off transition

The turns-off behavior is similar to the turn-on transition as shown in Fig. 7 but no reverse recovery losses in Stage III. Before the cascode GaN HEMTs turn off, the gate voltage is equal to V_g, and the inductor current I_l flows through cascode GaN HEMTs. There are three stages during turn-off transition in total, and a brief analysis as follows.

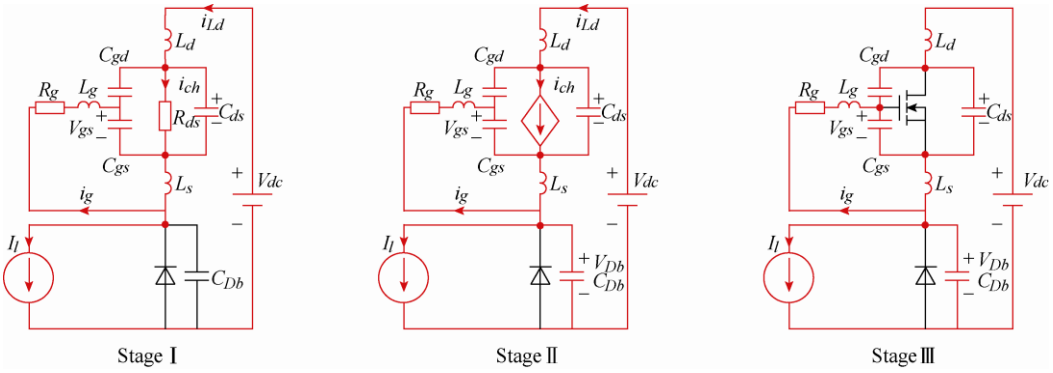

Fig. 7 Equivalent circuits for hard-switching turn-off transition corresponding to the totem-pole PFC converter

(1) Stage I: Delay period.

After the gate pulse voltage transition from V_g to 0 V, the junction capacitor C_{gs} and C_{gd} begin to discharge. In this stage, the gate voltage is given by

$$V_{gs}+i_gR_g+\left(L_g+L_s\right)\frac{\mathrm{d}i_g}{\mathrm{d}t}=0 \tag{20}$$

The delay period ends when the equation below is satisfied

$$I_l=g_m\left(V_{gs}-V_{th}\right) \tag{21}$$

(2) Stage II: Drain-source current decreasing and voltage rising.

When the channel saturation current is less than the inductor current I_l, the bottom switch junction capacitor is discharged by the rest of the I_l. The equivalent circuit is shown in Fig. 7, and the key equations are given by

$$I_l = i_{Ld} + C_{Db}\frac{\mathrm{d}V_{Db}}{\mathrm{d}t} \tag{22}$$

$$i_{Ld} = g_m\left(V_{gs} - V_{th}\right) + C_{gd}\frac{\mathrm{d}V_{gd}}{\mathrm{d}t} + C_{ds}\frac{\mathrm{d}V_{ds}}{\mathrm{d}t} \tag{23}$$

$$V_{dc} = V_{Db} + V_{ds} + \left(L_d + L_s\right)\frac{\mathrm{d}i_{Ld}}{\mathrm{d}t} \tag{24}$$

This period ends when the top switch channel current reaches 0 A.

(3) Stage III: Remaining charging.

In this stage, the top switch junction capacitor C_{ds} resonates with the parasitic inductances of the circuit. The i_{Ld} is easily found from Fig. 7

$$i_{Ld} = C_{gd}\frac{\mathrm{d}V_{gd}}{\mathrm{d}t} + C_{ds}\frac{\mathrm{d}V_{ds}}{\mathrm{d}t} \tag{25}$$

Formulas (21)-(23) are still the state equations for the Stage III until V_{ds} reaches V_{dc}. The total losses of the turn-off transition could be calculated as

$$P_{loss\_off}\left(t\right) = \int_{t_{\mathrm{II}}}^{t_{\mathrm{III}}} V_{ds}\left(t\right)\cdot i_{ch}\left(t\right)\mathrm{d}t \tag{26}$$

3.3 Model implementation

The efficient numerical algorithm that includes switching losses, conduction losses, and passive component losses. The lead inductances and loop inductances could be extracted by measurement or finite element analysis. To ensure the accuracy of the results, the model takes junction capacitances and transconductance into account. Moreover, the nonlinearities of the parameters are modeled by piecewise fitting curves provided by the device datasheets and updated after every step.

Specifically, after deriving the state equations corresponding to all stages, the "ode45" differential equation solver was used in MATLAB to get the expression of $V_{ds}(t)$ and $i_{ch}(t)$ for each subperiod. The final values of one subperiod are treated as the initial conditions for the next subperiod and the duration of each mode can be obtained with the given initial conditions. Because of the sinusoidal inductor current, the transition equations are derived from the simplified equivalent circuits and the total switching losses are calculated using the incremental method of the cycle-by-cycle accumulation in half line period. As shown in Fig. 8, the losses are accumulated for 500 iterations. That is because under the grid frequency of 50 Hz and the switching frequency of 50 kHz, there are exactly 500 iterations within half line period. The remaining power losses, including inductor losses and device conduction losses, are also calculated according to the inductor current.

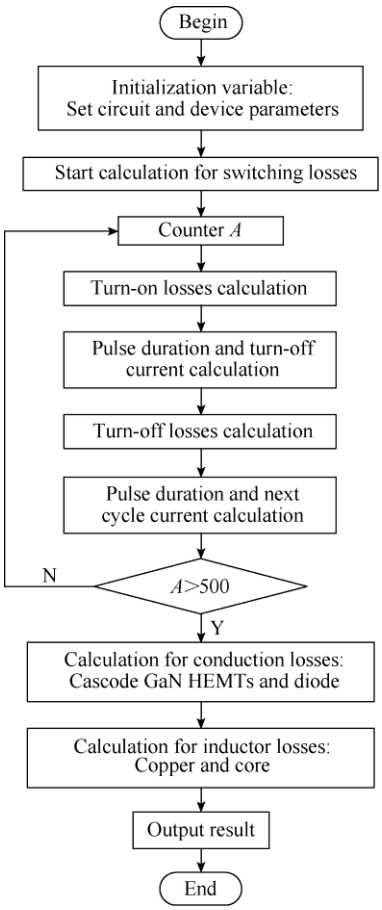

Fig. 8 Calculation flow of the power losses

4 Simulation and experimental results

In this section, the simulation and experimental results are presented to verify the simplified loss model for cascode GaN HEMTs in totem-pole PFC converter.

4.1 Measurement setup

The test converter consists of a symmetric cascode GaN half-bridge with an isolated gate driver, and the photograph is shown in Fig. 9. The bonding stray inductors and the parasitic capacitors inside the package both are neglected to simplify the switching loss calculation, which makes the model more concise and practical. In order to verify the accuracy of loss estimation, A 3.6 kW totem-pole PFC experimental prototype is built using TPH3207WS in a TO-247 package. The converter is running at a switching

frequency of 50 kHz with an 800 μH @0A PFC inductor, whose specifications and parameters are listed in Tab. 1.

2.5 GHz oscilloscope (MDO3024) from Tektronix is used for measurement. The line frequency AC voltage is measured with a high voltage differential probe (Tektronix P5200A), and the drain-source voltage is measured directly at the corresponding transistor pin with a high voltage probe (Tektronix P5120). The line frequency and drain-source current is measured using a AC/DC current probe (Agilent N2782A) with 50 MHz bandwidth and 50 A peak current measurement capability.

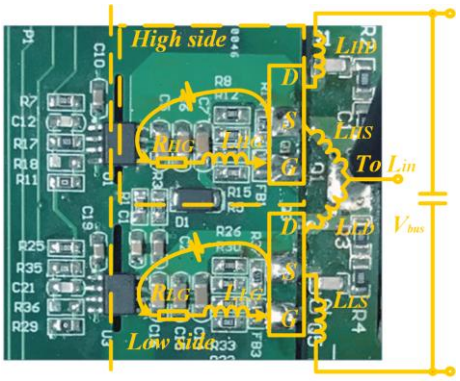

Fig. 9 Experiment prototype of totem-pole PFC GaN bridge

Tab. 1 Parameters and parasitic values

Section	Parameters	Values	Parameters	Values
Circuit inductor	L_s	11.3 nH	L_d	37 nH
	L_g	16.5 nH	L_f(0A)	800 μH
Gate driver	R_g	7.5 Ω	V_g	12 V
Cascode GaN TPH3207WS	Lead inductor	7.5 nH	R_{ds}(25℃)	35 mΩ
Diode DSEI120-06A	r_T	3.5 mΩ	V_{T0}	0.85 V

4.2 Simulation and experimental results

The test converter operate with a 230 V_{rms} input voltage and a 3 600 W output power. Fig. 10 shows the key waveforms measured during the full load operation at high line input. Important intermediate quantities for analytical loss estimation are computed for switching loss. The operating conditions are V_s = 230 V_{rms}, V_{dc} = 400 V and P_{out} = 3 600 W, and the simulation and experimental waveforms match closely in turn on/off speed, current spike and voltage slope as shown in Fig. 11 and Fig. 12. As plotted in Fig. 11, there exist significant distinctions between the measured and simulated current ringing after the transistor is fully turned on. Since the transistor voltage is already equal to zero, there is no additional loss.

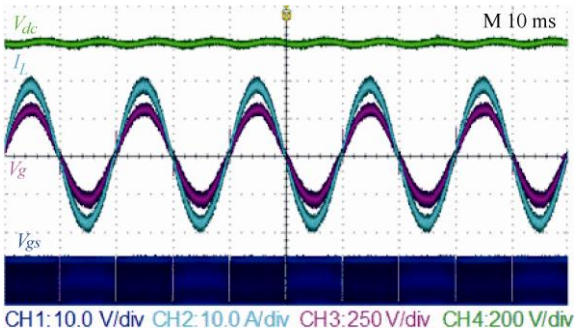

Fig. 10 Key waveforms of totem-pole PFC converter

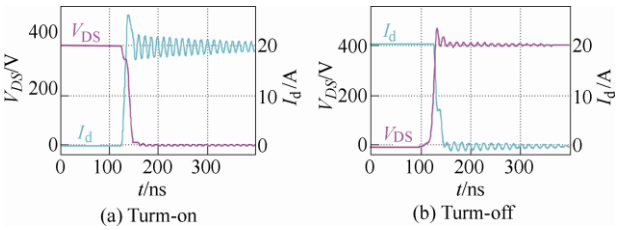

Fig. 11 Bottom switch turn on/off simulation waveforms at hard-switching condition: [400 V, 20 A]

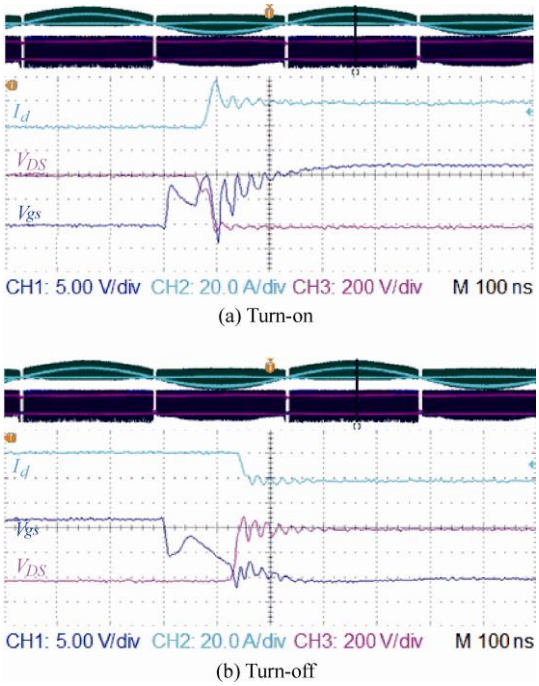

Fig. 12 Bottom switch turn on/off experimental waveforms at hard-switching condition: [400 V, 20 A]

The time delay between gate voltage and drain-source voltage in the experimental waveforms is also remarkable. The cascode GaN device is fabricated by packaging the high-voltage depletion-mode GaN HEMT with a low-voltage enhancement-mode silicon MOSFET. The cascode device is indirectly controlled

by the low voltage MOSFET. Compared with the enhancement-mode GaN HEMTs, the cascode devices have a larger delay from applying the gate voltage to the operation of the high-voltage transistor in nature.

Furthermore, based on the operation principle of the converter, the switching loss calculation requires at least half line cycle accumulation. Meanwhile, the effects of inductor current sinusoidal changes and current ripple that contribute to switching losses are taken into consideration. The estimated totem-pole PFC converter loss is calculated and compared to the experimentally measured loss in Fig. 13, which proves that it is feasible to approximate the switching loss according to the device datasheets. The trend followed by experimental data is clearly reproduced by the model. Peak efficiency of 99.26% is achieved for a 3.6 kW single phase CCM Totem-Pole PFC AC/DC converter switching at 50 kHz based on 650 V cascode GaN HEMTs. Fig. 14 shows the detailed breakdown of losses provided by the proposed method based on the totem-pole PFC converter prototype. The contribution of switching losses to the total losses is above 16% at full load condition. It can be seen that the proportion of the conduction loss is increasing rapidly than the switching loss.

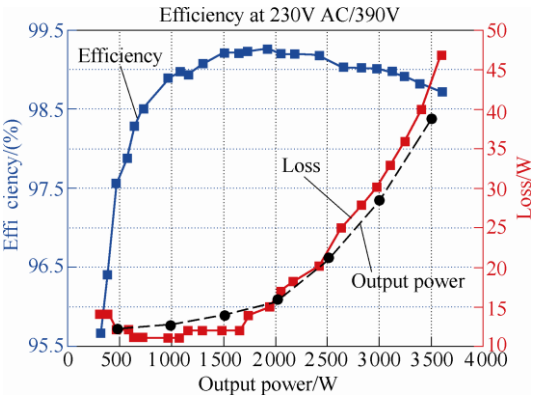

Fig. 13 Comparison between measured (solid lines) and simulation (dash line)

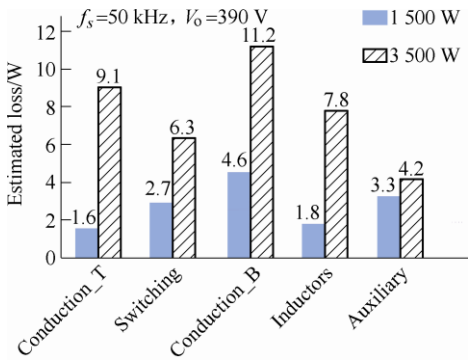

Fig. 14 Totem-pole PFC converter loss decomposition based on proposed model

5 Conclusions

This study presents a simplified switching loss model of cascode GaN HEMTs, which only requires parameters provided by device datasheets. The hard switching process analysis considering the impact of the stray inductances and the nonlinear junction capacitance is illustrated in detail and the implementation method is introduced based Totem-pole PFC converter. In comparison with the established cascode structure analytical models, this paper showed how those models must be redefined in order to simplify calculation process. It is shown that the estimation of losses for hard-switching converters can be achieved with the consideration of the non-ideal parameters. Finally, experiment results validate the correctness of the model in a 3.6 kW single phase CCM Totem-pole PFC converter with peak efficiency of 99.26%.

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