Effect of Center Voltage Vectors (CVVs) of Three-level Space Plane on the Performance of Dual Inverter Fed Open End Winding Induction Motor Drive

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Abstract: Dual inverter fed open end winding induction motor (IM) drive offers many advantages over other multilevel inverter fed IM drives. Pulse width modulation (PWM) techniques are employed for the control of output voltage and frequency. Space vector base PWM techniques are popular among all the PWM techniques. A simplified space vector PWM method with simple and small look-up table approach is presented for dual inverter configuration. Moreover the proposed space vector based PWM technique provides freedom in selecting the center voltage vector (CVV) by which different PWM techniques will be derived. The implementation of all these PWM techniques is generalized by using a constant a_o. The derived PWM techniques show superior performance in reducing the zero sequence voltage (ZSV) by maintaining the same quality of output voltage. The performance of all these PWM techniques are evaluated theoretically and verified in real time through dSPACE 1104 control board.

Keywords: Center voltage vectors, coupled PWM, decoupled PWM, space vector PWM, zero sequence voltage

1 Intrudction

With the advancement in semiconductor technology, voltage source inverter (VSI) fed induction motor (IM) drives are gaining importance. For the control of output voltage and frequency pulse width modulation (PWM) techniques [1-7] are employed to VSI's. As the PWM techniques are employed at high switching frequency, they improve the quality of output but because of switching action they also synthesizes high frequency common mode voltage (CMV) or zero sequence voltage which have adverse effects on motor bearings and electromagnetic interference to nearby systems [8-11].

These PWM techniques can be implemented based on carrier comparison approach and space vector approach [1-7]. Space vector based PWM technique (SVPWM) is a smart PWM technique due to its freedom in selecting voltage vectors [6-7]. The basic performance parameters like output voltage ripple and ZSV have defined the key features to assess the performance of inverter through various space vector based PWM techniques [12-16]. In a conventional two level inverter it is observed that voltage ripple or Total Harmonic Distortion (THD) can be reduced by choosing the nearest voltage states [12-13]. Among the available nearest voltage states, two will be active voltage states (100, 110, etc), and the remaining will be zero voltage states (000, 111). For reduced voltage ripple both the active states and zero states may be utilized satisfying the volt-second balance [12]. Based on the utilization of zero states different discontinuous PWM (DPWM) techniques [12-13] and based on replacement of zero states by active states active zero state PWM (AZSPWM) [14-16] techniques are defined in the literature. All these PWM techniques either decrease the voltage ripple (improve the voltage quality) or decrease the ZSV. The criteria to address the simultaneous reduction of output voltage ripple and ZSV is still to be resolved.

To some extant multilevel inverter topologies like diode clamped, capacitor clamped and H-bridge topologies [17-19] address the issue of simultaneous reduction of output voltage ripple and ZSV. But, these multilevel inverter topologies require clamping diodes, voltage balancing capacitors [20] and separate DC sources for its operation which increases the cost and weight, and there by the efficiency decreases. Along with this, diode clamped multilevel inverters suffers from drawbacks like neutral point fluctuations and

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Digital Object Identifier: 10.23919/CJEE.2019.000010

complexity in control algorithms for higher levels. In Refs. [21-25], a new and effective configuration for IM drive applications called open end winding induction motor (OEWIM) drive was proposed. For a conventional star connected induction motor when the neutral point is removed, a total of six stator terminals will be available as shown in Fig. 1 and it is termed as open end winding induction motor.

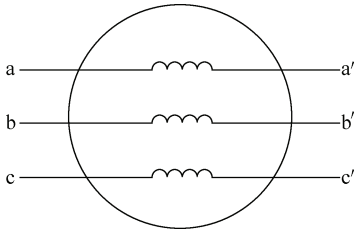


Fig. 1 Open end winding induction motor (OEWIM)

This OEWIM is fed by two-level inverters from both ends with isolated and non isolated (single DC link) DC sources [21]. The isolated DC sources can be easily met in applications where autonomous power supplies are available (like hybrid electrical vehicles, air craft's and ships propulsion). Isolated dual inverter configuration shown in Fig. 2 can arrest the circulating zero sequence currents. In the absence of circulating zero sequence currents zero sequence voltage or ZSV will appear across the negative rails of isolated DC sources (i.e across the potential O and O') [21]. Different coupled and decoupled PWM control strategies and circuit configurations [22-27] are proposed for isolated dual inverter fed open end winding induction motor drives. The implementation of these PWM techniques can be carried out based on space vector approach [22-25] and carrier comparison approach [26-27].

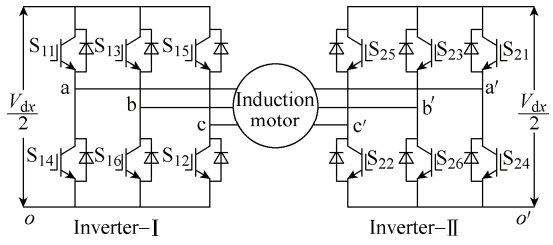


Fig. 2 Dual-inverter configuration with isolated DC

In this paper, a new theory of three-level coupled space vector PWM is presented for OEWIM drive. Conventional three-level coupled space vector PWM implementation requires storage of all the 36 switching states in the form of lookup table [28-29]. At every switching instant the switching states are realized from the look-up table which decreases the processing speed of the controller. The limitations of conventional coupled space vector approach are addressed with the proposed method by using the concept of symmetry of sub hexagons.

The three-level space plane is composed of seven two level regular sub hexagons with one at center and six are at corners as shown in Fig. 3. As the three-level space vector plane is composed of two level hexagons, the realization of three-level space vector PWM can be carried out similar to that of two-level space vector PWM. Hence the CVVs (V_0, V_7, V_8, V_9, V_{10}, V_{11}, V_{12}) of three level space vectors are termed as fictitious zero voltage vectors. Based on selection of center voltage vectors or fictitious zero voltage vectors different PWM techniques like 0127, 012, 721, 6123 yield for dual inverter fed OEWIM drive. The performance analysis of these PWM techniques for dual inverter fed OEWIM drive is evaluated and the results are presented.

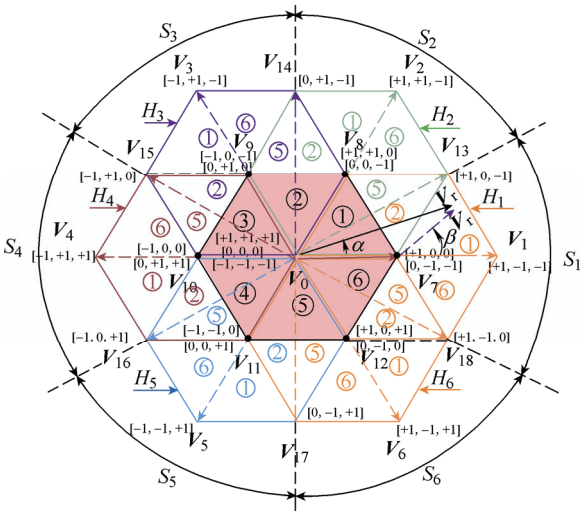


Fig. 3 Three level space plane showing sub hexagons H_1-H_6 and their centers

2 Three level space vector PWM algorithm

The pulse generation process using space vector algorithm is explained with the help of a three-level space vector plane shown Fig. 3. The switching states and their corresponding voltage vectors (V_0-V_{18}), sectors (S_1-S_6), sub hexagons (H_0-H_6) are shown in Fig. 3. In space vector PWM algorithm the voltage to be synthesized by the inverter is specified in terms of the reference voltage vector (V_r) which is a combination of the three instantaneous phase

voltages as given in formula (1). This reference voltage vector makes an angle α that transcend from 0° to 360° in a fixed time determined by the fundamental supply frequency of V_a, V_b and V_c. While transcending it passes through sectors S_1, S_2, ⋯, S_6, which are spatially positioned as given in Tab. 1. Using formula (1) and Tab. 1 the magnitude, angle or position and sector or sub hexagon in which V_r is located will be determined.

$$V_r\angle\alpha = V_a + V_b\exp(j2\pi/3) + V_c\exp(j4\pi/3)$$
$$V_a = \cos(\omega t); V_b = \cos(\omega t - 120^\circ); V_c = \cos(\omega t - 240^\circ) \quad (1)$$

The identified sub hexagons in a three-level space plane are similar to the conventional two-level hexagon. Also it is observed that three-level space plane contains 7 such two-level hexagons. 6 hexagons surround the CVVs (V_0, V_7, V_8, V_9, V_{10}, V_{11} and V_{12}) and one hexagon has the same centre as that of a conventional two level hexagon, shown in Fig. 3. The three-level space plane may be treated as composition of seven two-level space planes. Hence realization of three-level space vector PWM can be carried out similar to that of two-level space vector PWM. So to access the additional states of a three-level inverter, the V_r must be shifted to one of the sub hexagons with tail at its corresponding CVV'. Fig. 4 shows $\boldsymbol{V}_r$, the shifted or new reference voltage vector $\boldsymbol{V}_r'$. The $\boldsymbol{V}_r'$ is synthesized from the actual reference vector $\boldsymbol{V}_r$ by subtracting the corresponding centre voltage vector (CVVs) from $\boldsymbol{V}_r$ as given in formula (2). For this the corresponding CVVs are determined using formula (3) and Tab. 1.

Tab. 1 Sector or sub hexagon identification

Range of α /(°)	Sub hexagon or sector number	θ for calculation of CVVs/(°)
330-30	1	0
30-90	2	60
90-150	3	120
150-210	4	180
210-270	5	240
270-330	6	300

$$V_r'\angle\beta = V_r\angle\alpha - V_c\angle\theta \quad (2)$$

$$V_{cd} + jV_{cq} = 0.5\cos\theta + j0.5\sin\theta = V_c\angle\theta \quad (3)$$

$$Tri = 1 + \mathrm{fix}\left(rem\left(\frac{\beta}{60}\right)\right) \quad (4)$$

After determining the magnitude and position of new reference voltage vector $\boldsymbol{V}_r'$, sub triangle (Tri) in which $\boldsymbol{V}_r'$ is positioned may be determined using formula (4). Once knowing the exact position of $\boldsymbol{V}_r'$ in terms of sub hexagon (H) and sub triangle (Tri), optimal switching states are synthesized from the switching states of H_1 shown in Fig. 4. Optimal switching states are the states which give less voltage ripple satisfying the condition that during state transition, only one state need to change with reference to previous or subsequent state. This is for the reduction of switching losses and improving the overall efficiency of the inverter.

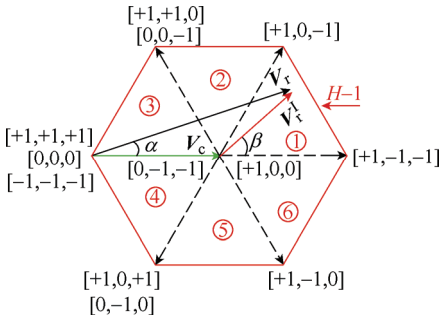


Fig. 4 Switching states and sub triangles of H_1

The nomenclature used for traditional two-level space vector algorithm is still valid with some adaption. '0' and '7' states refer to the two zero states 000 and 111. '1' and '2' refers to the two active states (active states vary depending on the position of V_r). At any switching instant these four switching states form a group of optimal switching states. In conventional two-level space vector PWM both the zero states and two active states are utilized in every switching cycle. The salient feature connecting the two-level and three-level implementation is that zero states of two-level are replaced with center voltage vectors (CVVs) or fictitious zero voltage vectors of three level space vector in every switching cycle. For instance if the instantaneous position of V_r' at a given switching instant is in sub triangle 1 of H1 the state '0' refers to 0-1-1, state '7' refers to 100, state '1' refers to 1-1-1 and state '2' refers to 10-1. Similarly based on position and sub triangle in which V_r' lies, the active and zero vectors can be used as given as in Tab. 2. Once the switching states are realized their dwell times are derived from the magnitude and angle information using formulas (5)-(7) [12, 28-29] similar to

that as done for two-level inverter times. Here T_1, T_2 are the active state durations and T_Z is the zero state duration in one sampling time T_S. V_{dc} is the normalized DC voltage. The zero state duration is equally shared among zero states. The term modulation index is defined by formula (8).

$$T_1 = \frac{V_r^{'}}{0.5 * V_{dc}} \frac{\sin\left(60^\circ - \beta\right)}{\sin\left(60^\circ\right)} T_S \tag{5}$$

$$T_2 = \frac{V_r^{'}}{0.5 * V_{dc}} \frac{\sin\left(\beta\right)}{\sin\left(60^\circ\right)} T_S \tag{6}$$

$$T_Z = T_S - (T_1 + T_2) \tag{7}$$

$$M = \frac{V_r}{2/3 V_{dc}} \tag{8}$$

2.1 Conventional Approach

Fig. 5a shows the flow chart for the realization of optimal switching states of a three level inverter through conventional space vector PWM approach. After finding the sub hexagon and sub triangle in which $\boldsymbol{V}_r'$ falls in, the nearest switching states are used to synthesize $\boldsymbol{V}_r'$. Hence, in conventional approach all the 36 switching states as given in Tab. 2 must be fed as input in the form of look-up table to synthesize $\boldsymbol{V}_r'$ based on the sub hexagon and sub triangle in which it resides. The limitation with the conventional approach is that Tab. 1 should be made as a look-up table and this needs large memory. Moreover, at every switching instant the switching states are to be realized from the look-up table which decreases the processing speed of the controller. The limitations of this approach are addressed with the proposed method.

2.2 Proposed simplified approach

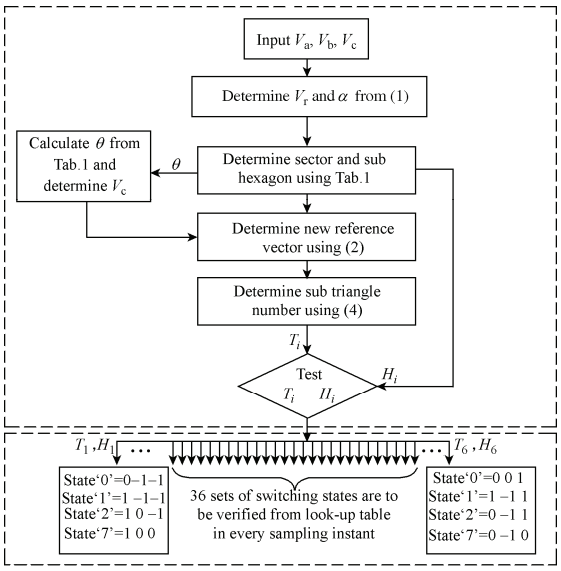
To save the controller memory and improve processing speed of the controller, some improvements are incorporated in the proposed method. Improvement with the proposed approach uses the principle of symmetry of sub hexagons and the optimal switching states are realized from the optimal switching of $\boldsymbol{V}_r'$ in H_1. For instance if $\boldsymbol{V}_r'$ resides in triangle-1 of H_1 then the four nearest switching states are 0–1–1, 1–1–1, 10–1, 100. These can be named as A1, A2 and A3 as given in second row, second column of Tab. 3. Similarly if the reference vector $\boldsymbol{V}_r'$ lies in triangle 1 of H_2 then the four switching states can be derived by replacing A1, A2, A3 with –A2,–A3,–A1 respectively which yields 110, 11–1, 01–1, 00–1 respectively.

Tab.2 Switching states used in different sub-triangles of all sub hexagons

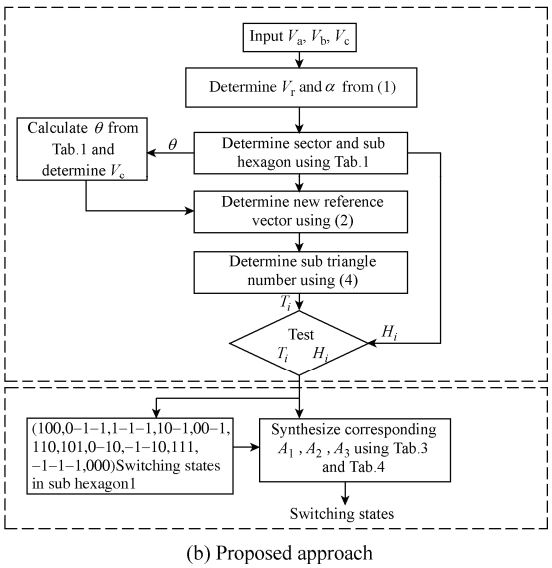
Sub hexagon	Sub triangle	'0' state	'1' state	'2' state	'7' state
H1	1	0–1–1	1–1–1	10–1	100
	2		0–0–1	10–1	
	3		00–1	000	
	4		0–10	000	
	5		0–10	1–10	
	6		1–1–1	1–10	
H2	1	00–1	01–1	11–1	110
	2		01–1	010	
	3		000	010	
	4		000	100	
	5		10–1	100	
	6		10–1	11–1	
H3	1	–10–1	–11–1	–110	010
	2		–100	–110	
	3		–100	000	
	4		00–1	000	
	5		00–1	01–1	
	6		–11–1	01–1	
H4	1	–100	–101	–111	011
	2		–101	001	
	3		000	001	
	4		000	010	
	5		–110	010	
	6		–110	–111	
H5	1	–1–10	–1–11	0–11	001
	2		0–10	0–11	
	3		0–10	000	
	4		–100	000	
	5		–100	–101	
	6		–1–11	–101	
H6	1	0–10	1–10	1–11	101
	2		1–10	100	
	3		000	100	
	4		000	001	
	5		0–11	001	
	6		0–11	1–11	

Tab. 3 Realization of switching states of all sub hexagons from H_1 states

Sub hexagon	H1			H2			H3			H4			H5			H6		
0127	0	–1	–1→0	1	1	0→7	–1	0	–1→0	0	1	1→7	–1	–1	0→0	1	0	1→0
	1	–1	–1→1	1	1	–1→2	1	1	–1→1	–1	1	1→2	–1	–1	1→1	1	–1	1→1
	1	0	–1→2	0	1	–1→1	–1	1	0→2	–1	0	1→1	0	–1	1→2	1	–1	0→2
	1	0	0→7	0	0	–1→0	0	1	0→7	–1	0	0→0	0	0	1→7	0	–1	0→7
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	A1	**A2**	**A3**	**–A2**	**–A3**	**–A1**	**A3**	**A1**	**A2**	**–A1**	**–A2**	**–A3**	**A2**	**A3**	**A1**	**–A3**	**–A1**	**–A2**



(a) Conventional approach



(b) Proposed approach

Fig. 5 Flow chart of three level space vector PWM

This is generalized for all sub triangles of all sub hexagons and is presented in Tab. 3. In Tab. 3 as an example it is shown for $\boldsymbol{V}_r'$ in T1 in all sub hexagons. The same can be applied for $\boldsymbol{V}_r'$ in all triangles of all sub hexagons following the principle of symmetry as given in Tab. 3. With this approach the size of the look-up table and hence memory requirement reduces to one-sixth of that required with the conventional approach and so processing speed is enhanced for the same switching frequency. Fig. 5b shows the flow chart of the proposed approach. Once switching states are derived dwell times are calculated from the magnitude and angle information using formulas (5)-(7).

3 Space vector PWM for dual inverter configuration

In Fig. 2 the circuit configuration of isolated dual inverter fed OEWIM drive is presented. The DC link voltage of $V_{dc}/2$ is applied to each two-level inverter to get an effective DC voltage of V_{dc}. Here V_{ao},V_{bo},V_{co} refers to inverter-I pole voltages, $V_{a'o'}$,$V_{b'o'}$, $V_{c'o'}$ refers to inverter-II pole voltages, $V_{aoa'o'}$,$V_{bob'o'}$,$V_{coc'o'}$ refers to effective pole voltage and $V_{aa'}$,$V_{bb'}$,$V_{cc'}$ refers to effective phase voltages. The pole voltages generated by each inverter is equal to $V_{dc}/2$ (when top switches are ON) or 0 (when bottom switches are ON). The effective pole voltage of OEWIM drive is given by formula (9). The ON state switches of each inverter and the calculated effective pole voltages are given Tab. 4.

$$V_{xox'o'} = V_{xo} - V_{x'o'} \qquad x = a,b,c \tag{9}$$

From Tab. 4, it is observed that isolated dual inverter fed OEWIM drive is capable of generating three-level effective pole voltage ($-V_{dc}/2$, 0, $V_{dc}/2$) and hence this configuration is called as three-level inverter configuration. The three-level switching states can be resolved as given in Tab. 5 to generate three-level output voltage from a dual inverter fed OEWIM drive. The mathematical expression for effective phase voltages in terms of effective pole voltages is given by formula (10).

Tab. 4 Effective pole voltage calculation

Switches to be turned ON in inverter-I	Inverter-I pole voltage	Switches to be turned ON in inverter-II	Inverter-II pole voltage	Effective pole voltage
S14 or S16 or S12	0	S25 or S23 or S21	$V_{dc}/2$	$-V_{dc}/2$
S14 or S16 or S12	0	S22 or S24 or S26	0	0
S11 or S13 or S15	$V_{dc}/2$	S25 or S23 or S21	$V_{dc}/2$	0
S11 or S13 or S15	$V_{dc}/2$	S22 or S24 or S26	0	$V_{dc}/2$

Tab. 5 Switching state selection of inverter-I & inverter-II

Switching state	Pole voltage	Switching stage of inverter-I	Switching stage of inverter-II
+1	$V_{dc}/2$	1	0
0	0	1 or 0	1 or 0
–1	$-V_{dc}/2$	0	1

$$\begin{aligned} V_{aa'} &= \frac{2}{3}V_{aoa'o'} - \frac{1}{3}V_{bob'o'} - \frac{1}{3}V_{coc'o'} \\ V_{bb'} &= \frac{2}{3}V_{bob'o'} - \frac{1}{3}V_{aoa'o'} - \frac{1}{3}V_{coc'o'} \\ V_{cc'} &= \frac{2}{3}V_{coc'o'} - \frac{1}{3}V_{bob'o'} - \frac{1}{3}V_{aoa'o'} \end{aligned} \tag{10}$$

As both the two-level inverters are isolated circulating zero sequence current will be absent but the zero sequence voltage will appear across the negative rails of inverters. The zero sequence voltage for the dual inverter fed OEWIM drive can be expressed mathematically as in formula (11) and measured across the terminals O and O'. At high switching frequencies and high input DC voltages, sharp edges of ZSV causes different currents (inverters to ground and motor to ground) which have adverse effects on motor bearings and electromagnetic interference on the nearby electronic systems.

$$\begin{aligned} V_{ZSV} &= V_{ZSV1} - V_{ZSV2} = \\ \frac{V_{ao} - V_{a'o'} + V_{bo} - V_{b'o'} + V_{co} - V_{c'o'}}{3} &= V_{OO'} = \\ \frac{V_{aoa'o'} + V_{bob'o'} + V_{coc'o'}}{3} & \end{aligned} \tag{11}$$

The calculated effective phase voltage levels for one quarter cycle with 0127 sequence is given in Tab. 6. It is observed that the effective phase voltage has voltage levels at 0, $V_{dc}/3$, $V_{dc}/2$ and $2V_{dc}/3$ with voltage step of $V_{dc}/6$ and $V_{dc}/3$ in one quarter cycle. For the remaining cycle magnitude of voltage step will not be affected and only change will be there in their polarities for the remaining cycle. The calculated zero sequence voltage with 0127 sequence is also given in Tab. 6. From Tab.6 it is observed that 0127 sequence generates a peak to peak CMV of $2V_{dc}/3$ with voltage levels $-V_{dc}/3$, $-V_{dc}/6$, 0, $V_{dc}/6$ and $V_{dc}/3$.

Tab. 6 Calculated effective phase voltage and zero sequence voltage with 0127 sequence (PMW1)

Sector & sub triangle	Sequence	Voltage vectors	Switching states of inverter-I	Switching states of inverter-II	Effective phase voltage	Effective ZSV V_{ZSV}
S1-5	0	0-1-1	100	111	$V_{dc}/3$	$-V_{dc}/3$
	1	0-10	101	111	$V_{dc}/6$	$-V_{dc}/6$
	2	1-10	101	011	$V_{dc}/2$	0
	7	100	111	011	$V_{dc}/3$	$V_{dc}/6$
S1-6	0	0-1-1	100	111	$V_{dc}/3$	$-V_{dc}/3$
	1	1-1-1	100	011	$2V_{dc}/3$	$-V_{dc}/6$
	2	1-10	101	011	$V_{dc}/2$	0
	7	100	111	011	$V_{dc}/3$	$V_{dc}/6$
S1-1	0	0-1-1	100	111	$V_{dc}/3$	$-V_{dc}/3$
	1	1-1-1	100	011	$2V_{dc}/3$	$-V_{dc}/6$
	2	10-1	110	011	$V_{dc}/2$	0
	7	100	111	011	$2V_{dc}/3$	$V_{dc}/6$
S1-2	0	0-1-1	100	111	$V_{dc}/3$	$-V_{dc}/3$
	1	10-1	110	011	$V_{dc}/2$	0
	2	00-1	110	111	$V_{dc}/6$	$-V_{dc}/6$
	7	100	111	011	$V_{dc}/3$	$V_{dc}/6$
S2-5	0	00-1	110	111	$V_{dc}/6$	$-V_{dc}/6$
	1	10-1	110	011	$V_{dc}/2$	0
	2	100	111	011	$V_{dc}/3$	$V_{dc}/6$
	7	110	111	001	$V_{dc}/6$	$V_{dc}/3$
S2-6	0	00-1	110	111	$V_{dc}/6$	$-V_{dc}/6$
	1	10-1	110	011	$V_{dc}/2$	0
	2	11-1	110	001	$V_{dc}/3$	$V_{dc}/6$
	7	110	111	001	$V_{dc}/6$	$V_{dc}/3$
S2-1	0	00-1	110	111	$V_{dc}/6$	$-V_{dc}/6$
	1	01-1	110	101	0	0
	2	11-1	110	001	$V_{dc}/3$	$V_{dc}/6$
	7	110	111	001	$V_{dc}/6$	$V_{dc}/3$
S2-2	0	00-1	110	111	$V_{dc}/6$	$-V_{dc}/6$
	1	01-1	110	101	0	0
	2	010	111	101	$-V_{dc}/6$	$V_{dc}/6$
	7	110	111	001	$V_{dc}/6$	$V_{dc}/3$

4 Effect of center voltage vectors (CVVs) on the performance of dual inverter configuration

From the principles of space vector PWM [6, 12], in a sample time Ts both the active states (1&2) and either or both the zero vectors (0 & 7) are used to

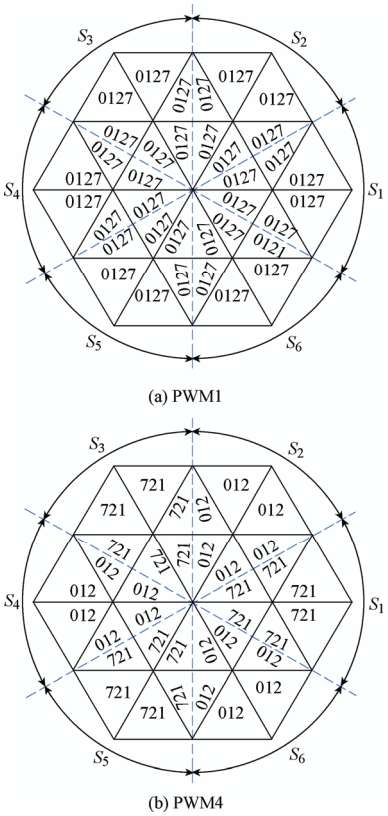
synthesize reference voltage vector. Utilizing the freedom of choosing the zero vector, leads to numerous PWM techniques [6, 12]. The zero vectors of two-level are replaced with center voltage vectors or fictitious zero voltage vectors of three level space vector plane. Hence, with choice in selecting center voltage vectors or fictitious zero voltage vectors yields to new PWM techniques.

4.1 Proposed PWM techniques for dual inverter configuration

The selection and positioning of voltage vectors is based on minimum state transitions in every switching cycle. Using principle of one state transition change, in conventional SVPWM switching states are selected as 0–1–1, 1–1–1, 10–1, 100 (0127 sequence here after referred as PWM1). In conventional SVPWM discussed in Section 2 both the active states and both fictitious zero states are used with zero state time equally shared between the two fictitious zero voltage vectors. Different sequences derived by eliminating one of the fictitious zero voltage vectors are 0-1-1, 1-1-1, 10-1 (012 sequence here after referred as PWM2) and 100, 10-1, 1-1-1 (721 sequence here after referred as PWM3). In PWM2 100 state and in PWM3 0-1-1 are eliminated to derive 012 and 721 sequences satisfying the conditions of space vector PWM. In PWM2 fictitious zero voltage vectors 7 and in PWM3 fictitious zero voltage vectors 0 are eliminated in the sectors S1-S6. After eliminating these fictitious zero voltage vectors effective phase voltage and zero sequence voltage are calculated using formulas (10)-(11). Since all the sub triangles of sub hexagons are symmetrical, the calculation of effective phase voltage and common mode voltage with 012 and 721 sequences is presented only for one sub triangle in each sub hexagons.

From Tab. 6 it is observed that with the elimination of fictitious zero voltage vectors 0 and 7 the magnitude of voltage step remains unaffected in effective phase voltage. With 012 sequence in all the even hexagons (S2, S4, S6) voltage level of $V_{dc}/3$ is eliminated from the zero sequence voltage but in all odd hexagons (S1, S3, S5) voltage level of $-V_{dc}/3$ still appears. With 721 sequence in all the even hexagons (S2, S4, S6) voltage level of $V_{dc}/3$ is in zero sequence voltage but in all odd hexagons (S1, S3, S5) voltage level of $-V_{dc}/3$ is eliminated. Based on pulse pattern analysis it is observed that with both 012 and 721 sequences voltage level and magnitude of voltage step in effective phase voltage remains unaffected but the peak to peak zero sequence voltages magnitude is reduced to $V_{dc}/2$ when compared with 0127 sequence.

With an idea to maintain the same effective phase voltage and to reduce the zero sequence voltage a new PWM technique (PWM4) is developed by combing both 012 (PWM2) and 721 (PWM3) sequences. In the proposed PWM4 in all odd sectors (S1, S3, S5) state '0' should be eliminated (which mean 721 sequence should be employed) and in all even sectors (S2, S4, S6) state '7' should be eliminated (which mean 012 sequence should be employed). The fictitious zero vector usage in different sub triangles of all the sub hexagons with PWM1 and PWM4 are shown in Fig. 6. Such a PWM technique will maintain same effective phase voltage but peak to peak zero sequence voltage is reduced to $V_{dc}/3$ with voltage levels $-V_{dc}/6$, 0 and $V_{dc}/6$. Hence it is observed that PWM4 is able to reduce 50% of zero sequence voltage maintaining same effective phase voltage.



(a) PWM1

(b) PWM4

Fig. 6 Zero states usage in different sub triangles and sub hexagons

In conventional two-level SVPWM in order to reduce common mode voltage different PWM techniques like

AZSPWM and NSPWM techniques were proposed [14-15]. In these PWM techniques zero state is replaced by active states. These PWM techniques follow switching sequences like 6123,123, 612, etc replacing the zero voltage vector with the nearby adjacent voltage vectors. These PWM techniques reduce zero sequence voltage but decrease the quality of output voltage because of using the nearby active and their adjacent voltage vectors like 6 and 3.

If same switching sequence is employed for three-level output the performance parameters like effective phase voltage and zero sequence voltage with sequence 6123 is investigated in Tab. 7. From Tab. 7 it is observed that with the usage of vectors 6 and 3, voltage levels in effective phase voltage are having a magnitude of $V_{dc}/2$, $V_{dc}/3$ and $V_{dc}/6$. When compared with other PWM techniques (PWM1, PWM2, PWM3 and PWM4) the magnitude of voltage level is high in 6123 sequence (PWM5). This is because of using adjacent active vectors in place of fictitious zero voltage vectors. As the magnitude of voltage step changed from $V_{dc}/3$ to $V_{dc}/2$, harmonics contentment present in the voltage also increases. Though the magnitude of voltage step in effective voltage is increased, the zero sequence voltage is having a peak-to-peak value of $V_{dc}/3$ with 6123 sequence (PWM5). ZSV remains same as PWM4 but the harmonic content present in the effective voltage is increased. Hence PWM4 is preferred when compared with 6123 sequence (PWM5). Also PWM4 has same quality of output as PWM1, PWM2 and PWM3 but generates low zero sequence voltage.

Tab. 7 Calculated Effective phase voltage and zero sequence voltage with 6123 sequence (PMW4)

Sector & sub triangle	Voltage vectors	Switching states of inverter-I	Switching states of inverter-II	Effective phase voltage	Effective ZSV V_{ZSV}
S1-1	**1-10**	**101**	**011**	$\boldsymbol{V_{dc}/2}$	**0**
	1-1-1	100	011	$2V_{dc}/3$	$-V_{dc}/6$
	10-1	110	011	$V_{dc}/2$	0
	00-1	**110**	**111**	$\boldsymbol{V_{dc}/6}$	$\boldsymbol{V_{dc}/6}$
S2-1	**010**	**111**	**101**	$\boldsymbol{-V_{dc}/6}$	$\boldsymbol{V_{dc}/6}$
	01-1	110	101	0	0
	11-1	110	001	$V_{dc}/3$	$V_{dc}/6$
	10-1	**110**	**011**	$\boldsymbol{V_{dc}/2}$	**0**

4.2 Realization of proposed PWM techniques

The realization of proposed PWM2, PWM3 and PWM4 can be carried out in similar way as that of PWM1. In PWM1 the fictitious zero voltage vector time or dwell time T_Z is shared equally among two fictitious zero voltage vectors. In order to generalize all the PWM techniques two new dwell times T_0 (dwell time of zero vector '0') and T_7 (dwell time of zero vector '7') are introduced as given in formula (12) which will be derived from original dwell time T_Z. Here a_o is a constant which can take values between 0 and 1.

$$T_0 = a_o T_Z \ \ and \ T_7 = (1 - a_o) T_Z \tag{12}$$

CSVPWM or PWM1 technique can be realized by choosing a_o=0.5. With a_o=0.5, formula (12) can be written as T_0=0.5T_Z and T_7=0.5T_Z, which indicate equal division of dwell time T_Z among the fictitious zero voltage vector. Hence choosing a_o=0.5 yields PWM1. By choosing a_o=1, formula (12) can be written as T_0=T_z and T_7= 0 which indicates that dwell time T_z is assigned to only one fictitious zero voltage vector 0. Hence choosing a_o=1 yields PWM2. Choosing a_o=0, formula (12) can be written as T_0=0 and T_7= T_z which indicate the allocation of dwell time T_z to only one fictitious zero voltage vector 7. Hence choosing a_o=0 yields PWM3. Similarly choosing a_o=0 for all odd sectors (S1, S3, S5) and choosing a_o=1for all even sectors (S2, S4, S6) yields PWM4.

For PWM1, PWM2 and PWM3 the value of a_o is constant in all the sectors and it is easy to generate. But for PWM4 the value of a_o is different for each sector. This complexity is eliminated and it is calculated in simple way from instantaneous reference voltages using formula (13). Here V_{max} and V_{min} are the instantaneous maximum and minimum values of commended reference signals at any given instance.

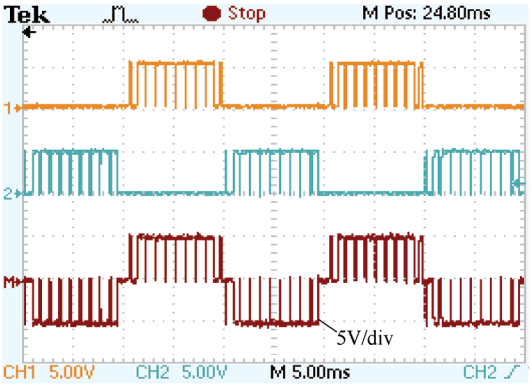
$$\begin{aligned} V_{max} + V_{min} < 0 \ \ then \ \ a_o = 0 \\ V_{max} + V_{min} \geqslant 0 \ \ then \ \ a_o = 1 \end{aligned} \tag{13}$$

For PWM5 zero states times is equally shared between new active voltage vectors 3 and 6. Hence to implement PWM5 a_o is chosen as 0.5.

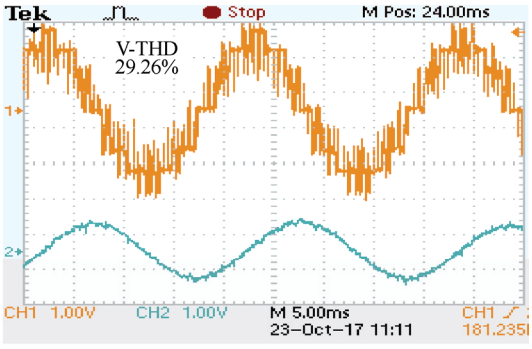
5 Results and discussion

To verify the performance of various coupled space vector based PWM techniques experimental tests have been carried on V/f controlled open end winding induction motor drive. The control signals are generated by using dSPACE 1104 control board at a

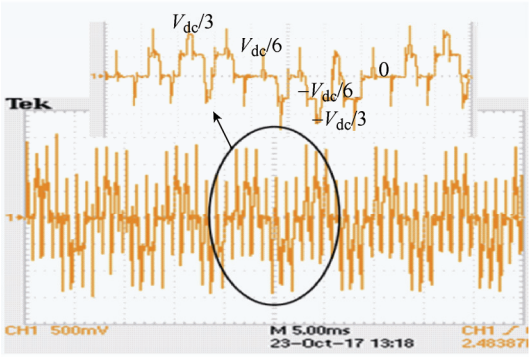
switching frequency of 1 kHz. The three phase 1 Hp, 415 V, 1.8 A and 50 Hz open end winding induction motor is fed from two 9.2 kVA DC link converters which have uncontrolled rectifier in its front end and PWM inverter at the back end. A DC bus voltage of 255 V is employed to each PWM inverter (effective DC voltage 510 V). For the result analysis, 500 V to 3.3 V regulator (LV20-P) is used to measure effective phase voltage and zero sequence voltage. The results of pulse patterns of a-phase top switches in both the inverters, calculated effective pole voltage, effective phase voltage, phase current and zero sequence voltage with PWM1 to PWM5 are shown in Fig. 7 to Fig. 11.



(a) Pulse pattern for inverter-Ⅰ, inverter-Ⅱ and calculated effective pole voltage of phase-a

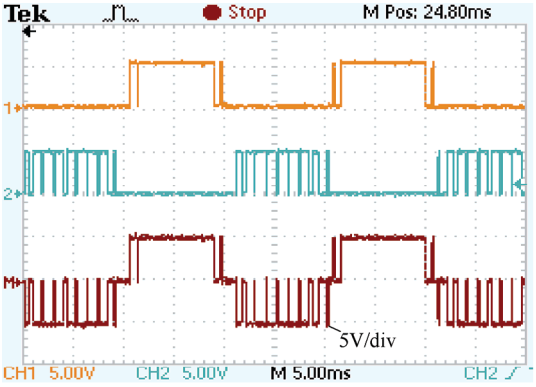


(b) Effective phase voltage and phase current

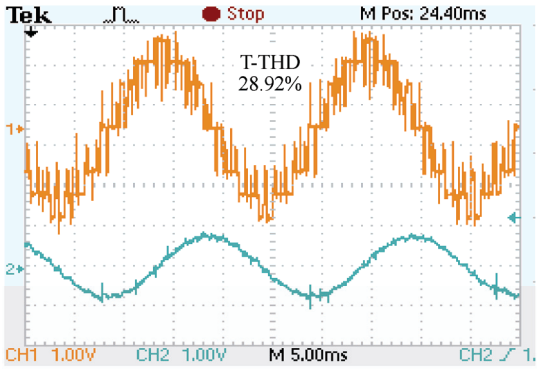


(c) Zero-sequence voltage

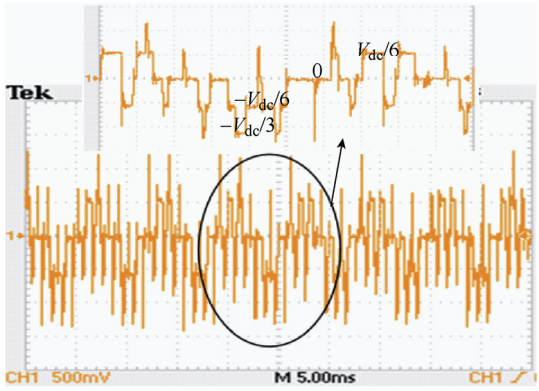
Fig. 7 Results of dual inverter fed OEWIM drive with 0127 sequence (PWM1) at M=0.83



(a) Pulse pattern for inverter-Ⅰ, inverter-Ⅱ and calculated effective pole voltage of phase-a

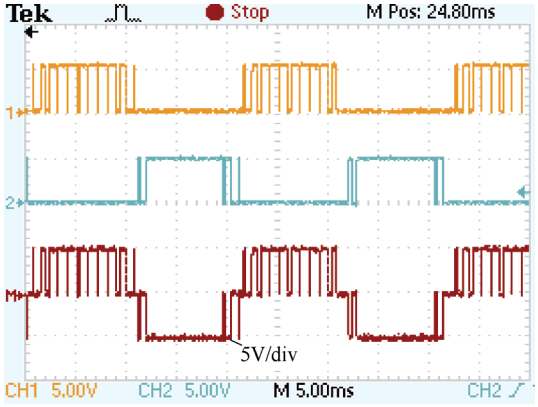


(b) Effective phase voltage and phase current

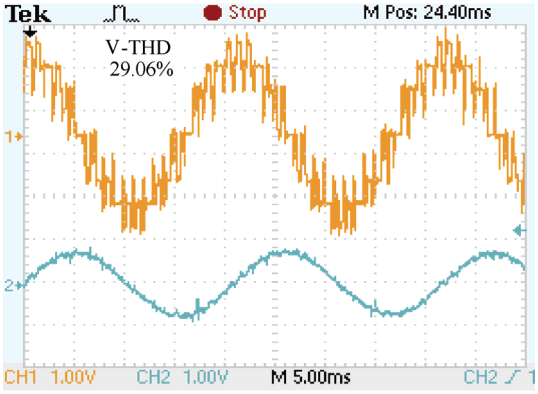


(c) Zero sequence voltage

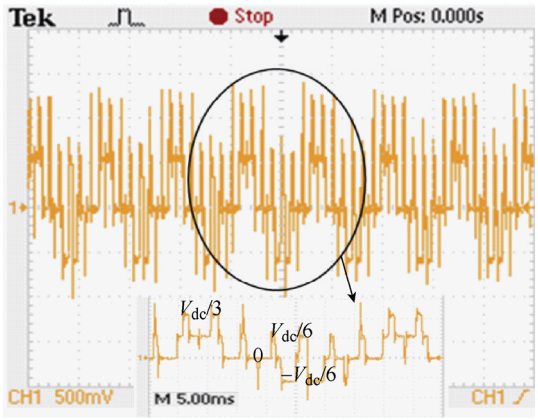
Fig. 8 Results of dual inverter fed OEWIM drive with 012 sequence (PWM2) at M=0.83



(a) Pulse pattern for inverter-Ⅰ, inverter-Ⅱ and calculated effective pole voltage of phase-a

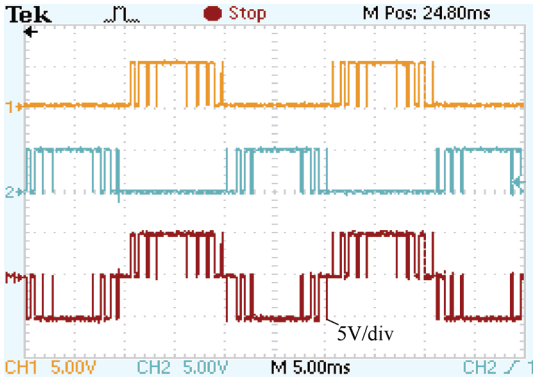


(b) Effective phase voltage and phase current

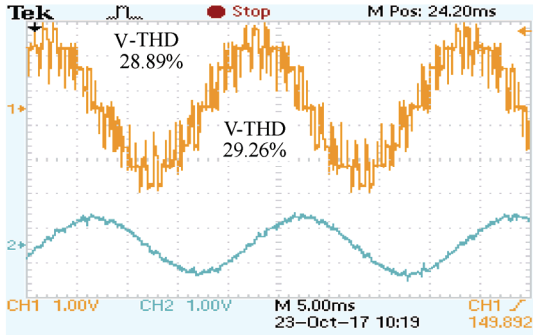


(c) Zero-sequence voltage

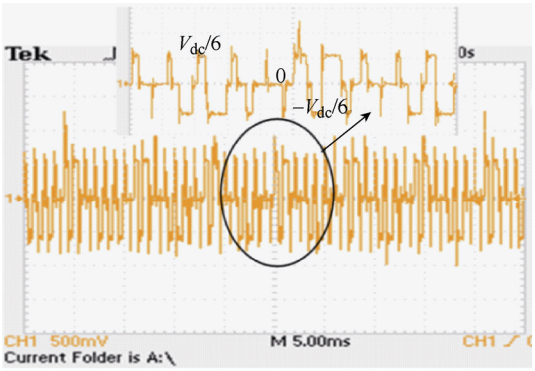
Fig. 9 Results of dual inverter fed OEWIM drive with 721 sequence (PWM3) at M=0.83



(a) Pulse pattern for inverter-Ⅰ, inverter-Ⅱ and calculated effective pole voltage of phase-a

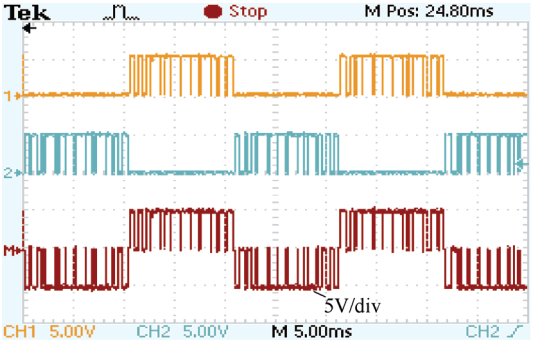


(b) Effective phase voltage and phase current

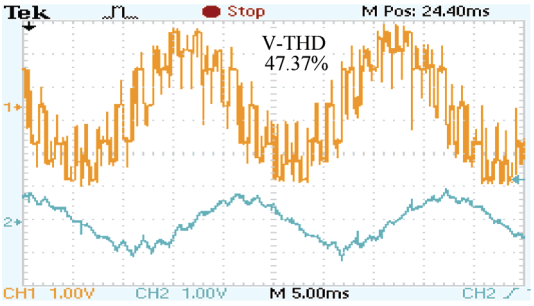


(c) Zero-sequence voltage

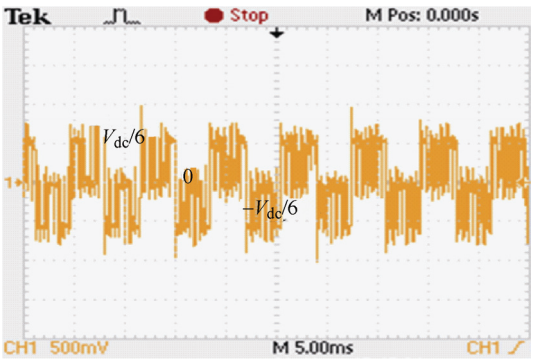
Fig. 10 Results of dual inverter fed OEWIM drive with 012&721 sequence (PWM4) at M=0.83



(a) Pulse pattern for inverter-Ⅰ, inverter-Ⅱ and calculated effective pole voltage of phase-a



(b) Effective phase voltage and phase current



(c) Zero-sequence voltage

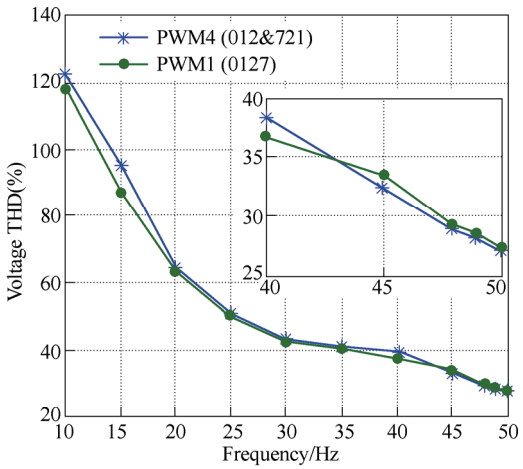
Fig. 11 Results of dual inverter fed OEWIM drive with 6123 sequence (PWM5) at M=0.83

It can be noted that with 0127 sequence or PWM1 and PWM5 as shown in Fig. 7a and Fig. 11a, for an output frequency f ($T=1/f$), the associated

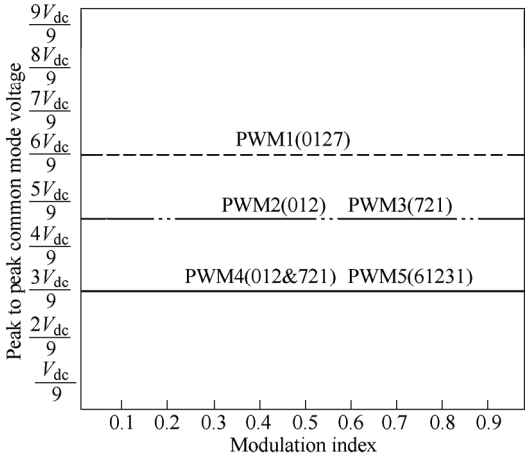
phase in inverter-I will be in operation for a time period of $T/2$ and remains clamped for $T/2$ time period. It is also observed that when a-phase of inverter-I is in operation then a-phase of inverter-II will be clamped and vice versa. Hence it can be concluded that when compared with conventional two-level inverter, switching of each two-level inverter used in dual inverter configuration is reduced by 50%. With PWM2 as shown in Fig. 8a the pulse pattern of inverter-I is clamped for a time period $2T/3$ in time interval $T/2$.

Hence 83.33% of inverter-I switching is reduced and as switching of inverter-II remains unaffected and same as PWM1 so 50% of switching is reduced. Similarly with PWM3 as shown in Fig. 9a. 83.33% of inverter-II switching is reduced and as switching of inverter-I remains unaffected and same as PWM1 so 50% of switching is reduced. With PWM 4 as shown in Fig. 10a, 66.67% of both the inverters switching is reduced. Because pulse pattern of both the inverters are clamped to time period T/3 in time interval T/2. Though switching is different all the PWM techniques will generate an effective pole voltage with voltage levels $V_{dc}/2$, 0 and $-V_{dc}/2$.

The voltage levels created in effective phase voltage as shown in Fig. 7b to Fig. 11b with different PWM techniques are matched with the theory discussed in Section 5. The voltage levels with PWM1, PWM2, PWM3 and PWM4 techniques look symmetrical and having a magnitude of $V_{dc}/6$ or $V_{dc}/3$. As magnitude of voltage level and number of voltage steps are same with PWM1, PWM2, PWM3 and PWM4 techniques THD is slightly effected. The difference in their THD is due to change in pulse position. The voltage levels creased with PWM5 are having a magnitude of $V_{dc}/6$ or $V_{dc}/3$ or $V_{dc}/2$. The high magnitude of voltage step ($V_{dc}/2$) is due to the selection on non-nearest or adjacent voltage vectors of active voltage vector. Hence the THD of effective phase voltage is high with PWM5 when compared with PWM1, PWM2 PWM3 and PWM4. As the modulation index decreases magnitude of voltage step remains same but number of voltage steps decreases. Hence as modulation index decrease THD increases and drive operates with reduced quality of output voltage. As the voltage harmonics increases current harmonics also increase. For simplicity the variation of effective phase voltage THD at different frequencies with PWM1 and PWM4 are presented in Fig. 12 a. For modulation index less than 0.74 PWM1 has superior performance and for modulation index greater than 0.74 PWM4 has superior performance. For clear visualization the variation of THD with PWM2 and PWM3 were not presented but at all the modulation indices PWM2 and PWM3 THD plots lies between the curves of PWM1 and PWM4.



(a) Voltage THD at different frequencies



(b) Peak-to-peak CMV profile

Fig.12 Voltage THD at different frequencies peak to peak CMV profile

The levels created by the ZSV in one sampling times (T_s) can be observed from the zoomed portions of Fig. 7c to Fig. 11c. The ZSV profiles obtained theoretically in Section 4 (Tab. 6) are in agreement with experimentally results shown in Fig. 7c to Fig. 11c. It is observed in Fig. 7c that PWM1 generates a ZSV of $-V_{dc}/3$ and $V_{dc}/3$. From Fig. 9c it is observed that with 012 it is reduced to $V_{dc}/6$ and $-V_{dc}/3$.

From Fig. 9c it is observed that with 721 it is

reduced to $V_{dc}/3$ and $-V_{dc}/6$. From Fig. 10c and Fig.11c it is observed that With PWM4 and PWM5 it further reduces to $V_{dc}/6$ and $-V_{dc}/6$. Due to switching non-idealities (dead time and etc) ZSV levels during switching transients will deviate from being ideal. It can therefore be concluded that PWM4 and PWM5 generates low zero sequence voltage when compared with PWM1. The zero sequence voltage profiles with all the PWM techniques at all the modulation indices are shown in Fig. 12b. In the entire of modulation index PWM4 and PWM5 has very low peak to peak zero sequence voltage of $V_{dc}/3$ ($\pm V_{dc}/6$).

6 Conclusions

The present work mainly focuses on two issues that improve the performance of the dual inverter fed open end winding induction motor. Firstly a generalized space vector approach that doesn't requires storage of lengthy look-up tables as in the conventional approach presented.

This approach provides freedom in selecting fictitious zero voltage vectors or CVVs. Utilizing the freedom in selecting CVVs five types of PWM techniques were derived for dual inverter configuration. Secondly the effect of CVVs in reducing the zero sequence voltage in comparison with the conventional PWM is highlighted. The practical results also validate that PWM4 (012 & 721 sequence) give superior performance by reducing zero sequence voltage still maintaining good quality of output voltage profile at all the modulation indices.

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