CSI and CSI7 Current Source Inverters for Modular Transformerless PV Inverters*

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Abstract: Current source inverter (CSI) is a class of power electronic converters that, thanks to the inherent boost capability and ease of control, is investigated for grid-tied photovoltaic power conversion applications. Traditional CSI and CSI7 topologies are here analyzed and compared with two kind of space vector modulation strategies mainly in terms of ground leakage current both in simulations and experiments. Furthermore, THD of the injected grid current and the computation of conduction and switching semiconductor power losses are also carried out in numerical simulations. The topology comparison is carried out with the use of a different number of PV modules, to analyze the robustness of the topologies to different size of the PV strings. Simulation and experimental results show that the CSI7 topology, with respect to conventional CSI, allows to strongly reduce ground leakage current, phase current THD and semicondutor power losses, at the price of an additional power device.

Keywords: Current source inverter, photo-voltaic power systems, ground leakage current, renewable energy sources

1 Introduction

Photovoltaic (PV) energy has been in the spotlight of academia and industry for more than 10 years. This development had been fueled by the widespread funding of the national and international agencies, in the attempt to reduce the pollutant emissions and reach the target set by the international agreements. Whereas grid-connected PV systems, which used to inject power to the grid, had been economically advantageous thanks to political choices, with the gradual decrease or cancellation of the economic incentives, the PV industry had to adapt to a different context. With an increasing price of the electricity in Europe [1], the interest has shifted to smaller power converters that could contribute to the power supply of a household unit, with the goal of minimizing the energy exchange with the mains. The possibility to perform grid-forming operation also constitute an interesting research topic. This trend pushed researchers to investigate the Smart Home [2] concept, where the residential unit is equipped with distributed energy resource (typically PV), storage and smart appliances.

In this framework, low-power photovoltaic converters are extremely interesting; targets are high efficiency and high voltage transfer ratio. These requirements imply the use of transformer-less topologies, preferably single-stage, to reduce the number of energy conversions. The vast majority of power electronics interfaces for PV are voltage source inverters (VSI), thanks to the wide adoption in the electric drives industry and their good efficiency when the DC supply level is high enough. Current source inverter (CSI) topologies are based on a different concept, where the DC link is constituted by an inductor and the devices are used to modulate the DC current directly to the load. The need of the DC current control and of reverse-blocking semiconductor devices has limited the diffusion of these kinds of converter. For small-medium PV installation, however, the CSI concept has the advantages of intrinsic voltage boost capability. A fair comparison of VSI and different CSI were evaluated in Ref. [3]. Efficiency and ground leakage current still constitute a major issue [4-5].

A particular three-phase VSI topology, called H8 [6], in-troduces a decoupling between AC side and DC side adding additional devices and with the use a dedicated Space Vector Modulation. This solution allows in particular to cancel the common-mode Voltage

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variation for a significant range of modulation index. For classic transformerless three-phase VSI, the active common-noise canceler can be used to reduce the common-mode voltage variations [7].

This paper thoroughly analyzes the original CSI topology and the modified CSI7 or H7 topologies [8-10] from the point of view of mainly ground leakage current, but also power quality and semiconductor power losses. Some solutions of single-phase current source inverters are able to reduce the conduction losses during the zero-vector [11] and thanks to two additional switches, it is also possible to reduce the ground leakage current [12].

Because the common-mode voltage of a CSI depends on the instantaneous current, a novel definition is here applied to perform a better comparison between the architectures. The analysis is carried out in case of two different space vector modulations (SVMs) and different number of PV panels. Numerical simulations results are compared in terms of ground leakage current and THD of the injected grid currents. The paper is organized as follows: Section 2 presents the different CSI topologies that will be compared and the associated SVMs; Section 3 reports the simulation results for the different solutions in Matlab/Simulink environment; Section 4 shows the experimental results and Section 5 draws the conclusions.

2 Topology comparison

Two topologies will be analyzed: the three-phase current source inverter (CSI), Fig. 1 and the CSI7 [8] topology, Fig. 2. The key idea is that an additional switch is used to provide the zero state, reducing the number of series-connected devices and hence the conduction losses. Because the assumption is made that a low-power PV inverter has to process only a limited amount of reactive power, no series diode is

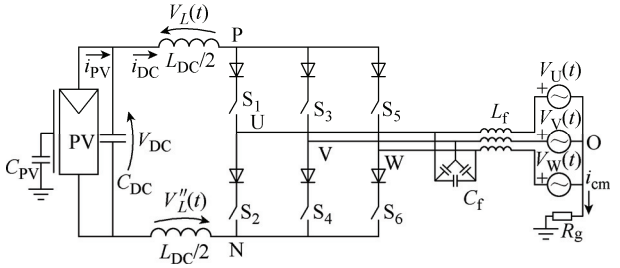


Fig. 1 Schematic of traditional CSI topology

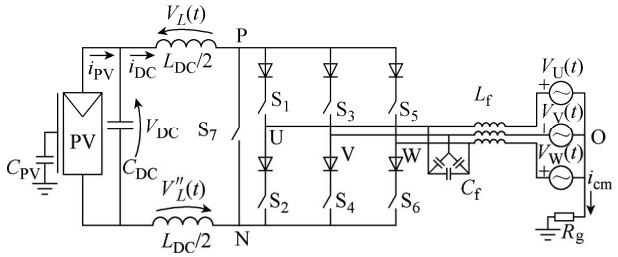


Fig. 2 Schematic of CSI7 topology

used for the additional switch, i.e., the drain-source voltage during the zero state is never reversed.

The converters are controlled with a space vector modulation (SVM). Among the nine admissible states, six are active vectors and three are zero vectors (i.e., DC link short circuit). In the CSI7 SVM the zero vector generation is always implemented by the switch on of only the additional switch S_7. Whereas in a VSI topology dead-times need to be added to the commutation sequence to prevent the DC capacitor short-circuit, in a CSI an overlap time, t_{ov}, must be added to prevent the DC inductor open-circuit, with consequent voltage spikes. This overlap time, if not compensated, causes a marked distortion in the output current, see Ref. [8].

A further degree of freedom of the SVM is the sequence with which the states are generated. In this paper two possibilities are analyzed, the base sequence and the advanced alternated sequence, see Fig. 3. In this figure, t_a and t_b represent the dwell time intervals for the application of the two active vectors (curent vectors ***A*** and ***B***) and t_0 the time interval for the application of the zero vector in a switching period T_S. The alternated SVM sequence must be customized depending on the odd/even sextant type and a specific transition sequence must be implemented to avoid resonance excitation of the output filter [8]. Dwell times are calculated according to the SVM. Because the

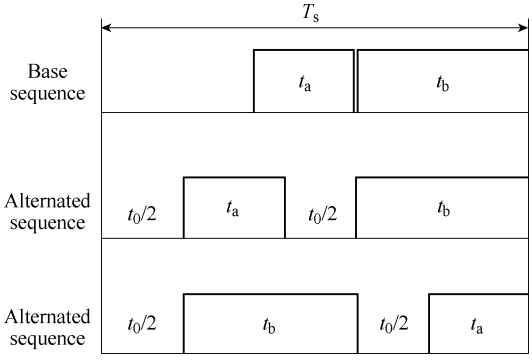


Fig. 3 Comparison of the commutation sequences

alternated sequence implies a reduced current THD, in order to realize a fair comparison, the following analysis assumes a double switching frequency for the base sequence.

Thanks to the overlapping time of implemented alternate SVM, the additional switch S_7 is switched on while the full-bridge is still generating an active vector. This operation draws the DC current to S_7, releasing the full-bridge switches, whose current goes to zero. When these switches are turned off at the end of the overlapping time, S_7 is already carrying the whole DC current, so they are switched off with zero current switching. In the case of base SVM this does not happen for the turn-off of one transistor (S_1~S_6) during the transition from current vector ***A*** to current vector ***B***.

The ground leakage current in PV systems is mainly caused by the frame-to-earth parasitic capacitance of the PV panels and the common-mode voltage variation introduced by the power converter operation [13].

For CSI topologies shown in Fig. 1, the common-mode voltage, v_{cm}, will be assessed, see Fig. 4. According to Refs. [14-15] on CSI, the v_{cm} can be computed using the star connection of the three-phase grid voltage as voltage reference, resulting in

$$v_{cm}=\frac{V_{P0}+V_{N0}}{2} \tag{1}$$

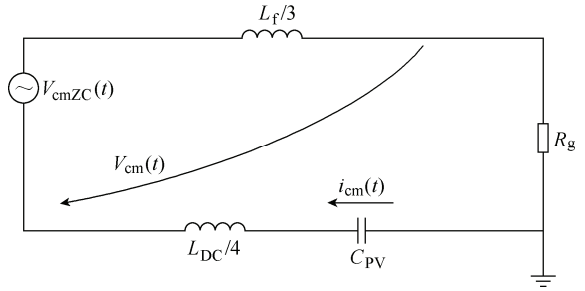


Fig. 4 Commom-mode circuit in case of CSI with split DC input inductor

For a CSI topology, the common-mode voltage is not independent from the common-mode current (as it is the case in VSI). If formula (1) is adopted, i_{cm} perturbs v_{cm} because it is also flowing through the output filter inductor L_f. The non-uniqueness of the common-mode voltage definition causes problems in the analysis, making it difficult to compare different solutions. For this reason, a novel definition of common-mode voltage is hereby adopted, to make the analysis of the CSI ground leakage current similar to the VSI one. In the following v_{cmZC} identifies the v_{cm} signal with a null common-mode current i_{cm}, i.e. with a zero C_{PV}.

The two topologies CSI and CSI7 differ in the common-mode voltage generation, because in the case of CSI7 the zero vector is obtained by switching off all the full-bridge devices while S_7 is on, whereas for the CSI one leg is used to implement the DC link short-circuit as shown in Fig. 5. The complete decoupling between the grid voltage and the DC input is what allows for the superior performance of the CSI7. Altough the CSI topology is also reported with a single inductor in the DC link, because of the poor performance [16] of this solution, only the split-inductors version is considered in this work.

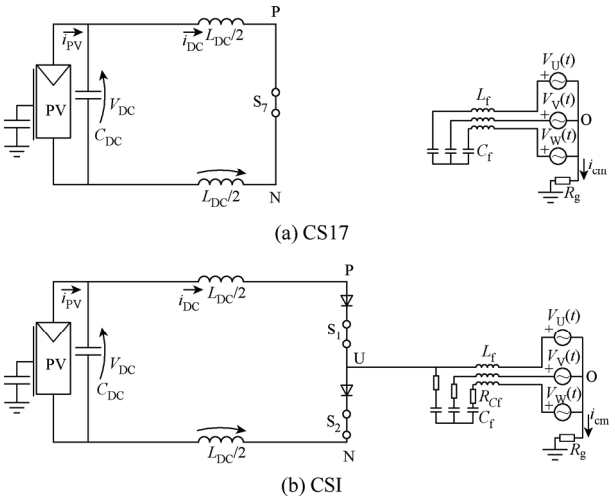


Fig. 5 Equivalent circuit under zero vector

The components present in the equivalent common-mode circuit in case of classic CSI, shown in Fig. 4, are the equivalent PV parasitic capacitance C_{PV}, 1/3 of the inductive part of the output filter, 1/4 of the total DC input inductance L_{DC} and the ground resistance R_g.

The additional common-mode filter inductor on the line side, typically added for EMC issues, results in series with L_f /3. Adopting a split input inductor is mandatory to reduce the i_{cm}, since with a sole input DC inductor its contribution disappears in the common-mode circuit.

3 Numerical simulations

The two topologies and SVMs were simulated in

Matlab-PLECS environment using the same application circuit detailed in Fig. 6.

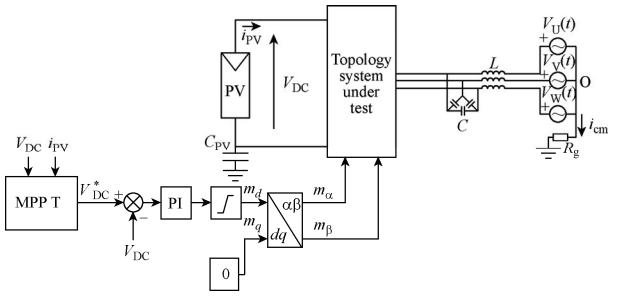


Fig. 6 Test bench for the simulation of different solutions

The PV power source is formed by a varying number of PV modules and the AC side is connected to the grid with a capacitive-inductive filter. Tab. 1 summarizes the parameters of the SHARP ND-RC250 PV module: a worst case scenario of 100 nF/kWp (as indicated in technical information of SMA [17]) was considered for the equivalent parasitic capacitance C_{PV} , resulting in a value of 25 nF for each module.

Tab. 1 Nameplate data of the PV module used in simulations

Name	Value
V_{mpp}/V	30.3
I_{mpp}/A	8.24
$C_{PV_{single\text{-}panel}}$/nF	25

The simulations were carried out with strings of 2, 4, 6 and 8 PV modules in MPP operation and consequently with different values of equivalent PV parasitic capacitance and PV power source, see Tab. 2.

Tab. 2 Summary of PV source scenarios

Numbers of PV modules	P_{DC}/W	V_{mppt}/V	C_{PV}/nF
2	500	60.6	50
4	1 000	121.2	100
6	1 500	181.8	150
8	2 000	242.4	200

The classic maximum power point tracker (MPPT) and the input voltage control with a PI regulator were adopted. No current control is mandatory, as the injected grid current is directly controlled via the duty cycle, see Ref. [8]. For the sake of simplicity the modulation index m_q was imposed equal to zero: doing so, a small reactive power can flow, determined by the CL filter supplied by the grid. The park transformation dq-αβ obtained with the measure of the angle of grid voltage vector determines the input of SVM.

The performance comparison was carried out with two topologies and two different SVM modulations:

(1) Traditional CSI with base SVM.

(2) Traditional CSI with alternated SVM.

(3) CSI7 with base SVM.

(4) CSI7 with alternated SVM.

In order to perform a fair comparison between base and alternated SVMs, the switching period T_s in case of base SVM is halved with respect to alternated SVM one, $T_{S\text{-}basePWM}$ = 33.33 μs and $T_{S\text{-}altPWM}$ = 66.67 μs. Tab. 3 shows all the other parameters.

Tab. 3 Simulation and experimental parameters

Name	Value
L_{DC}/mH	2
$T_{S\text{-}BasePWM}$/μs	33.33
$T_{S\text{-}AltPWM}$/μs	66.67
T_{ov}/μs	1
V_{grid} (line-to-line)/N	400
F_{grid}/Hz	50
L_{f*}/mH	1.4
C_f/μF	1.5
R_g/Ω	4.7

In this way, the number of hard switching commutations (per unit of time) of the seventh switch S_7 results the same along with the ripple at switching frequency of the injected grid current [8,16]. In the same works it is possible to see that, in case of CSI7 topology with alternated SVM, the other switches commutate in zero current switching (ZCS).

In order to set the resonance frequency of the equivalent common-mode circuit of Fig. 4 to be always lower than the minimum switching frequency, i.e. $f_{S\text{-}altPWM}$=15 kHz, a three-phase AC common-mode inductance was added to all solutions simulated. In actual application a common-mode filter is always used also for EMC issues.

Since a smaller C_{PV} value determines an higher resonance frequency, it was considered a minimum value of C_{PV}, often determined by additional filters added in the power converter for EMI problems, equal to 10 nF. Considering this value, it was chosen L_{cm} = 3×20 mH to obtain a resonance frequency still lower to $f_{S-altPWM}$ = 15 kHz. In this scenario the resonance of frequency response i_{cm} (jω) results equal to 11 kHz, see Fig. 7.

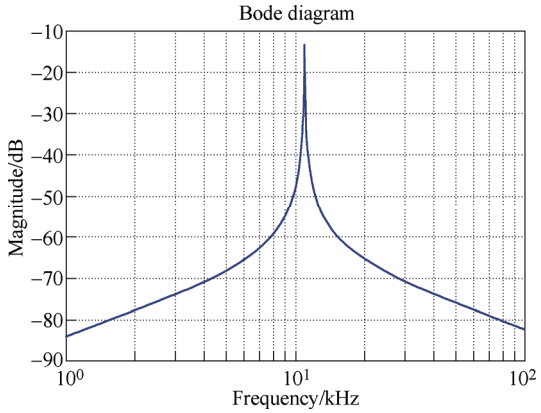


Fig. 7 Bode diagram of $i_{cm}(j\omega)$ in case of $C_{PV} = 10$ nF and $L_{cm} = 3 \times 20$ mH

At first, the performance comparison was carried out with the use of a PV source formed by 4 PV modules. Waveforms of v_{cmZC}, injected phase current, and i_{cm} and their FFT are shown.

In case of CSI7 topology with alternated SVM, when the zero vector is applied, devices $S_1 \sim S_6$ are in off-state. As a consequence, there is no connection between the DC link and the grid. Considering real devices, various parasitic capacitances are associated with e.g. Mosfet output capacitance C_{oss}, diode junction capacitance C_j and stray PCB capacitance. The value of v_{cmZC} during null state is affected by the aforementioned capacitance and the instantaneous values of grid voltage.

Fig. 8 describes the two extreme cases of V_{cmZC} values during the zero vector application, i.e. during $t_Z/2$.

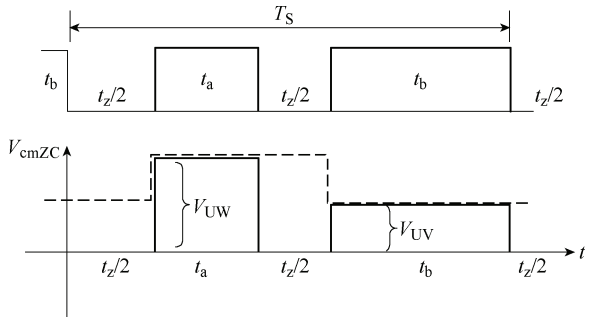


Fig. 8 Different V_{cmZC} transients in CSI7 topology with alternated SVM during zero active vector times t_Z

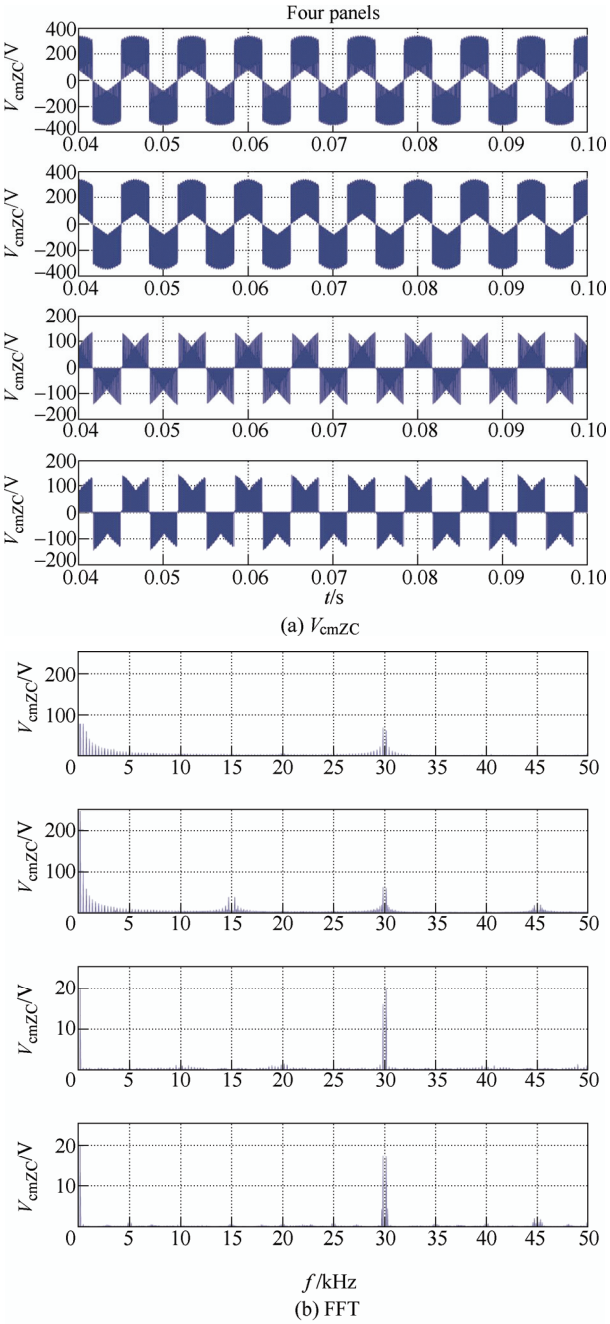
Two cases are possible:

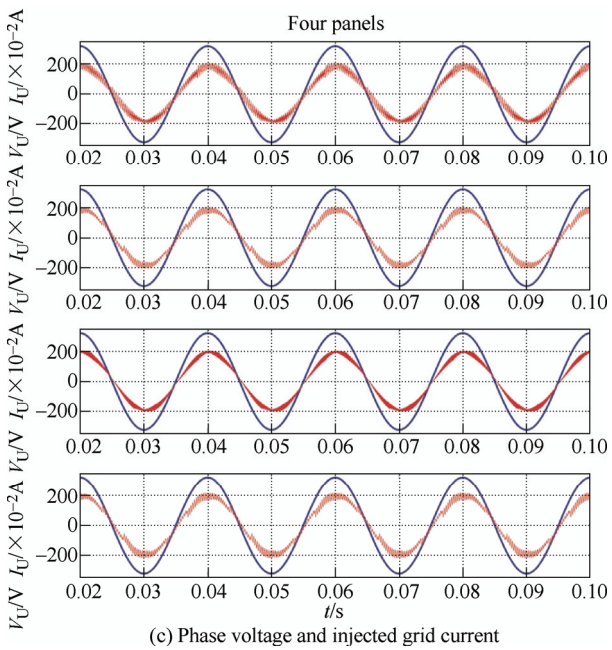
(1) V_{cmZC} remains unchanged to the previous instantaneous value during the application of an active vector.

(2) V_{cmZC} reach zero value (in case of negligible parasitic capacitance).

In the present work, simulations of the CSI7 topology were carried out assuming the latter condition (negligible parasitic capacitance). In actual applications, this is related to a low value of output capacitance of the power semiconductors. In this case, the main harmonic content of V_{cmZC} is located at $2/T_S$. In the first scenario (not considered in simulations) a lower harmonic content would be present and the main harmonic content would be located at $1/T_S$. A detailed analysis of this behaviour is beyond the scope of the present paper.

Fig. 9a shows the V_{cmZC} waveforms in the four scenarios with null C_{PV} value, whereas Fig. 9b shows their spectra. It is possible to see the lower harmonic



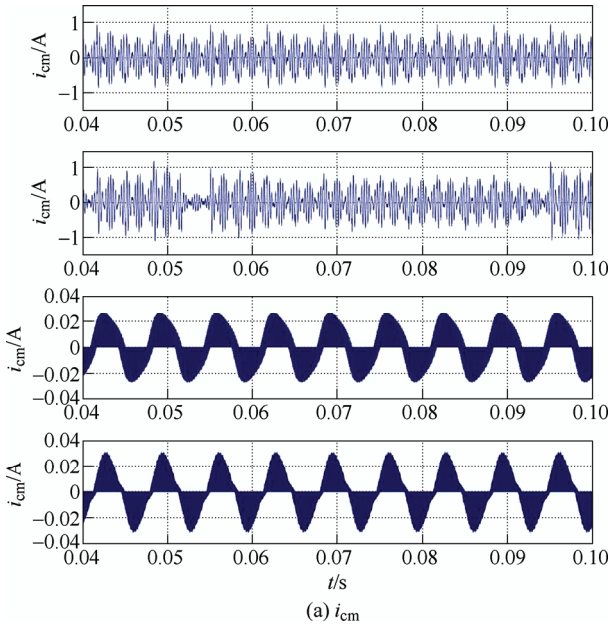


(c) Phase voltage and injected grid current

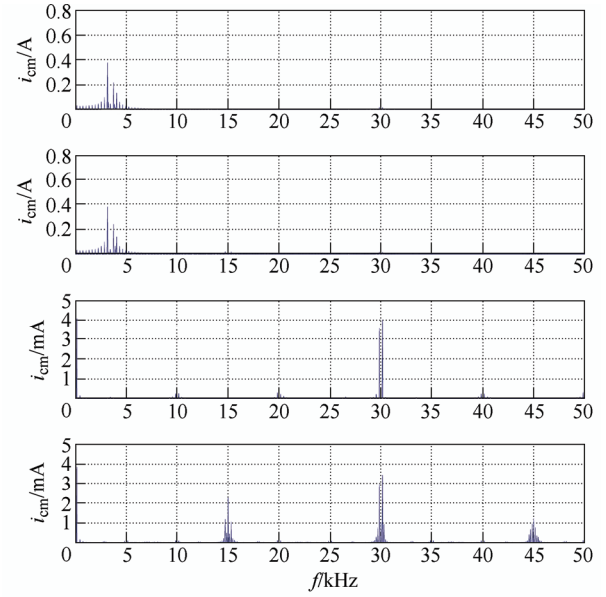
Fig. 9 Simulation waveforms in the four scenarios with 4 PV modules with null C_{PV}

content of v_{cmZC} in case of CSI7 topology, both with base and alternated SVMs. Under the same operating conditions, Fig. 9c shows the injected grid current in the four scenarios. From Figs. 8 and 11, it is possible to see as the minimum THD of the injected grid current is present in the case of CSI7 topology with alternated SVM, see Ref. [8].

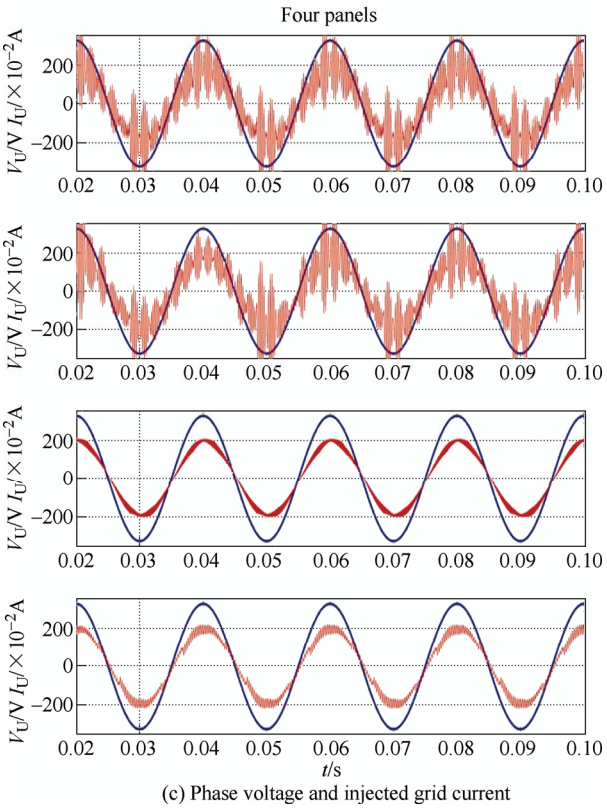
Fig. 10a and 10b show the effect of C_{PV} in case of four PV modules. It is possible to see a high values of i_{cm} in case of traditional CSI topology, which determines an unacceptable THD for the injected grid current in Fig. 10c. Fig. 10b shows the spectra of i_{cm}.



(a) i_{cm}



(b) FFT



(c) Phase voltage and injected grid current

Fig. 10 Simulation waveforms in the four scenarios with 4 PV modules with C_{PV}=100 nF

As expected in the case of CSI topology, a significant harmonic content is present also at low frequencies in the spectra of v_{cmZC}.

The histograms of Figs. 11 and 12 show the THD of the injected grid current in the four scenarios with and without C_{PV}, in case of varying number of PV panels. Tab. 4 highlights a negligible increase of the THD due to C_{PV} in case of CSI7 topology with alternated SVM.

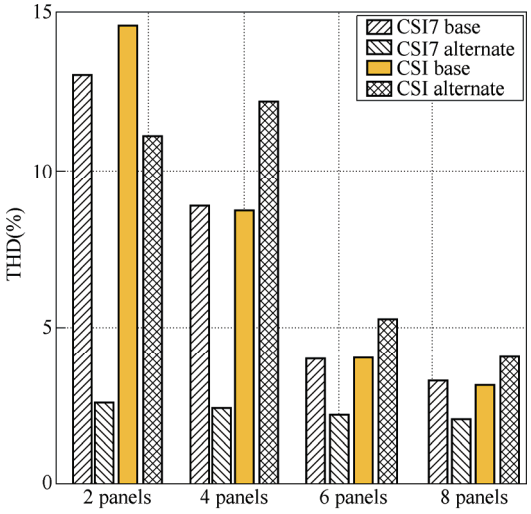


Fig. 11 THD of the injected grid current with a null C_{PV} in four scenarios and different numbers of PV modules

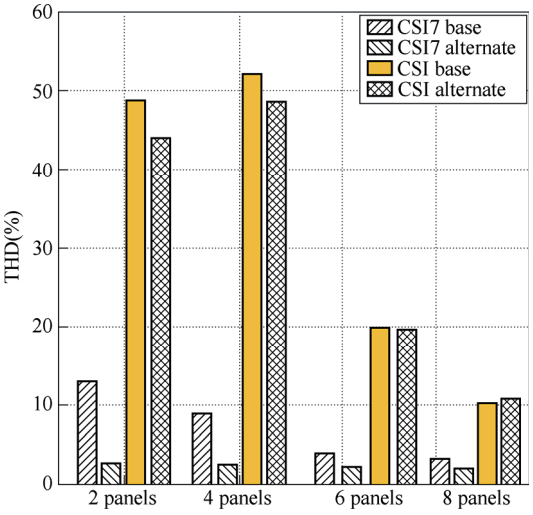


Fig. 12 THD of the injected grid current with C_{PV} in four scenarios and different numbers of PV modules

Tab. 4 THD of the injected grid current in case of CSI7 with alternated SVM

THD (%)	2 modules	4 modules	6 modules	8 modules
Null C_{PV}	2.616 2	2.436 7	2.201 4	2.066 3
With C_{PV}	2.618 8	2.444 3	2.218 6	2.086 6

Fig. 13 summarizes the evolution of RMS values of i_{cm} in the four scenarios and with a different number of PV modules.

Comparing Figs. 12 and 13, it is possible to appreciate the very low values of i_{cm} also in case of CSI7 topology with base SVM despite the higher THD of the injected current.

The last set of simulations were carried out in order to compare semiconductor power losses in the four scenarios separating switching and conduction losses for the six switches of the main full-bridge and

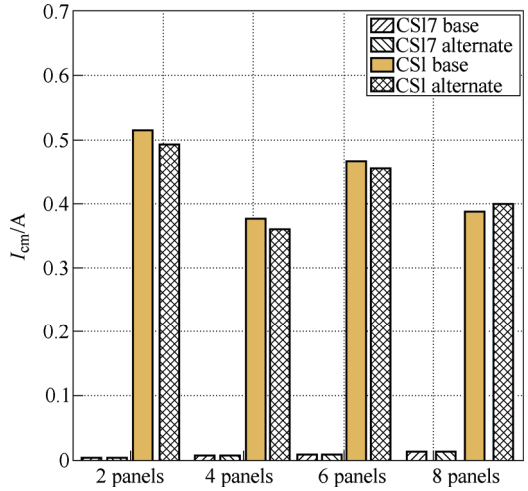


Fig. 13 RMS value of i_{cm} with different numbers of PV modules

for the additional S_7 switch present in CSI7 topology. This information allows for a proper selection of power switches tailored for the particular topology.

The semiconductor power losses were computed with the support of PLECS thermal models. For the sake of simplicity, the same power switches and diodes were chosen for the four scenarios: IGBT 1 200 V/15 A (IGW15N120H3) and diode 1 200 V/30 A (RHRG30120).

Figs. 14 and 15 show respectively the evolution of semi-conductor conduction and switching power losses for every power switch S_x of the main full-bridge and for the additional S_7, if present. From these figures, it is important to highlight that, in case of CSI7 with alternated SVM, the switching power losses of every S_x transistor of the main bridge are almost zero thanks to ZCS commutations, and are independent of the number of PV modules. All the switching power losses are concentrated on the seventh switch in CSI7 topology with altenated SVM: for this reason the use of a Silicon Carbide device for S_7 is advantageous in terms of power losses reduction [9, 18]. Concerning conduction power losses in traditional CSI topology, as expected there is no difference in power losses by varying the number of PV modules in the input string. In case of CSI7 topology, there is a decrease of losses on S_7 when the number of PV modules increases: however the concurrent losses increase on S_x devices reduces the impact of S_7 on conduction power losses reduction.

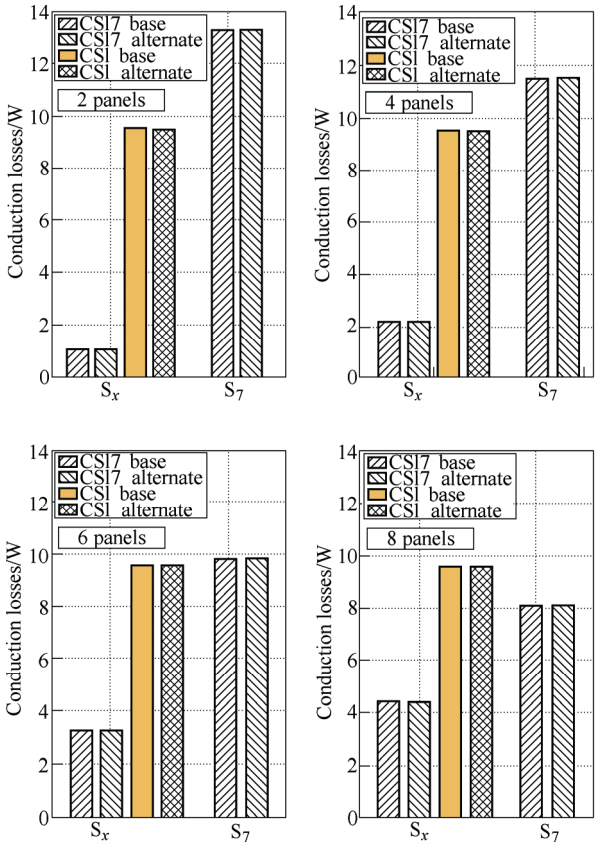


Fig. 14 Semiconductor conduction losse (S_x represents the losses of a single switch of the main full-bridge)

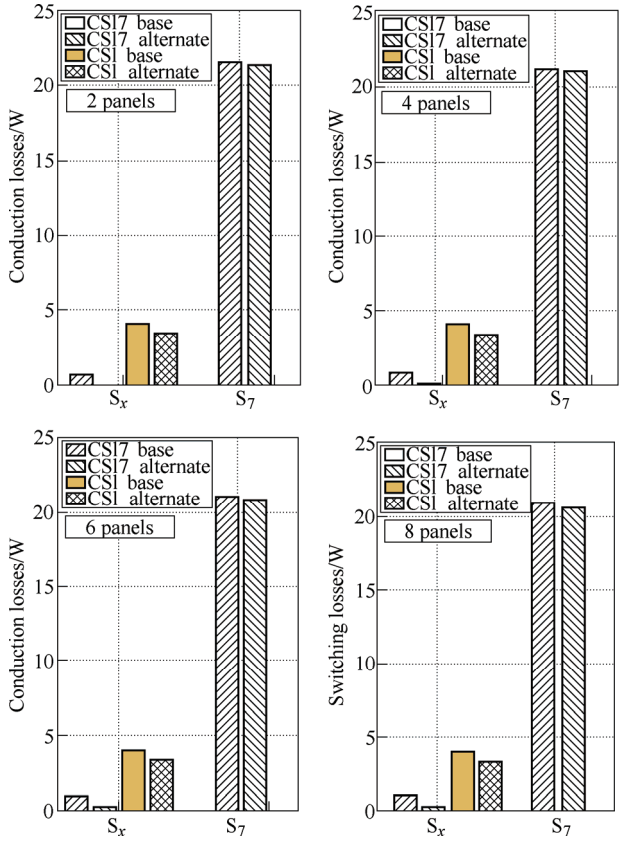


Fig. 15 Semiconductor switching power losses in the four scenarios and with a different number of PV modules

Fig. 16 compares the total semiconductor power losses in the four scenarios with different number of PV modules. Even employing the same Si devices for all the transistors, the total power losses are nonetheless lower in the case of CSI7 topology with alternated SVM due to the application of the zero vector with the seventh switch, allowing ZCS for the other S_x transistors.

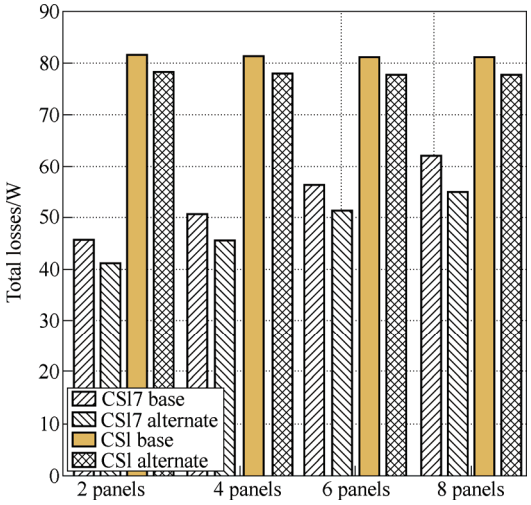


Fig. 16 Total semiconductor power losses in the four scenarios and with a different number of PV modules

4 Experimental validation

The experimental validation was carried out with the prototype power converter shown in Fig. 17, according to the operating parameters summarized in Tab. 3. Input DC voltage was set equal to V_{DC}=120 V with a C_{PV}=100 nF corresponding to the presence of 4 PV modules. Instead of grid tied operation, the experiments were carried out in island operation, with the use of a balanced resistive load (3 R_L=252 Ω). For this reason the phase injected grid current results equal to 0.91 A(RMS) in order to obtain a three-phase output voltage equal to V_{grid} (line-to-line)= 400 V(RMS) . The additional common-mode inductor L_{CM} was not added. Only the two most significant scenarios were experimentally evaluated: traditional CSI topology with base SVM and CSI7 topology with alternated SVM. The goal of the experimental validation is related to the ground leakage analysis between these two solutions. Because of this reason, the THD of the injected grid current is not evaluated, as the difference between the grid impedance and the resistor load would make the comparison not representative of the actual condition.

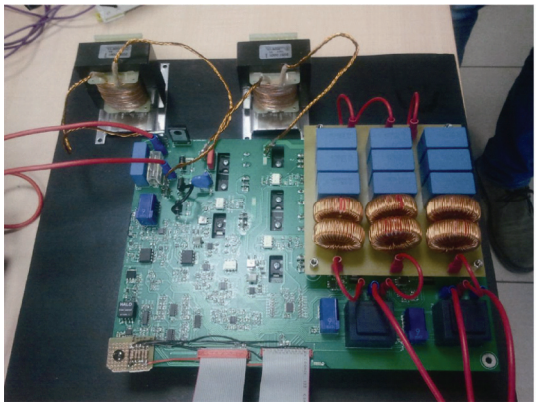


Fig. 17 CSI7 power converter prototype

Figs. 18 and 19 show the injected grid current, V_{cmZC} and its spectrum with a null C_{PV} in case of CSI with base SVM. Figs. 20 and 21 the same quantities in case of CSI7 with alternated SVM. For CSI7 topology with alternated SVM, when comparing these figures against simulation results, the main difference is the harmonic content of V_{cmZC}. As explained in the simulation section (see Fig. 10), because of output capacitance of the power devices employed in the prototype the v_{cmZC} value during the application of the zero vector remain similar to the last voltage value imposed by the previous active vector. As a result the first switching harmonics encountered are not grouped around 30 kHz (switching frequency of the S_7) but around 15 kHz. Fig. 22 shows a magnified view of V_{cmZC} during a T_S, demonstrating the effect described. A thorough study of the influence of these parasitic capacitance on CSI7 topology is beyond the scope of the present paper.

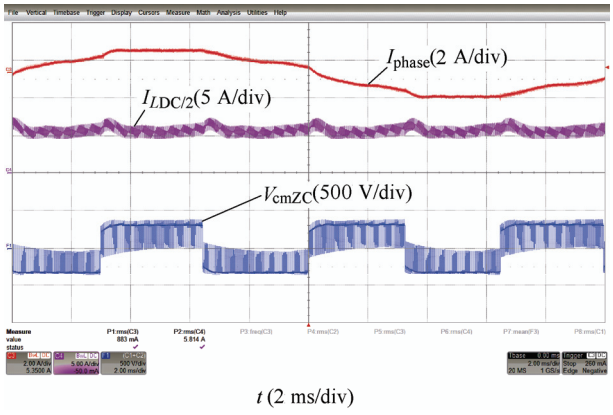


Fig. 18 CSI topology with base SVM with a null C_{PV}

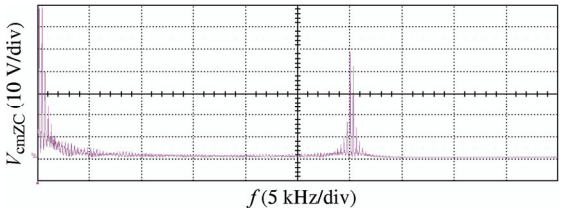


Fig. 19 CSI topology withbase SVM with a null C_{PV}

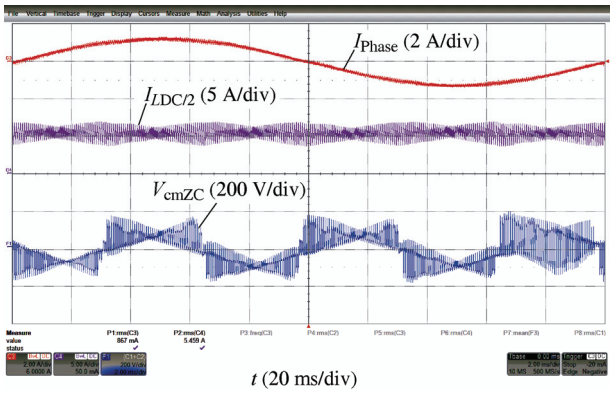


Fig. 20 CSI7 topology with alternated SVM with a null C_{PV}

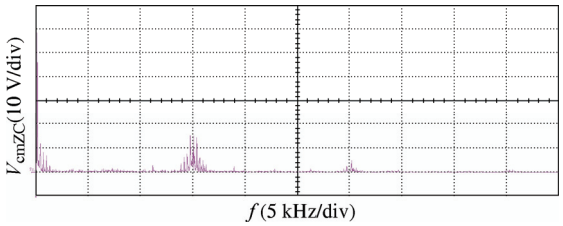


Fig. 21 CSI7 topology with alternated SVM with a null C_{PV}

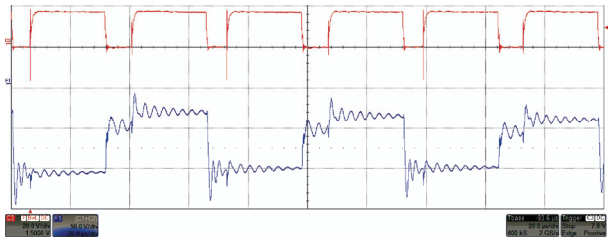


Fig. 22 Enlarged view of v_{cmZC} waveform during a T_S

Figs. 23 and 24 show the injected phase current, the i_{cm} waveform and its spectrum in case of CSI topology with base SVM . Figs. 25 and 26 show the same quantities in case of CSI7 topology with alternated SVM. The RMS of i_{cm} resulted equal to 22.53 mA in case of CSI7 topology with alternated SVM while in case of CSI topology with base SVM resulted equal to 251 mA. Looking at Fig. 23, it is possible to notice that the i_{cm} waveform is distorting the injected phase current.

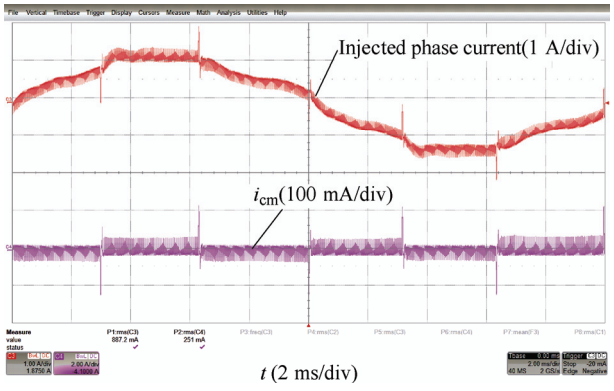


Fig. 23 CSI topology with Base SVM

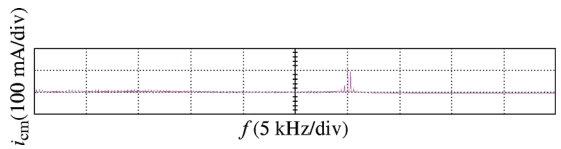


Fig. 24 CSI topology with Base SVM Spectrum of i_{cm}

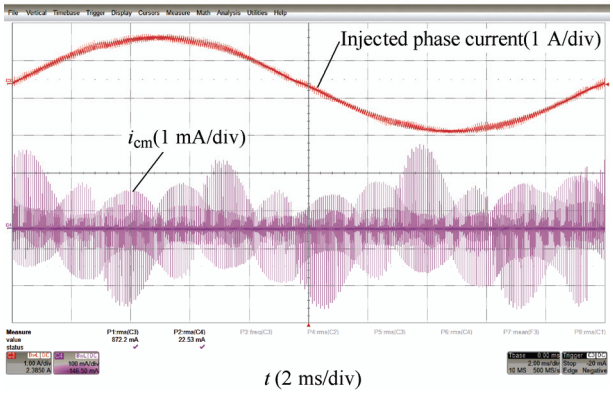


Fig. 25 CSI7 topology with alternated SVM

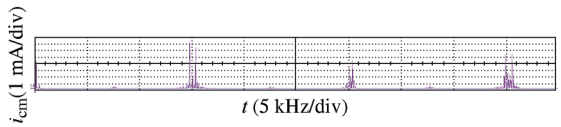


Fig. 26 CSI7 topology with alternated SVM

Figs. 27 and 28 show the voltage waveform (v_{CPV}) across the equivalent parasitic capacitance C_{PV} in the two topologies. The results confirm the higher harmonic content of V_{CPV} in case of traditional CSI + base SVM that determined higher i_{cm} RMS and harmonic content.

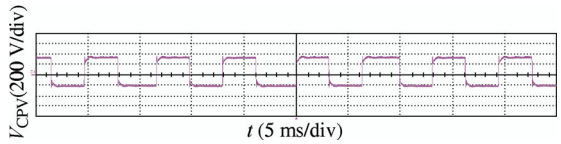


Fig. 27 V_{CPV} waveform in case of CSI and base SVM

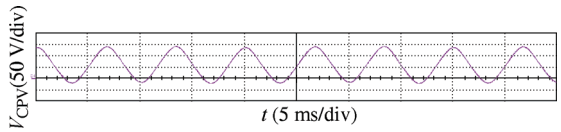


Fig. 28 V_{CPV} waveform in case of CSI7 with alternated SVM

5 Conclusions

This paper thoroughly analyzed two grid-connected current source inverter topologies: traditional CSI with base SVM and CSI7 with alternated SVM. The modified topology CSI7 reduces the semiconductor power losses and THD of the injected phase currents, as already shown in previous literature. In the present work the two CSI topologies were compared against each other in terms of ground leakage current (i.e. common-mode current) considering a varying number of PV modules. Other figures of merit adopted for the sake of comparison include the THD of the injected phase currents, with and without the parasitic capacitance C_{PV}, and the switching and conduction semiconductor power losses for every transistor. The most notable results of this comparison are:

(1) The CSI7 topology, when compared against traditional CSI topology, is able to strongly reduce the RMS of i_{cm} both in case of base SVM and alternated SVM.

(2) The CSI7 topology is highly robust to the capacitance variation of the photovoltaic panels.

(3) The CSI7 topology with alternated SVM with respect to the same topology with base SVM presents a lower THD of the injected phase currents.

(4) The CSI7 topology with alternated SVM with respect to the same topology with base SVM presents lower switching semiconductor power losses and all the switching power losses are concentrated in the seventh switch S_7.

In conclusion, CSI7 topology demonstrated lower losses and insensitivity of the ground leakage current versus the number of PV modules adopted. Hence CSI7 with alternated SVM outperforms the CSI in all areas, and it can represent the ideal solution for small grid-tied systems characterized by high voltage transfer ratio.

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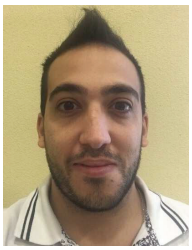

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