Two-Stage Transformerless Dual-Buck PV Grid-Connected Inverters with High Efficiency

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Abstract: A semi-two-stage common-ground-type transformerless dual-buck-based grid-connected inverter is proposed in this paper. The common-ground-type topology can eliminate common mode (CM) leakage current by connecting the negative terminal of the photovoltaic(PV) directly to the neutral point of the grid, which bypasses the PV array's stray capacitance. The dual-buck-based topology guarantees increased robustness since the dc-link cannot be short-circuited by a shoot-through event. The semi-two-stage topology features multi-level characteristic, which has a lower forward-voltage drop and smaller d*v*/d*t*. Compared with the conventional two-stage inverter, the proposed topology achieves higher efficiency and higher reliability. Experimental results of a 1.5kW prototype show that the proposed inverter is able to achieve high efficiency and low leakage currents.

Keywords: Common mode current, photovoltaic, semi-two-stage inverter, transformerless inverter, common-ground-type inverter.

1 Introduction

Since the energy crisis and environmental pollution problem is becoming increasingly serious, solar energy, wind energy, fuel cell and other new energy power generation technologies have been paid more attention to [1-3]. For residential PV generation grid-tied systems, because of the *I-V* characteristic of PV arrays, the input voltage of a residential PV inverter may vary in a wide range, such as 200~500V. As a result, two-stage PV grid-tied inverters, which are characterized by step-up and step-down functions, are widely used. As the key part of the PV grid-tied inverter system, it is important to improve the efficiency of the grid-tied inverters[4-6].

For conventional two-stage transformerless photovoltaic grid-tied inverters, all the output power of PV arrays needs to be boosted by a front-end DC-DC converter and feed to the utility grid by a grid-tied inverter. Therefore, all the output power of PV arrays is two-stage high-frequency transferred, which makes this kind of circuit difficult to be highly efficient[7-9]. With the purpose of reducing leakage current and improving the power conversion efficiency, many solutions have been proposed. Common-ground-type PV inverter, i.e. doubly ground inverter can effectively reduce the leakage of the PV system and has attracted a lot of interest from both academic and industry, as shown in Fig.1. The doubly grounded topologies are those where the negative terminal of the PV array is directly connected to the ground[10-13]. Because of the common-ground type structure, the common mode leakage current to the grid is eliminated by connecting the negative terminal of the PV directly to the neutral point of the inverter. The dual-buck inverter can overcome the shoot-through issue of bridge arm without setting dead time[14-16]. Dual-buck structure cells, as shown in Fig.2, with its high reliability, have become a research hotspot of many scholars in recent years[17-22].

Considering these aspects, a novel common-ground-type five-level semi-two-stage dual-buck inverter is investigated in this paper for PV applications. It increases the efficiency and reliability of two-stage grid-connected inverter. The leakage current to the grid is eliminated by connecting the negative terminal of the PV directly to the neutral point of the inverter.

This paper is organized as follows: Section 2presents the operating principles of the proposed inverter. Section 3 analyzes the leakage current model. The operating modes are discussed in detail in Section 4. Simulations and experimental results of the 1.5kW inverter topology are eventually presented in Section 5 for verification, and Section 6 concludes the paper.

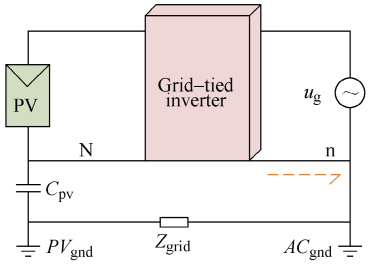
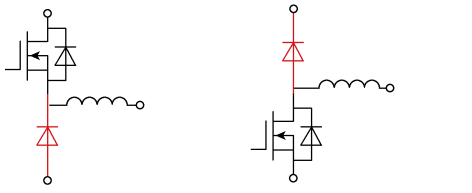


Fig.1 The diagram of common ground inverter



(a) Buck cell (b) Boost cell (inversed buck cell)

Fig.2 Dual-buck structure

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2 The proposed topology and PWM strategy

The proposed topology is a transformerless five-level common-ground-type dual-buck structure inverter. As shown in Fig.3, it utilizes a low voltage branch clamp to realize five discrete output voltages: U_{dc}, U_{pv}, 0, $-U_{pv}$, $-U_{dc}$. In addition, the conduction losses are reduced due to a lower forward-voltage drop, and the switching loss is reduced due to the smaller dv/dt. When the PV array voltage is lower than the grid voltage, energy is transferred by front-end boost. When the PV array voltage is higher than the grid voltage, energy is transferred by the inverter directly. Compared with the conventional two-stage inverter, the proposed topology can realize more efficient transmission and improve the grid-connected efficiency. Besides, with a common ground connection between the negative terminal of the PV panel and the neutral connection of the grid, the leakage current is eliminated, since the parasitic capacitor of the PV array is bypassed.

Fig.4 shows the modulation strategy for the inverter. A conventional modulation approach is used where the switching signals are generated by comparing four modulation waves to a carrier waveform. An interlock delay time between the transitions of S_3 and S_4, at the zero crossings of u_g is required in order to prevent a short circuit of the capacitor C_f during the polarity reversal events of the ac-side voltage u_g. This can be solved by using an algorithm that has a phase locked looped(PLL) providing the ac-side voltage angle and a voltage sensor that measures the voltage. S_1, S_2, S_5 and S_6 are switched in the PWM mode and S_3, S_4 are kept on as a polarity selection switch in the half grid cycle.

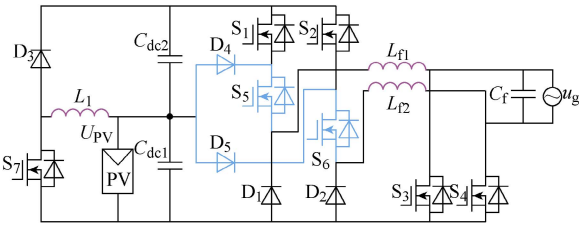


Fig.3 Proposed two-stage transformerless inverter

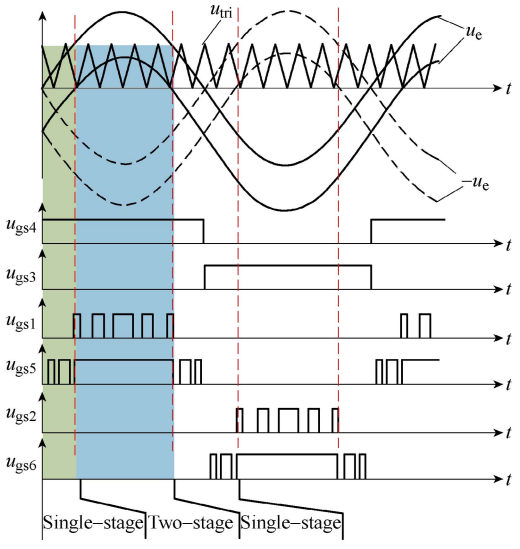


Fig.4 PWM modulation scheme of the proposed topology

3 Leakage current model of the inverter

In the transformerless PV inverter system, a galvanic connection exists between the ground of the grid and the PV array. The PV mental frame is normally grounded[9]. In order to analyze the leakage current of the topology, a model is established.

In the positive half grid cycle, the leakage current model of the common ground converter is shown in Fig.5(a). According to the standard of grid-connection, the ground impedance Z_G is very small. So, the parasitic capacitance C_{PV} between the negative point of PV cell and the earth may be seen as short-circuited.

The common mode voltage of the parasitic capacitor can be obtained as

$$u_{CM} = \frac{u_{Pn} + u_{Nn}}{2} \tag{1}$$

Where P and N are the positive and negative terminals of PV array respectively, and n is the negative terminal of AC side. It can be seen in the Fig.5(a) that the u_{Pn}=U_{PV} and u_{Nn}=0. Therefore, the expression of common mode voltage of the common-ground-type inverter can be deduced as

$$u_{CM} = \frac{U_{PV}}{2} \tag{2}$$

$$i_{CM} = C_{PV}\frac{\mathrm{d}u_{CM}}{\mathrm{d}t} \tag{3}$$

Obviously, u_{CM} is constant and does not contain any high-frequency components. According to the formula (2), (3), it is known that the common-ground-type inverter can almost eliminate the common mode leakage current i_{CM}.

In the negative half grid cycle, the leakage current model of the common ground converter is shown in Fig.5(b). It can be seen that the positive terminal of the AC side is directly connected to the negative point of the PV cell, and the common mode voltage of the parasitic capacitance C_{PV} is equivalent to grid voltage u_g. As shown by the following equation.

$$u_{CM} = u_g \tag{4}$$

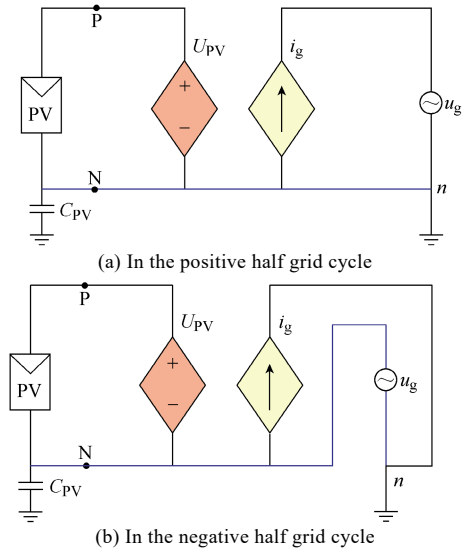


Fig.5 Leakage current model

Due to the low-frequency variation of the grid voltage and no other high-frequency components, the common mode current i_{CM} is very low at this time.

From the aforementioned analysis, the proposed semi-two-stage non-isolated topology features low leakage current.

4 Analysis on the proposed semi-two-stage inverter

4.1 Operation mode analysis

The key waveforms of the proposed topology are shown in Fig.4. In order to avoid the shoot-through problem, the dead time has been set between the drive signals of the switches S_3 and S_4. u_{AN} is the voltage difference between the node A and node N, and u_{BN} is the voltage difference between the node B and node N. Two filter inductors, L_{f1} and L_{f2}, operates at each half cycle of the utility grid alternately.

On the other hand, the semi-two-stage five-level topology operates with unity power factor(UPF). In order to avoid the distortion of inductor current, at the beginning of the positive half cycle of the utility grid, the switches S_1 and S_4 are turned ON at the same time. Similarly, at the beginning of the negative half cycle of the utility grid, the switches S_2, and S_3 are turned ON at the same time. Since the proposed topology is digitally controlled, this modulation method is easy to implement. The control circuit is implemented based on a DSP chip TMS320F2808 from Texas Instruments.

The semi-two-stage topology has six operation modes, which are shown in Fig.6.

4.1.1 State #1 [Refer to Fig.6(a)]

Maximum positive output, $u_{AN}=U_{dc}$. There is no current flowing through the inductor L_{f2}, thus the voltage on the inductor L_{f2} is equal to zero, and $u_{BN}=0$. As a result, $u_{AB}=U_{dc}$. S_1, S_4 and S_5 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig.6(a). The drain-source voltage on S_3 is equal to u_g. During this state, the inductor current i_{Lf1} increases linearly,

$$U_{dc}-u_g=L_{f1}\frac{di_{Lf1}}{dt} \tag{5}$$

4.1.2 State #2 [Refer to Fig.6(b)]

PV cell positive output, $u_{AN}=U_{pv}$. There is no current flowing through the inductor L_{f2}, thus the voltage on the inductor L_{f2} is equal to zero, and $u_{BN}=0$. As a result, $u_{AB}=U_{pv}$. S_4 and S_5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.6(b). The drain-source voltage on S_1 is equal to U_{dc}-U_{pv}, and the reverse blocking voltage on D_1 is equal to U_{pv}. During this state, the inductor current i_{Lf1} decreases linearly when the voltage of the utility grid is higher than $0.5U_{dc}$,

$$U_{pv}-u_g=-L_{f1}\frac{di_{Lf1}}{dt} \tag{6}$$

While the inductor current i_{Lf1} increases linearly when the voltage of the utility grid is lower than U_{pv},

$$U_{pv}-u_g=L_{f1}\frac{di_{Lf1}}{dt} \tag{7}$$

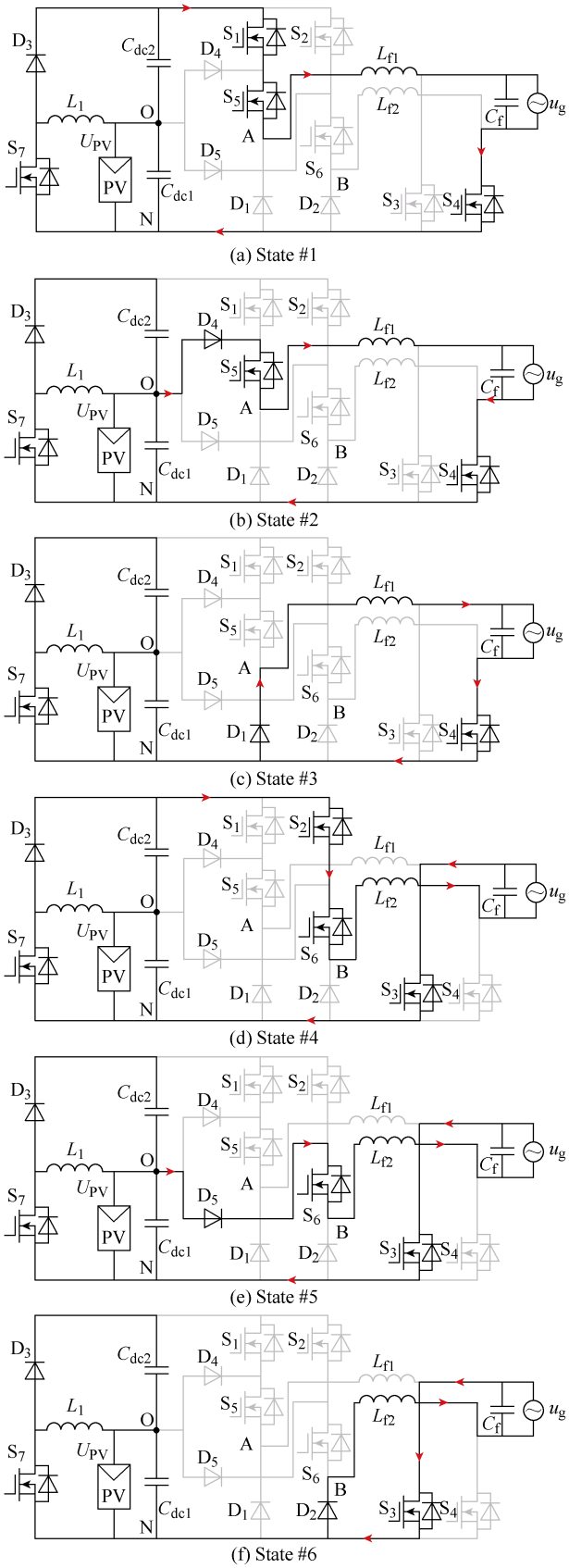


Fig.6 Equivalent circuits of operation mode

4.1.3 State #3 [Refer to Fig.6(c)]

Zero output at the positive half period of the utility grid, u_{AN}=0. There is no current flowing through the inductor L_{f2}, thus the voltage on the inductor L_{f2} is equal to zero, and u_{BN}=0. As a result, u_{AB}=0. S_4 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.6(c). Both the drain-source voltages on S_1 and S_2 are equal to U_{pv}. During this state, the inductor current i_{Lf1} decreases linearly,

$$-u_g = L_{f1}\frac{di_{Lf1}}{dt} \tag{8}$$

4.1.4 State #4 [Refer to Fig.6(d)]

Maximum negative output, u_{BN}=U_{dc}. There is no current flowing through the inductor L_{f1}, thus the voltage on the inductor L_{f1} is equal to zero, and u_{AN}=0. As a result, u_{AB}=$-U_{dc}$. S_2, S_4 and S_3 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.6(d). During this state, the drain-source voltage on S_1 is equal to U_{dc}. In this mode, the inductor current i_{Lf2} decreases linearly,

$$-U_{dc}-u_g = -L_{f2}\frac{di_{Lf2}}{dt} \tag{9}$$

4.1.5 State #5 [Refer to Fig.6(e)]

PV cell negative output, u_{BN}=U_{PV}. There is no current flowing through the inductor L_{f1}, thus the voltage on the inductor L_{f1} is equal to zero, and u_{AN}=0. As a result, u_{AB}=$-U_{pv}$. S_3 and S_6 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.6 (e). The drain-source voltage on S_2 is equal to U_{dc}-U_{pv}, and the reverse blocking voltage on D_2 is equal to U_{pv}. During this state, the inductor current i_{Lf2} decreases linearly when the voltage of the utility grid is lower than U_{pv},

$$-U_{pv}-u_g = -L_{f2}\frac{di_{Lf2}}{dt} \tag{10}$$

While the inductor current i_{Lf2} increases linearly when the voltage of the utility grid is higher than U_{pv}.

$$-U_{pv}-u_g = L_{f2}\frac{di_{Lf2}}{dt} \tag{11}$$

4.1.6 State #6 [Refer to Fig.6(f)]

Zero output at the negative half period of the utility grid, u_{BN}=0. There is no current flowing through the inductor L_{f1}, thus the voltage on the inductor L_{f1} is equal to zero, and u_{AN}=0. As a result, u_{AB}=0. S_3 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.6(f). Both the drain-source voltages on S_2 and S_1 are equal to U_{dc}. During this state, the inductor current i_{Lf2} increases linearly,

$$-u_g = L_{f2}\frac{di_{Lf2}}{dt} \tag{12}$$

From the above operation mode analysis, there is no current flowing through the body diodes of the switches. Therefore, the proposed semi-two-stage topology is free of reverse recovery problem in the freewheeling mode, and the MOSFETs with low on-resistances can be used to replace IGBTs. In addition, the voltage jump of each high-frequency switch in the proposed topology is nearly half of the input voltage. Therefore, the switching loss of the proposed topology is much lower than that of the three-level topology.

4.2 Analysis of voltage stress

The maximum drain-source voltages on the switches, S_1, S_2, S_3 and S_4, are equal to U_{dc}. The maximum reverse blocking voltages on the diodes, D_1 and D_2, are equal to U_{PV}. The maximum drain-source voltages on the switches, S_5 and S_6, are equal to U_{pv}. On the whole, part of the devices bear low voltage stress.

4.3 Control strategy

The semi-two-stage PV grid-connected inverter has two different power conversion processes, and the DC-DC stage and DC-AC can be controlled separately. As shown in Fig.7, the output voltage U_{PV} and output current I_{PV} of the PV panel, in which part of the output current I_{PV} named I_{PV1} flows to the front stage DC/DC converter, the other part of the current I_{PV} named I_{PV2} flows directly to the rear stage inverter. Here, the total current I_{PV} of the PV output and the output voltage U_{PV} of PV array are sampled. The sample results are analyzed by MPPT algorithm to obtain i_{MPPT}. Then, the given reference value of the rear stage current is obtained by proportional-integral(PI) regulator. At this time, the input power of the rear stage is the total output power of the PV array, so that the maximum power of the solar panel flows into the rear stage converter is achieved. The front-end stage directly samples the bus voltage U_{dc}, then it is compared with the reference voltage U_{dcref}, and then processed by the PI regulator. According to the change of sampling parameters, the duty cycle D of Boost circuit is determined, and the bus voltage U_{dc} is controlled. The PV output terminal is directly connected to the grid, and the output voltage is clamped to grid voltage, so the grid-connected current is supposed to keep the same frequency and amplitude with the grid current.

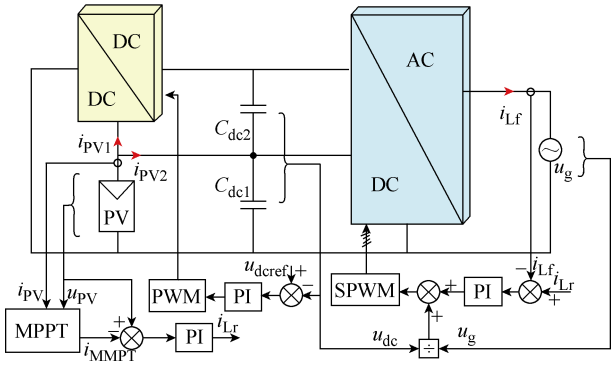


Fig.7 Control block of the proposed topology

The inverter is controlled by a single current loop. The output inductance current is controlled to ensure the topology operates with unity power factor. The reference current i_{Lr}, obtained from the previous maximum power tracking analysis, is compared with the instantaneous value i_{Lf} of the output grid current. The deviation signal is adjusted by the PI regulator.

5 Simulation and experimental results

A prototype of the semi-two-stage dual-buck transformerless PV grid-tied inverter has been built up to verify the feasibility of the proposed inverter. The specifications of the inverter topology are listed in Table 1. The control circuit is implemented based on a DSP chip TMS320F2808. Fig.8 shows the picture of the prototype.

Simulation results of the proposed topology are shown in Fig.9, where u_g and i_g are grid voltage and the grid-tied current respectively. u_{AB} is the voltage of point A to point B.

Table 1 Parameters of the experimental prototype

Parameters	Values
Input PV voltage/V	200~550
Input DC link capacitance/μF	1300
Grid voltage/V	220
Grid frequency/Hz	50
Maximum output power/W	1500
Output filter/mH	3.67
Switching frequency/kHz	20
PV capacitance/nF	100
Digital controller	Texas Instrument's 2808
MOSFET	SPW47N60C3(650V)
DIODE	C3D20060D

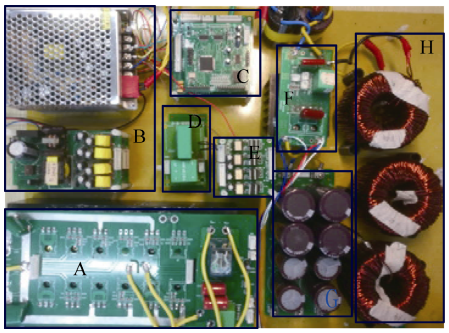
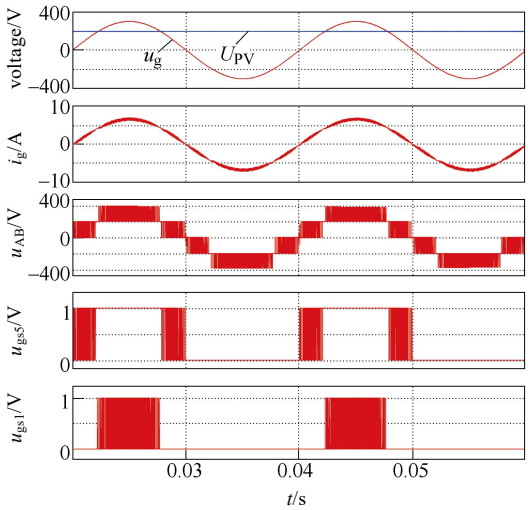
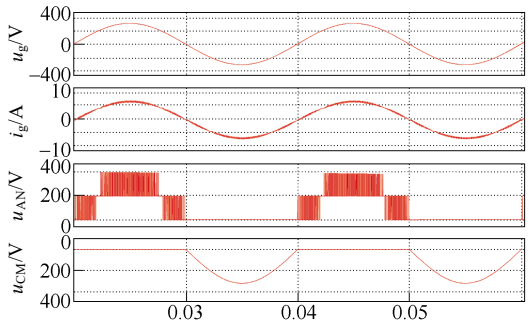


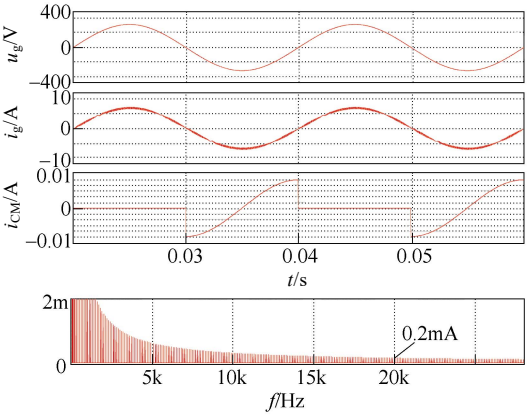
Fig.8 Picture of the prototype(A. inverter, B. auxiliary power, C. controller chip, D. sampling circuit, E. driver, F. boost, G. DC capacitor, H. inductors)



(a) u_{AB}, u_{gs5}, u_{gs1}



(b) u_{AN}, u_{CM}



(c) i_{CM}, FFT of i_{CM}

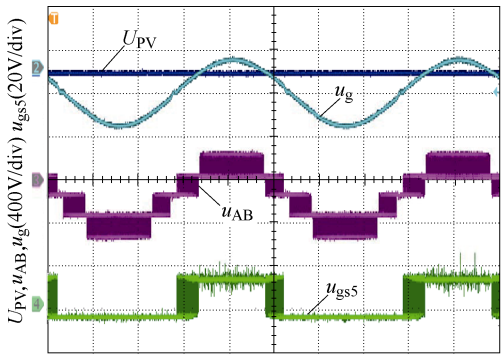
Fig.9 Simulation waveforms of the proposed inverter

From Fig.9(a), it can be seen that the semi-two-stage inverter has five output voltage levels: U_{dc}, U_{pv}, 0, $-U_{pv}$, and $-U_{dc}$. From Fig.9(b), it can be seen that the common mode voltage u_{CM} is consistent with the theoretical analysis. From Fig.9(c), it can be seen that the leakage current at the switch frequency is 0.2mA, which can be ignored.

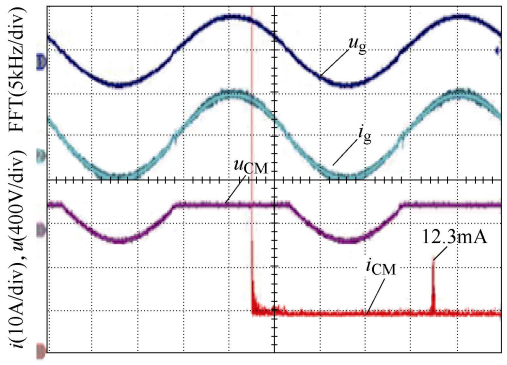
Experimental results of the proposed topology are shown in Fig.10, where u_g and i_g are grid voltage and the grid-tied current respectively. From Fig.10(a), it can be seen that the voltage jump of switches is equal to half of the input voltage. From Fig.10(b), it can be seen that the leakage current at the switch frequency is 12.3mA.

The efficiency of the proposed two-stage dual-buck transformerless PV grid-tied inverter is shown in Fig.11.

From Fig.11, it can be seen that the maximum efficiency of the proposed topology is 97.36%.



(a) u_{AB}



(b) u_{CM}, i_{CM}

Fig.10 Experimental waveforms of the proposed topology

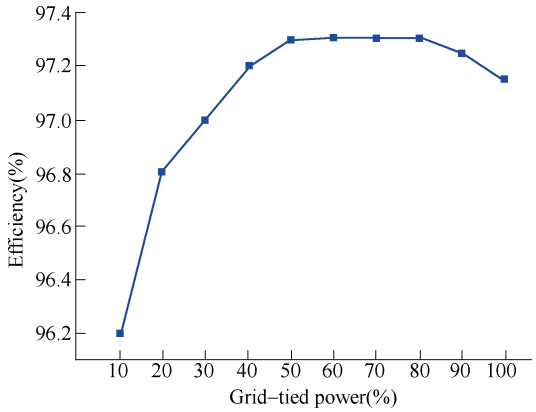


Fig.11 Efficiency of the proposed topology

6 Conclusion

A semi-two-stage five-level transformerless dual buck-based inverter that can be used in grid-connected applications was proposed. Two low-frequency switches are used to connect the negative terminal of the DC-bus to the AC-side terminals directly, which guarantees an ideally non-CM voltage at the switching frequency. Experimental results of a 1.5kW prototype were presented, showing that the proposed inverter features a very low common mode voltage at the switching frequency. Moreover, the dual-buck-based inverter achieved a high efficiency of 97.36%.

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