# Designing an On-board Charger to Efficiently Charge Multiple Electric Vehicles

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**Abstract:** An on-board charger for efficiently charging multiple battery-operated electric vehicles (EVs) is introduced. It has evolved as a single-input dual-output (SIDO) integrated boost-single ended primary inductor converter (SEPIC) fly-back converter, offering cost-effectiveness, reliability, and higher efficiency compared to conventional chargers with equivalent specifications. The proposed system includes an additional regulated output terminal, in addition to an existing terminal for charging the EV battery of a 4-wheeler, which can be used to charge another EV battery, preferably a 2-wheeler. With the aid of control techniques, unity power factor operations are obtained during constant-voltage (CV)/constant-current (CC) charging for the grid-to-vehicle (G2V) operating mode. Using mathematical modelling analysis, the proposed system is developed in a Matlab/Simulink environment, and the results are validated in a real-time simulator using dSPACE-1104. The proposed system is employed for charging the batteries of two EVs with capacities of 400 V, 40 A • h and 48 V, 52 A • h for the 4-wheeler and 2-wheeler, respectively. Its performance is investigated under different operating modes and over a wide range of supply voltage variations to ensure safe and reliable operation of the charger.

**Keywords:** Continuous conduction mode (CCM), CV/CC, electric vehicles (EVs), power factor correction (PFC), single input dual output (SIDO), state of charge (SOC)

## 1 Introduction

The daily demand for electric vehicles (EVs) in the transportation sector has increased in recent years, driven by concerns over fossil fuel scarcity and global warming [1]. Consequently, practice engineers, researchers, and EV manufacturers are faced with numerous challenges and issues that need to be addressed to make EVs a viable and sustainable option for transportation, such as developing a charging infrastructure, cost-effective storage systems, improving efficiency, and creating mobility services with minimum environmental impact [2-3]. The EVs charging system comprises battery packs, power semiconductor devices, passive components, voltage- and current-sensing elements, and an effective controller [4]. Therefore, the role of a charging system is critical for the successful implementation of EV-based transport systems. Moreover, researchers are concerned regarding the development of more reliable and efficient EVs. Thus, it is desirable to develop chargers that can simultaneously charge multiple EVs (2-wheeler and 4-wheeler) batteries from a single-phase main supply. Hence, the objective of this study is to develop a dual-output onboard EV charger embedded in a 4-wheeler that can simultaneously charge a 2 W battery.

The majority of conventional EVs battery chargers utilize front-end diode bridge rectifiers (DBR) that can cause significant current distortion at the supply side [5], resulting in poor power factor at the AC mains. To address this issue, a PFC converter was developed as a front-end active power converter, which utilizes conventional DBR circuits in conjunction with DC-DC converters. Several single-stage AC-DC topologies for power factor improvement have been reported [6-7]. The boost converter is the most widely used topology for PFC applications; however, for a wide range of input voltages, the buck-boost converter presents a more attractive solution. Certain non-inverting buck-boost converters suitable for PFC applications have been proposed [8]. Numerous topologies have

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been previously selected for this application, such as isolated CUK, SEPIC, zeta, and fly-back converters [9]. Unidirectional isolated CUK and SEPIC converters have also been designed in the discontinuous conduction mode (DCM) [10]. With an effective feedback control, the aforementioned isolated converters in DCM mode have been used for LED lighting applications [11]. Thus, an isolated SEPIC converter provides an excellent solution for unidirectional offboard EVs battery chargers.

Power converters with multiple DC outputs can also be used for a wide variety of applications, such as hybrid electric vehicles, stand-by/auxiliary power supplies, and LED drivers [12-14]. In general, to implement a highly efficient system, 2*N* switches are used for *N* multiple outputs, where *N* indicates the quantity [13]. Consequently, proper coordination of the feedback control is required to regulate the multi-output voltages for power flow management in each converter [14]. Compared to separate conventional converters, for a single input, the multiple-output integrated architecture offers fewer switches, that is, (*N*+1) switches for *N* outputs [15]. The cost and complexity of a system can be reduced by using fewer switches. This, in turn, decreases the number of associated drivers required, resulting in lower costs [16-18]. In addition, owing to its integrated architecture, all system outputs are regulated using the same set of switches; therefore, the coordination of feedback control in a multi-output system becomes easier [12].

In multiple-output converters, a high-frequency transformer (HFT) is used to create multiple secondary windings for multiple outputs, and the secondary voltages vary according to the turn ratio. Owing to the magnetic coupling among the outputs, the precise regulation of each output voltage is difficult. Therefore, different post-regulation schemes have been utilized on the secondary side, such as linear regulators and synchronous-switch post-regulators [17-18]. Several full-bridge DC-DC converters have been integrated into a single topology by sharing a common leg to achieve multiple outputs [19-21]. Uniquely connected two-transformer-based designs have been previously reported [21-22], which provide better cross-regulation under all load conditions and use complementary pulse width modulation.

A SIDO converter-based charging system is proposed, in which a single-phase AC supply is used to concurrently provide step-up and step-down outputs. Simultaneously, a proper coordinated control is required, which is essential for regulating the dual outputs of the proposed system. In the SIDO converter, the HFT is required to provide the required output voltage by adjusting the number of turns. In addition, owing to its integrated architecture, all outputs of the system are regulated using the same set of switches, making coordination control easier.

A brief introduction, literature review, motivations, and research objectives were provided in this section. Section 2 describes the proposed circuit configuration for the simultaneous step-up and step-down outputs. The steady-state operation and analysis of the integrated converter are presented in Section 3. The proposed charging system design and control strategy are described in Sections 4 and 5, respectively. Based on the simulation and experimental results, the steady-state and dynamic behavior analysis of the system is described in Section 6. Finally, Section 7 concludes this study regarding dual battery charging.

## 2 System description

Fig. 1 presents the circuit diagram of the proposed charger, which facilitates two output terminals for simultaneously charging the batteries of two EVs. One terminal charges the low-voltage battery of a 2-wheeler EV and the other charges the high-voltage battery of a 4-wheeler EV. It comprises three main converters: boost, SEPIC, and fly-back. In this system, the aforementioned converters are integrated into a boost-SEPIC configuration, where the SEPIC converter output is fed to a low-voltage battery terminal through a fly-back converter, as shown in Fig. 1.

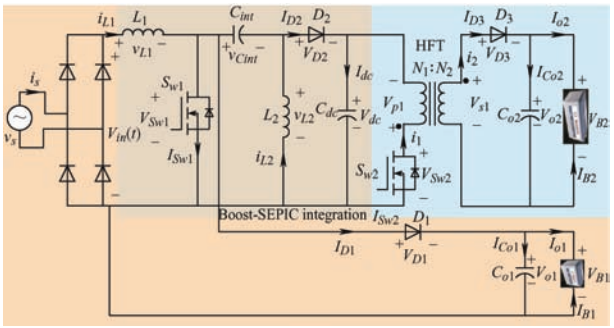


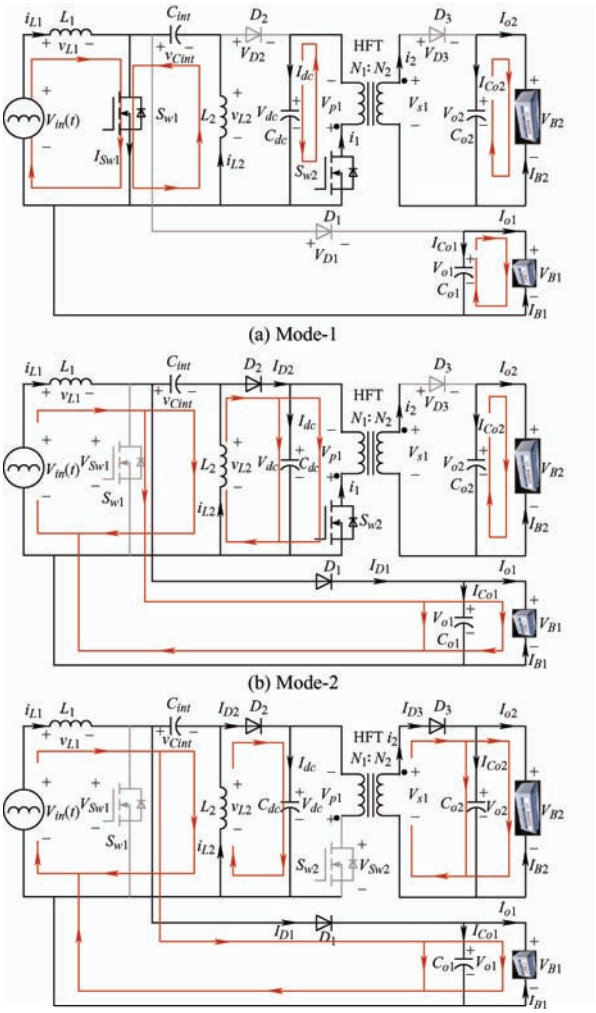

Fig. 1 Schematic of the off-board charger with integration of the boost-SEPIC fly back converter

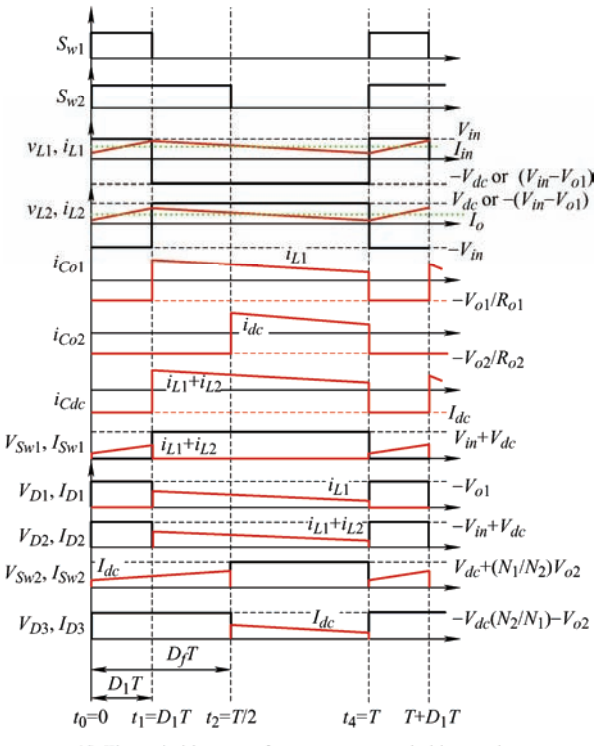
Furthermore, the output of the boost converter is directly connected to the terminal of the high-voltage

battery. In the proposed integrated system, the single-phase grid supply is fed to the DBR and the rectified output ($V_{in}$) of the DBR is fed to both the boost and SEPIC circuits. The DBR, input inductor $L_1$, and input side switch $S_{w1}$ are common parts of both the SEPIC and boost converter circuit. In the integrated converter, the boost-SEPIC combination comprises a common input inductor $L_1$, switch $S_{w1}$, output diode $D_2$, and the output capacitor $C_{o1}$ of the boost converter. Similarly, it comprises an intermediate capacitor $C_{int}$, output inductor $L_2$, output $D_2$, and output DC-link capacitor $C_{dc}$ of the SEPIC converter shown in Fig. 1. The output capacitor $C_{o1}$ of the boost converter is connected with the HV battery rated at 400 V, 40 A·h. Furthermore, the output of the SEPIC converter ($V_{dc}$) is connected as an input to the fly-back converter, and the output capacitor $C_{o2}$ of the fly-back converter is connected with the LV battery (48 V, 52 A·h). The fly-back converter comprises an HFT, switch $S_{w2}$, diode $D_3$, and output capacitor $C_{o2}$. The HFT transformer with a primary-to-secondary turn ratio ($N_1$ : $N_2$) provides the required DC voltage gain by adjusting the turn ratio $N$ in addition to the duty ratio of the switch $S_{w2}$. The output capacitors ($C_{o1}$, $C_{o2}$) filter the high frequency ripples from the battery current ($I_{B1}$, $I_{B2}$) individually and provide a ripple-free charging current to the respective batteries.

## 3 Steady-state operation

Prior to starting the analysis of the steady-state operation, the following assumptions were made. The passive components (inductor, capacitor) and semiconductor devices, such as switches and diodes, are assumed to be ideal. The values of the capacitors are assumed to be sufficiently large to provide a constant and ripple-free output voltage. The supply voltage ($v_s$) is assumed to be constant with an instantaneous value of $V_{in}$ during one switching cycle. The switching frequency is assumed to be significantly large compared to the line frequency, that is, 50 Hz/60 Hz. The converters operate in CCM mode in each mode. Fig. 2 shows the equivalent circuits for various operating modes based on the state (on/off) of switches ($S_{w1}$ and $S_{w2}$), as well as the switching voltage and current waveforms. Detailed operations of the converter during each operating mode are presented in the following subsections.




(d) The switching waveforms over one switching cycle

Fig. 2 Steady-state operation of the proposed converter mode-wise equivalent circuits

Mode-1($t_0<t<t_1$): $t_0$=0, this mode starts with switches $S_{w1}$ and $S_{w2}$ turned on, and diodes $D_1$, $D_2$, and $D_3$ are reverse-biased, as shown in Fig. 2a and 2d. Both inductors ($L_1$, $L_2$) start charging, and their respective currents, $i_{L1}$ and $i_{L2}$, increase linearly. Hence, during this period, energy transfer to the high-voltage output was achieved through output capacitor $C_{o1}$ of the boost converter. In addition, the intermediate capacitor $C_{int}$ starts discharging into inductor $L_2$. In this mode, the HFT stores energy from the DC-link capacitor ($C_{dc}$) of the SEPIC, and the output capacitor ($C_{o2}$) of the fly-back converter provides energy to charge the LV battery ($V_{B2}$). The related equations of the voltage and current are provided in Tab. 1.

**Tab. 1 Summary of the switching voltage and current equations**

| Circuit parameter | Mode of operation | | |
|---|---|---|---|
| | Mode-1 $(t_0<t<t_1)$ | Mode-2 $(t_1<t<t_2)$ | Mode-3 $(t_2<t<t_3)$ |
| $V_{L1}$ | $V_{in}$ | $-V_{dc}$ | $-V_{dc}$ |
| $V_{L2}$ | $V_{in}$ | $V_{dc}$ | $V_{dc}$ |
| $V_{D1}$ | $-V_{o1}$ | 0 | 0 |
| $V_{D2}$ | $-(V_{in}+V_{dc})$ | 0 | 0 |
| $V_{D3}$ | $-\left(\left(\frac{N_2}{N_1}\right)V_{dc}+V_{o2}\right)$ | $-\left(\left(\frac{N_2}{N_1}\right)V_{dc}+V_{o2}\right)$ | 0 |
| $I_{D1}$ | 0 | $I_{L1}$ | $I_{L1}$ |
| $I_{D2}$ | 0 | $I_{L1}+I_{L2}$ | $I_{L1}+I_{L2}$ |
| $I_{D3}$ | 0 | 0 | $I_{o2}$ |
| $V_{p1}$ | $V_{dc}$ | $V_{dc}$ | $-\left(\frac{N_1}{N_2}\right)V_{o2}$ |
| $V_{s1}$ | $\left(\frac{N_2}{N_1}\right)V_{dc}$ | $-\left(\frac{N_2}{N_1}\right)V_{dc}$ | $V_{o2}$ |
| $V_{Sw1}$ | 0 | $V_{in}+V_{dc}$ | $V_{in}+V_{dc}$ |
| $V_{Sw2}$ | 0 | 0 | $V_{dc}+\left(\frac{N_1}{N_2}\right)V_{o1}$ |
| $I_{Sw1}$ | $I_{L1}+I_{L2}$ | 0 | 0 |
| $I_{Sw2}$ | $I_{dc}$ | $I_{dc}$ | 0 |

Mode-2 ($t_1<t<t_2$): $t=t_1$, switch $S_{w1}$ turns off, switch $S_{w2}$ remains in the on state, and diode $D_3$ remains in the off state. Diodes $D_1$ and $D_2$ are forward-biased at $t=t_1$, as shown in Fig. 2b and Fig. 2d. In this mode, both inductors $L_1$, $L_2$ start discharging, and their respective currents, $i_{L1}$ and $i_{L2}$, decrease linearly. The input inductor $L_1$ discharges its energy to the step-up output through the freewheeling diode $D_1$ and charges the intermediate capacitor $C_{int}$. The output inductor $L_2$ transfers its energy through the freewheeling diode $D_2$ to the DC-link capacitor $C_{dc}$ to the fly-back converter. The energy transfers to the step-down output through the output capacitor ($C_{o2}$) of the fly-back converter. The voltage- and current-related equations are listed in Tab. 1.

Mode-3 ($t_2<t<t_3$): $t=t_2$, switches $S_{w1}$ and $S_{w2}$ turned off, and diode $D_3$ is forward-biased. However, diodes $D_1$ and $D_2$ are already in the conducting state at $t=T/2$, as shown in Fig. 2c and Fig. 2d. Similar to mode-2, input inductor $L_1$ discharges its energy to the step-up load through the freewheeling diode $D_1$, and the output inductor $L_2$ discharges its energy to the DC link capacitor $C_{dc}$. When switch $S_{w2}$ is in the off state, the stored energy of the HFT of the fly-back converter is transferred to the step-down output through the freewheeling diode $D_3$. The corresponding voltage and current equations are listed in Tab. 1.

## 4 Design considerations

This section describes the design aspects of the proposed integrated converter. The battery charger is designed for two output terminals rated at 400 V, 40 A·h and 48 V, 52 A·h. All passive components of the proposed converter are designed such that the converter operates in the CCM. The supply voltage $v_s(t)$ and output of the diode bridge rectifier $V_{in}(t)$ for the proposed single input dual output converter can be expressed as follows

$$\begin{cases} v_s(t) = V_m \sin(2\pi f_L t) \\ V_{in}(t) = V_m \left|\sin(2\pi f_L t)\right| \end{cases} \quad (1)$$

where, $V_m$ and $f_L$ indicate the peak voltage and line frequency of the input voltage, respectively.

The design of the integrated converter includes selection of the following various components: first, the boost-SEPIC integrated part, such as the input inductor ($L_1$), output inductor ($L_2$), intermediate capacitor ($C_{int}$), and DC link capacitor ($C_{dc}$) of the SEPIC converter and output capacitor ($C_{o1}$) of the boost converter; second, the SEPIC-fly-back part of the integrated converter consists of an HFT and an output capacitor ($C_{o2}$). For a satisfactory design of the input and output inductors ($L_1$, $L_2$), the average of inductor voltages $v_{L1}$ and $v_{L2}$ for one switching cycle should be zero.

$$\begin{cases} V_{L1} = V_{in}(DT_S) + (-V_{dc})(1-D)T_S = 0 \\ V_{L2} = (-V_{in})(DT_S) + V_{dc}(1-D)T_S = 0 \quad \text{For HV side} \\ V_{L1} = V_{in}(DT_S) + (V_{in} - V_{o1})(1-D)T_S = 0 \quad \text{For LV side} \end{cases} \tag{2}$$

where, $V_{dc}$ is the DC link output voltage of the SEPIC, and $V_{o1}$ is the output voltage of the boost converter. The simplification of Eq. (2) yields Eq. (3) as follows

$$\begin{cases} \dfrac{V_{o1}}{V_{in}} = \dfrac{1}{1-D} \\ V_{dc} = V_{in}\left(\dfrac{D}{1-D}\right) \end{cases} \tag{3}$$

Based on Eq. (3), the duty ratio $D$ for the HV output side is calculated to be $D$=0.2, and the value of $V_{dc}$ is calculated to be 81.25 V at the peak value of the supply voltage of 325 V.

The DC voltage gain in terms of the duty ratio $D_f$ for the LV-side output terminal is expressed in Eq. (4) as follows

$$V_{dc} = V_{o2}\left(\frac{N_2}{N_1}\right)\left(\frac{D_f}{1-D_f}\right) \tag{4}$$

where $V_{dc}$ is the DC-link output voltage of the SEPIC converter, which is the input for the fly-back converter, $V_{o2}$ is the output of the fly-back converter, $N$ is secondary to the primary turn ratio, and $D_f$ is the duty ratio of the fly-back converter.

To achieve the required output voltage with a considerable $D_f$, $N$ was set to 0.6. As the output voltage across the battery was 48 V, the calculated duty ratio $D_f$ based on Eq. (4) was 0.5. The primary and secondary voltages ($Vp_1$, $Vs_2$) of the HFT were calculated based on the design requirements as follows

$$\begin{cases} \left.\begin{cases} V_{p1} = V_{dc} \\ V_{s1} = \left(\dfrac{N_2}{N_1}\right)V_{dc} \end{cases}\right\} \text{When } S_{w2} \text{ is ON} \\ \left.\begin{cases} V_{p1} = \left(\dfrac{N_1}{N_2}\right)V_{o2} \\ V_{s1} = V_{o2} \end{cases}\right\} \text{When } S_{w2} \text{ is OFF} \end{cases} \tag{5}$$

### 4.1 Design of the input ($L_1$) and output ($L_2$) inductors

The proposed integrated converter has a common input inductor $L_1$, which is designed based on a conventional boost converter or SEPIC topology, and an output inductor $L_2$ is designed based on a conventional SEPIC topology. The critical inductance $L_{crit}$ is required to ensure CCM operation. In practical applications, the values of the inductance should be greater than their respective $L_{crit}$, for inductor currents ($I_{L1}$, $I_{L2}$) are continuous in nature.

$$\begin{cases} L_{1crit} = \dfrac{(1-D)^2 R}{2Df_s} \\ L_{2crit} = \dfrac{(1-D)R}{2f_s} \end{cases} \tag{6}$$

For the design of the input and output inductors, the average input and output inductor currents ($I_{L1}$, $I_{L2}$) were considered to be equal to the average input $I_{in}$ and DC link current $I_{dc}$ of the SEPIC.

The ripple across the input and output inductor current was assumed to be $\Delta i_{L1}$=30% of the input current $I_{in}$, and $\Delta i_{L2}$=30% of the output current $I_{dc}$. The input and output inductors in terms of the ripple current are expressed as follows

$$\begin{cases} L_1 = \dfrac{V_{in} \times D}{f_s \times \Delta i_{L1}} \\ L_2 = \dfrac{V_{o2} \times (1-D)}{f_s \times \Delta i_{L2}} \end{cases} \tag{7}$$

Based on Eq. (7), the calculated values of the min critical input and output inductor are 1.47 mH and 0.36 mH, respectively.

### 4.2 Design of the intermediate capacitor ($C_{int}$), DC link capacitor ($C_{dc}$), and output capacitors ($C_{o1}$, $C_{o2}$)

For the design of the intermediate capacitor $C_{int}$ and DC link output capacitor $C_{dc}$ of the SEPIC converter, the output capacitor $C_{o1}$ of the boost converter and the output capacitor $C_{o2}$ of the fly-back converter, it is assumed that the large values of the capacitors maintain the intermediate, DC link, and output voltages constant. Therefore, a small percentage of the ripple was considered to maintain the intermediate, DC link, and output voltages constant. The design equations for the intermediate, DC link, and output capacitors ($C_{int}$, $C_{dc}$, $C_{o1}$, and $C_{o2}$) are given by Eqs. (8)-(9) as follows

$$C_{int} = \frac{D}{R\left(\dfrac{\Delta V_{Cint}}{V_{o2}}\right)f_s} \tag{8}$$

where, the average voltage across the intermediate capacitor is equal to the output voltage of the DBR $V_{cint}$=$V_{in}$. Therefore, the ripple across the intermediate capacitor is $\Delta V_{Cint}$=10% of the input voltage ($V_{in}$).

$$\begin{cases} C_{dc}=\dfrac{D}{R\left(\dfrac{\Delta V_{dc}}{V_{dc}}\right)f_s} \\ C_{o1}=\dfrac{D}{R\left(\dfrac{\Delta V_{o1}}{V_{o1}}\right)f_s} \\ C_{o2}=\dfrac{D_f}{R\left(\dfrac{\Delta V_{o2}}{V_{o2}}\right)f_s} \end{cases} \tag{9}$$

The ripples across the outputs and DC link capacitor are $\Delta V_{Cdc}$=1% of the DC link output voltage $V_{dc}$, $\Delta V_{Co1}$, and $\Delta V_{Co2}$=1% of the output voltages $V_{o1}$ and $V_{o2}$, respectively. The calculated value of $C_{int}$ is 10.6 μF and the values of $C_{dc}$, $C_{o1}$, and $C_{o2}$ are 3 800 μF, 4 000 μF, and 2 173 μF, respectively.

## 5 Control scheme

A schematic of the control schemes for the constant current (CC) and constant voltage (CV) modes of the HV and LV batteries is presented in Fig. 3. This control structure is used for PFC at the grid side, while also maintaining a constant voltage/current for charging the dual batteries (HV and LV) of the proposed charging system. The switching action of switch $S_{w1}$ is controlled to maintain power factor correction at the input side and regulate the output voltage/current of the HV side ($V_{o1}$, $I_{o1}$). The control block for switch $S_{w2}$ is solely utilized to regulate the LV-side output voltage/current ($V_{o2}$, $I_{o2}$). Therefore, there is no additional requirement for the sensing circuit for $S_{w2}$ for power-factor correction on the grid side, making the control structure simpler. The overall control of the charger is implemented using minimum-sensing devices, as shown in Fig. 3.

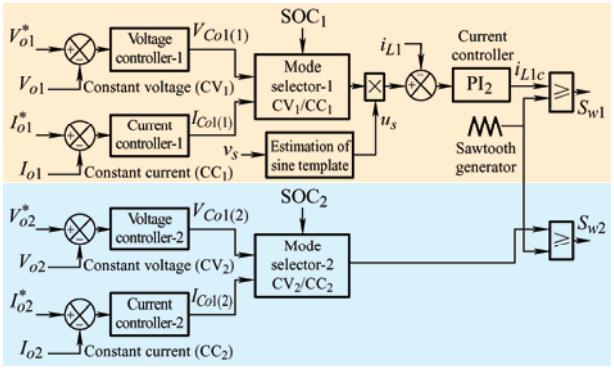



Fig. 3 Control structure for the SIDO dual battery charger

In an integrated SIDO-based battery charging system, the output voltage and current of the HV battery connected to the grid via a boost converter is sensed for charging in the CV and CC modes, respectively. Similarly, the output voltage and current of the LV battery connected to the grid via the SEPIC-fly-back converter is sensed for charging in the CV and CC modes, respectively.

In addition, the input inductor current $i_{L1}$ of the boost-SEPIC integrated side is also sensed for PFC at the grid side in the proposed system. The CV and CC modes of the charging operation are operated according to the selected SOC value through a mode selector block.

The control arrangement of the HV side, as shown in Fig. 3, comprises two controllers: the voltage controller CV$_1$ and current controller CC$_1$. These controllers work together to regulate the output voltage ($V_{o1}$)/current ($I_{o1}$). The mode selector block determines the operation of the controllers and ensures the operation of one controller at a time according to the SOC value. In the beginning, the SOC$_1$ of the HV battery is at 30%; therefore, the HV battery charges under a constant current mode CC$_1$. Subsequently, the output current $I_{o1}$ is detected and compared with the reference output current $I_{o1}^*$; the obtained current error $I_{eo1}(j)$ at instant $j$ is given by Eq. (10). The error $I_{eo1}(j)$ *is* fed to current controller-1 (CC$_1$) to generate the controlled output $I_{Co1}$ as follows

$$\begin{cases} I_{eo1}(j)=I^*_{o1}(j)-I_{o1}(j) \\ I_{Co1}(j)=I_{Co1}(j-1)+k_{ijc1}I_{eo1}(j)+k_{pjc1}[I_{eo1}(j)-I_{eo1}(j-1)] \end{cases} \tag{10}$$

where, $k_{ijc1}$ and $k_{pjc1}$ indicate the current controller-1 integral and proportional gains.

When SOC$_1$ reaches a 90% value, the mode selector block changes its charging profile from the CC$_1$ to CV$_1$ mode. In the constant-voltage (CV$_1$) mode of operation, voltage controller-1 (CV$_1$) is used to maintain a constant output voltage to charge the HV battery. The output voltage $V_{o1}$ is detected and compared with the reference voltage; the obtained error $V_{eo1}(j)$ is fed to voltage controller-1 (CV$_1$) to generate the controlled output voltage $V_{Co1}(j)$ at any instant $j$.

$$\begin{cases} V_{eo1}(j) = V^*_{o1}(j) - V_{o1}(j) \\ V_{Co1}(j) = V_{Co1}(j-1) + k_{ijv1} V_{eo1}(j) + k_{pjv1}[V_{eo1}(j) - V_{eo1}(j-1)] \end{cases} \tag{11}$$

where $k_{ijv1}$ and $k_{pjv1}$ indicate the voltage controller-1 integral and proportional gains.

Subsequently, the controlled output of the selector mode is multiplied by the unit sine template $u_s$, and the obtained reference is given by Eq. (12) as follows

$$\begin{cases} u_s(j) = \left| \dfrac{v_s(j)}{V_m} \right| \\ i^*_{L1}(j) = u_s(j) \cdot V_{Co1}(j) = u_s(j) \cdot I_{Co1}(j) \end{cases} \tag{12}$$

In the inner loop of the control structure, the reference obtained from Eq. (12) is compared with the detected inductor current $i_{L1}$, obtaining the current error $i_{L1e}(j)$ at instant '$j$'. This current error is fed to the next current controller $PI_2$, and the controlled output $i_{L1c}$ is generated as follows

$$\begin{cases} i_{L1e}(j) = i^*_{L1}(j) - i_{L1}(j) \\ i_{L1c}(j) = i_{L1c}(j-1) + k_{iL1} i_{L1e}(j) + k_{pL1}[i_{L1e}(j) - i_{L1e}(j-1)] \end{cases} \tag{13}$$

Here, $k_{iL1}$ and $k_{pL1}$ are the current controller integral and proportional gain, respectively. This generated current controller output was compared with a saw tooth triangular wave with a frequency of 5 kHz, and generated a pulse for the common switch $S_{w1}$ of the integrated SEPIC-boost converter.

Further, in the control arrangement of the LV battery charging, the voltage controller-2 ($CV_2$) and current controller-2 ($CC_2$) operated in the CV and CC modes of operation, respectively. Charging was controlled by controlling the duty cycle of switch $S_{w2}$ of the fly-back converter. At the beginning, the LV battery was charged in the CC mode at $SOC_2$=30%. The mode selector block selected the $CC_2$ controller to ensure the charging operation in the CC mode. The output current $I_{o2}$ was detected and compared to the reference output current, and the current error $I_{eo2}(j)$ was obtained at instant $j$, as shown in Eq. (14). The error $I_{eo2}(j)$ was fed to $CC_2$ to generate the controlled output $I_{Co2.}$

$$\begin{cases} I_{eo2}(j) = I^*_{o2}(j) - I_{o2}(j) \\ I_{Co2}(j) = I_{Co2}(j-1) + k_{ijc2} I_{eo2}(j) + k_{pjc2}[I_{eo2}(j) - I_{eo2}(j-1)] \end{cases} \tag{14}$$

where $k_{ijc2}$ and $k_{pjc2}$ indicate the current controller-2 integral and proportional gains.

When $SOC_2$ reaches a 95% value, the mode selector block is changed from the CC to CV mode. In the constant-voltage ($CV_2$) mode of operation, the LV battery output voltage $V_{o2}$ is detected and compared to the reference voltage, and the error $V_{eo2}(j)$ is obtained, which is fed to voltage controller-2 ($CV_2$) to generate the controlled output $V_{Co2}(j)$ at any instant $j$.

$$\begin{cases} V_{eo2}(j) = V^*_{o2}(j) - V_{o2}(j) \\ V_{Co2}(j) = V_{Co2}(j-1) + k_{ijv2} V_{eo2}(j) + k_{pjv2}[V_{eo2}(j) - V_{eo2}(j-1)] \end{cases} \tag{15}$$

where $k_{ijv2}$ and $k_{pjv2}$ indicate the voltage controller-2 integral and proportional gains.

The controlled output of either voltage $V_{Co2}$ or current $I_{Co2}$ of the mode-selector block is compared to a saw tooth triangular wave with an operating frequency of 5 kHz, which generates a pulse for switch $S_{w2}$ of the fly-back converter.

## 6 Results and discussions

The proposed dual battery charger is rated at 3.2 kW and designed to charge an HV battery of 40 A·h and a 48 V LV battery of 52 A·h. The charger operates from a single-phase supply of 230 V and 50 Hz, and is capable of providing 3.2 kW for the HV battery and 500 W for the LV battery. The performance of the developed charging system has been evaluated and validated for both resistive and battery loads through simulations using the Matlab toolbox, with an "ode4" solver and 20 μs sampling time. The control parameters for the simulation study were as follows. For the HV battery, the parameters were $k_{pjv1}$=0.1 and $k_{ijv1}$=25 in the CV mode, and $k_{pjc1}$=0.1 and $k_{ijc1}$=80 in the CC mode. For the LV battery, the parameters were $k_{pjv2}$=0.12 and $k_{ijv2}$=2.5 in the CV mode, and $k_{pjc2}$=0.009 and $k_{ijc2}$=0.9 in the CC mode. For the inner PI current controller, $k_{pL1}$=0.9 and $k_{iL1}$=2.5, which were the same in both CV and CC mode operations.The design parameters of the proposed dual battery charger are shown in Tab. 2.

**Tab. 2 Design parameters for the simulation and experimental study**

| No. | Specified parameters | Design values |
|---|---|---|
| 1 | Single-phase supply voltage | 230 V, 50 Hz |
| 2 | Input and output inductances $L_1$, $L_2$ | $L_1$=2.5 mH<br>$L_2$=1.25 mH |
| 3 | Intermediate capacitors $C_{int}$/μF | 10 |
| 4 | Output capacitors $C_{o1}$, $C_{o2}$ and DC link capacitor $C_{dc}$/μF | 5 000 |
| 5 | Switching frequency for both switches $S_{w1}$, $S_{w2}$ $f_s$/kHz | 5 |

These simulation results were validated in steady and dynamic states with a resistive load, and the same system was tested with the battery load in a laboratory environment, as shown in Fig. 4; the entire system was implemented using dSPACE-1104. To verify the dual operation of the proposed system, simulation and experimental results were obtained using the following four different combinations of the HV and LV battery: CC-CC, CC-CV, CV-CV, and CV-CC modes.

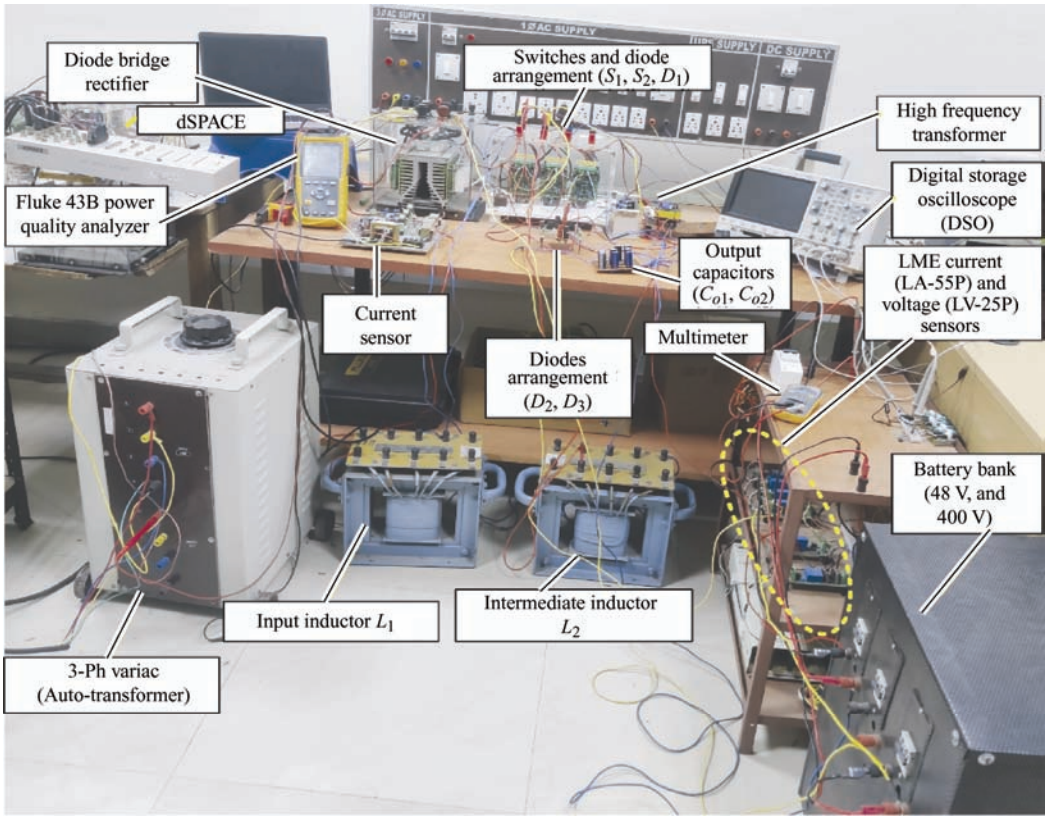



Fig. 4 Image of prototype power circuit of SIDO integrated based dual battery charger

## 6.1 Simulation results

### 6.1.1 Steady state performance of the proposed charger with 230 V, 50 Hz single-phase supply in the CC and CV operating modes

The waveforms of the supply voltage ($v_s$), supply current ($i_s$), and battery parameters ($V_{B1}$, $I_{B1}$, $SOC_1$ (%), $V_{B2}$, $I_{B2}$, $SOC_2$ (%)) with the four modes of operation (CC-CC, CC-CV, CV-CC, and CV-CV) are shown in Fig. 4. Fig. 5 reveals that the supply voltage and current are in the same phase and maintain PFC at each four different operating modes from $t$=0.3 s to 0.9 s. The results shown in Fig. 5a indicate that both the HV and LV batteries are operating in a constant current mode with identical SOCs of 30%. Accordingly, the results display constant currents of 8 A and 10.4 A for the HV and LV batteries, respectively. At first, both batteries are charging under the CC mode; as a result, the battery voltages are lower, that is, 368 V across the HV battery and 44.5 V across the LV battery.

Fig. 5b presents a constant current of 8 A for the HV battery operating in the CC mode and a constant voltage of 48 V for the LV battery in the CV mode. The HV battery in the CC mode and the LV battery in the CV mode have a lower voltage and current of 368 V and 4.5 A, respectively, as shown in Fig. 5b. Fig. 5c presents the results of when both batteries are operating in the CV mode, where $SOC_1$ of the HV battery is 90% and $SOC_2$ is 95%. In the CV mode of operation, the system provides a constant voltage of

400 V and a lower current of 3.5 A for the HV battery at 90% $SOC_1$; similarly, a constant voltage of 48 V and lower current of 4.5 A appears for the LV battery at 95% $SOC_2$.

Fig. 5d presents the results of the CV-CC operation mode, where the HV battery is in the CV mode and the LV battery is in the CC mode. Here, the HV battery maintained a constant voltage of 400 V at a 90% $SOC_1$ value, whereas the LV battery maintained a constant current of 10.4 A at a 30% $SOC_2$ value.

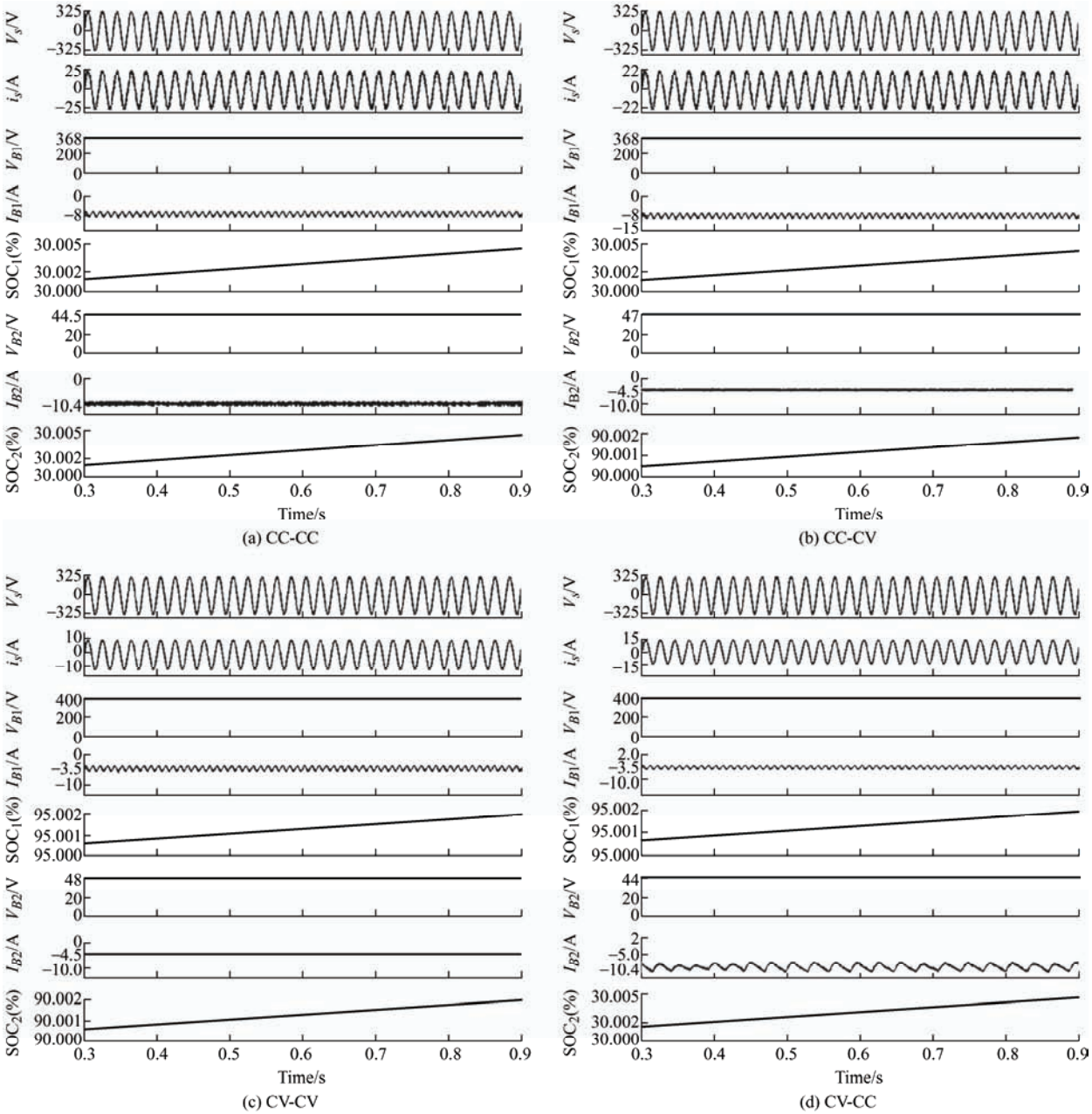


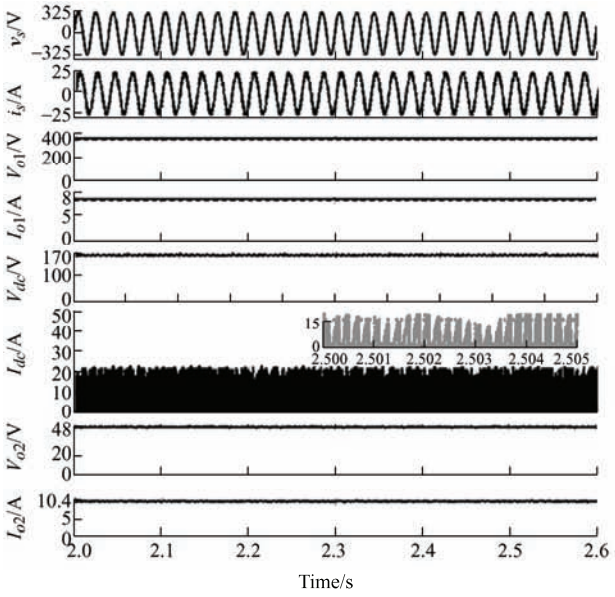

Fig. 5 Steady-state results of charging two batteries in different operating modes at a 230 V supply voltage

6.1.2 Steady-state performance of the integrated boost-SEPIC fly-back converter-based dual battery charger at a 230 V supply voltage with a resistive load

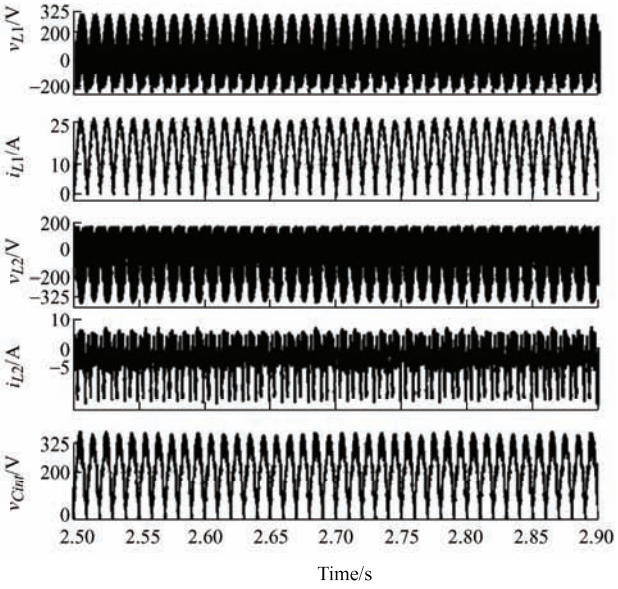
The steady-state performance of the proposed system was explained by a resistive load at a supply voltage of 230 V. The dual output converter system resulted in a step-up output of 400 V and 3.2 kW, and step-down output of 48 V and 500 W of the resistive load simultaneously.

Fig. 6 presents the waveforms of the input voltage and current ($v_s$, $i_s$), the DC output of the SEPIC converter and input of the fly-back converter ($V_{dc}$, $I_{dc}$), and the dual step-up and step-down outputs ($V_{o1}$ and $I_{o1}$, $V_{o2}$ and $I_{o2}$). It also demonstrates the waveforms of the inductor voltage and current ($v_{L1}$, $i_{L1}$, $v_{L2}$ and $i_{L2}$),

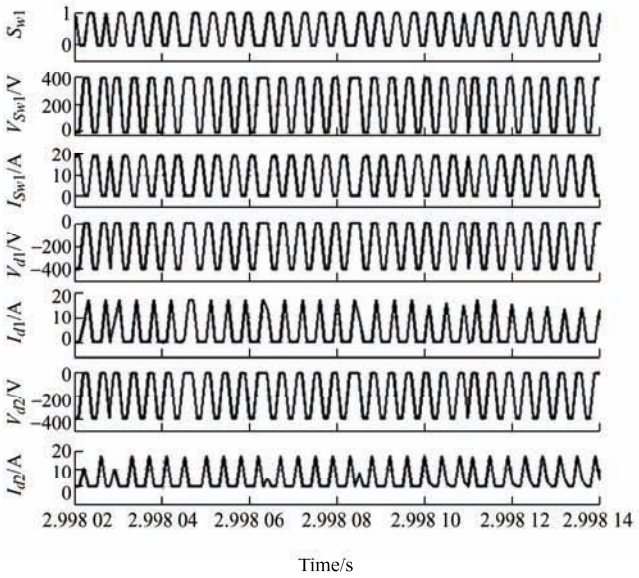
intermediate capacitor voltage ($v_{Cint}$), and voltage stress across the switches and diodes ($V_{Sw1}$, $I_{Sw1}$, $V_{Sw2}$, $I_{Sw2}$, $V_{d1}$, $I_{d1}$, $V_{d2}$, $I_{d2}$ and $V_{d3}$, $I_{d3}$). Fig. 6a depicts the power factor unity by virtue of the input voltage and current in the same phase from $t$=2 s to 2.6 s. The regulated step-up output voltage and current ($V_{o1}$, $I_{o1}$) were 400 V and 8 A, respectively; the step-down output voltage and current ($V_{o2}$, $I_{o2}$) were 48 V and 10.4 A. Furthermore, the DC link output voltage and current of the integrated converter ($V_{dc}$, $I_{dc}$) were 170 V and 10 A. The DC link current is discontinuous in nature, which is the input for a fly-back converter that offers a step-down output. According to the condition of the switch (on and off), Fig. 6b presents the inductor voltage and current waveforms ($v_{L1}$, $v_{L2}$, $i_{L1}$ and $i_{L2}$) from $t$=2.5 s to 2.9 s.



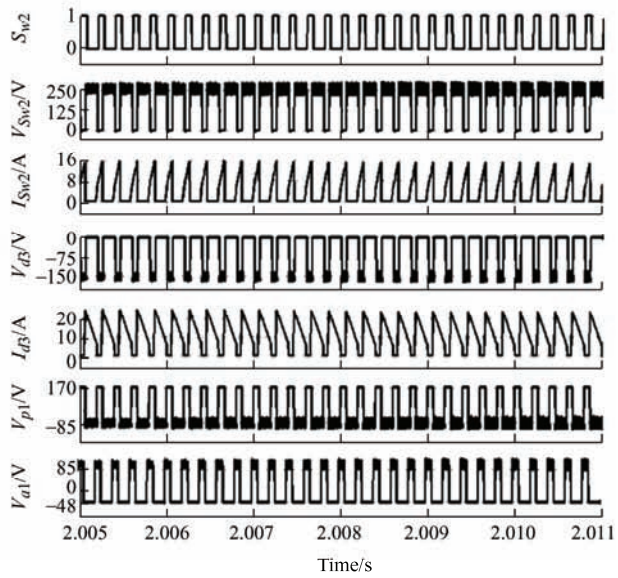

(a) Output voltages w.r.t supply voltage




(b) Inductor voltage and currents




(c) Voltage and current stress across $S_{w1}$, $d_1$, and $d_2$




(d) Voltage and current stress across $S_{w2}$, $d_3$ and the primary and secondary voltage across the transformer

Fig. 6 Steady-state results for the resistive load at a 230 V supply voltage

Fig. 6b demonstrates that the input inductor voltage is equal to the input voltage of 325 V, and the DC link output voltage is –170 V. The same waveform represents an intermediate capacitor ($v_{Cint}$) that follows the output voltage waveform of the DBR. The voltage and average current stress across the switch and diodes ($S_{w1}$, $D_1$ and $D_2$) are 400 V and 10 A, respectively, as shown in Fig. 6c from $t$=2.998 02 s to 2.998 14 s. Fig.

6d presents the waveform of the voltage stress across the switch and diode ($S_{w2}$, $D_3$), and the primary and secondary voltages of the HFT used to offer the step-down output. Fig. 6d demonstrates that the voltage stress and average current stress of switch $S_{w2}$ are 250 V and 10 A, respectively.

It also demonstrates that the voltage stress and average current stress across diode $D_3$ are 129 V and 10.4 A, respectively, where the average current stress is equal to the output current $I_{o2}$. Fig. 6d presents the primary and secondary voltages across the HFT according to the turn-on and turn-off conditions of switch $S_{w2}$. These results satisfy the requirement of a step-down output voltage of 48 V from $t$=2.005 s to 2.011 s.

6.1.3 Harmonic spectra of the battery charger with a battery and resistive load

Fig. 7 demonstrates the THD in the input current for four different operating conditions of the HV- and LV-side batteries and the resistive load. The input current THDs were 2.5% in the CC-CC mode, 2.87% in the CC-CV mode, 4.43% in the CV-CV mode, and 5.55% in the CV-CC mode for the HV and LV battery operating modes, respectively. The THD in the input current is 3.67% for the dual output resistive loads of 400 V, 3.2 kW and 48 V, 500 W. Fig. 7 demonstrates that the THDs in the input current at different operating modes are satisfied within the limit of IEEE-519-2014 standard.

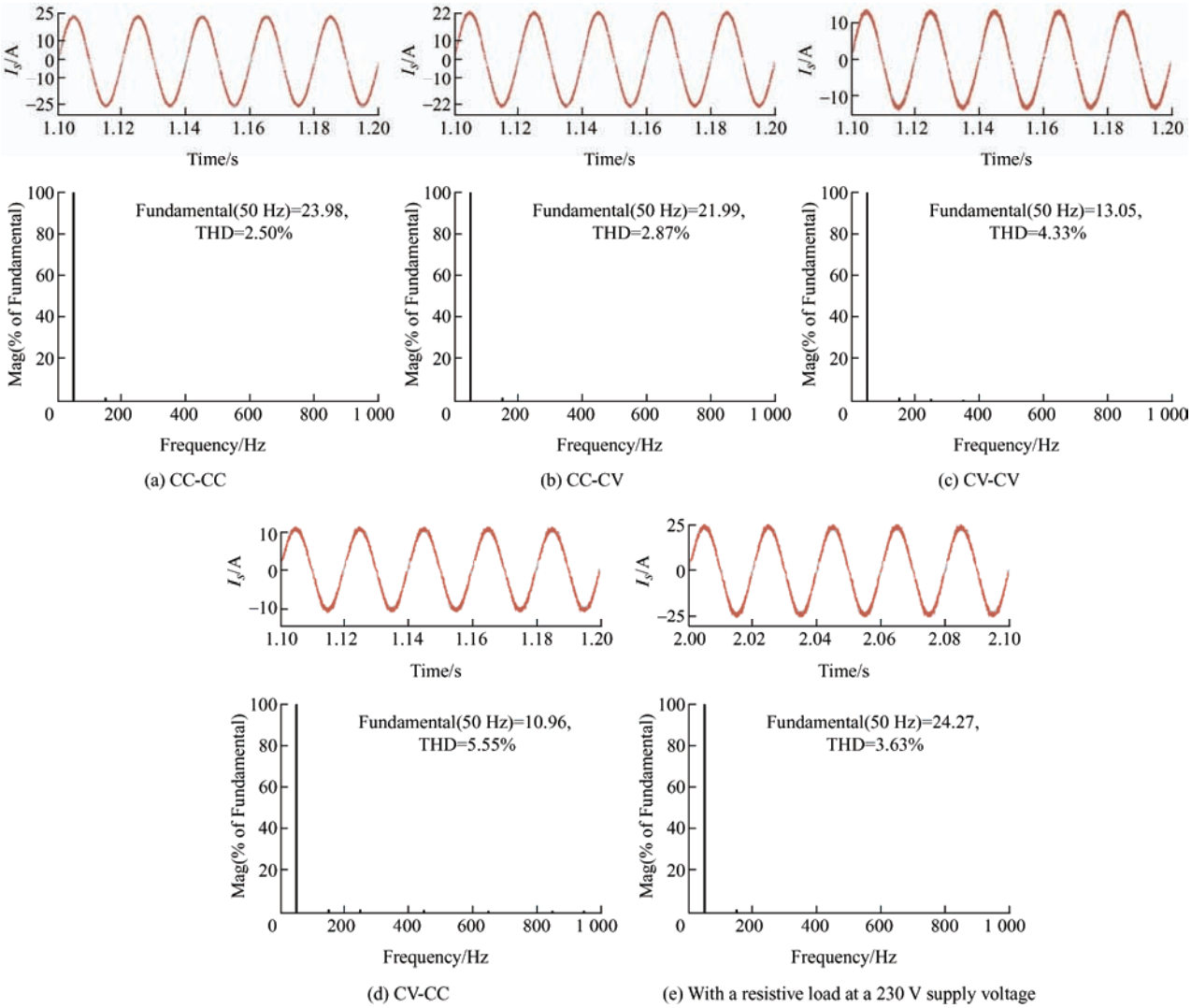
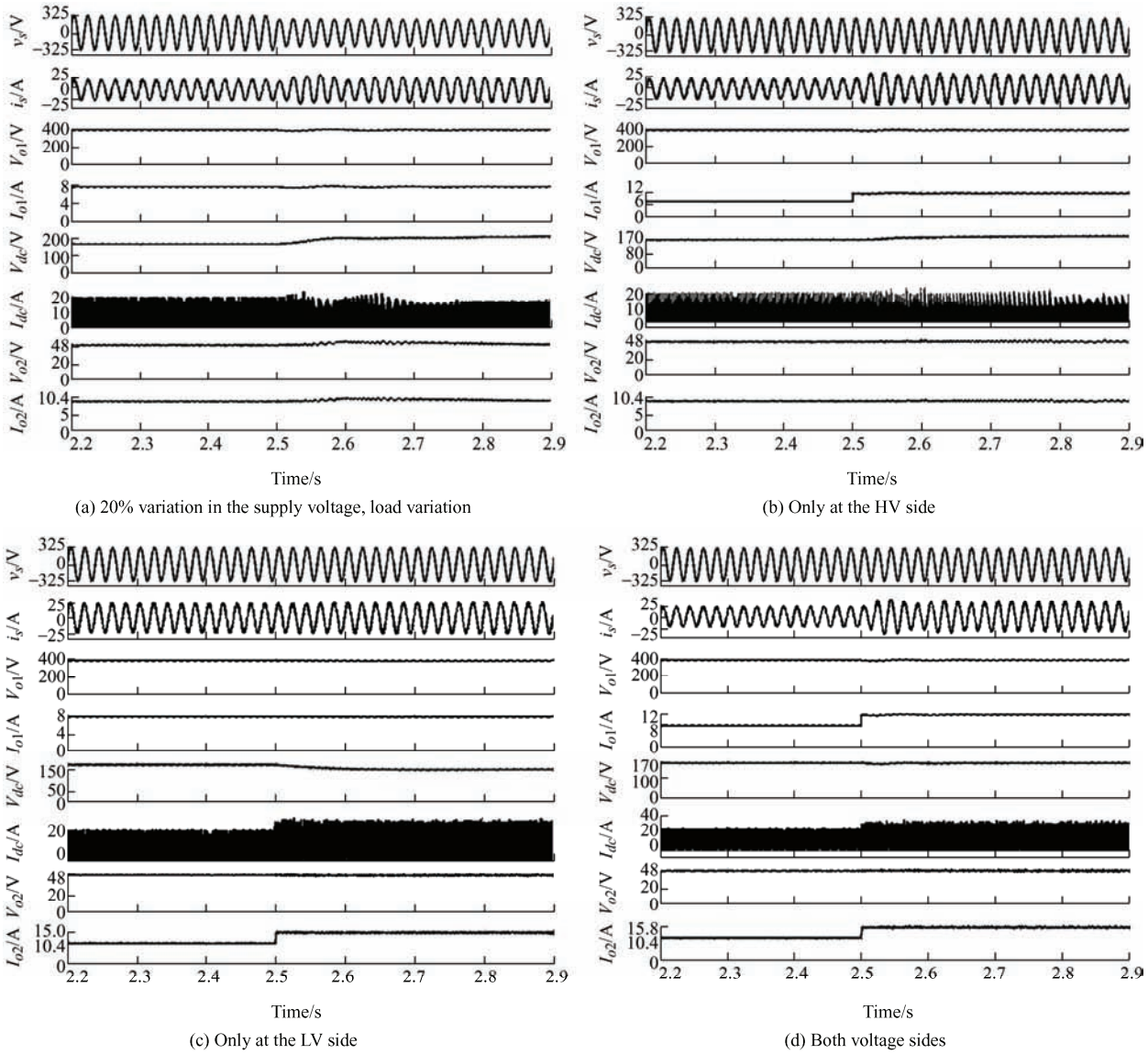



Fig. 7 Harmonic spectra of the input current with four different operating modes

6.1.4 Dynamic performance of the integrated boost-SEPIC fly-back converter-based dual battery charger

The dynamic performance of the system with supply and load variations are presented in Fig. 8 from $t$=2.2 s to 2.9 s. Fig. 8a presents the results with a 20% step decrement in the supply voltage from 230 V to 180 V, demonstrating the variation in the input current to

maintain the output power constant at $t$=2.5 s. Therefore, Fig. 8a depicts the output voltages $V_{o1}$ and $V_{o2}$ that were maintained constant at 400 V and 48 V, respectively, after a 300 s variation at $t$=2.5 s. Owing to the variation in the input voltage at $t$=2.5 s, the DC link voltage and current also undergoes into variations, while still maintaining the constant output voltages Fig. 8b and Fig. 8d present the load variation for three different conditions: variation in the HV side, variation in the LV side, and variation in both the HV and LV sides. Fig. 8b presents the load variation from 8 A to 12 A at the high-voltage side, despite maintaining a constant output voltage of 400 V. However, it represents no variation at the LV-side load. Similarly, Fig. 8c presents the constant output voltage of 48 V at the load variation from 10.4 A to 15.8 A at the LV side, continuing to present no variation at the HV side load. Figs. 8b and 8c also present the variation in the DC link voltage and current of the SEPIC with the variation in load at either the HV or LV sides. Fig. 8d presents the load variation at both the HV and LV sides at $t$=2.5 s. Fig. 8d presents constant output voltages of 400 V at the HV side and 48 V at the LV side, as well as a constant DC link voltage of 170 V after a 100 s cycle variation at $t$=2.5 s.




(a) 20% variation in the supply voltage, load variation

(b) Only at the HV side

(c) Only at the LV side

(d) Both voltage sides

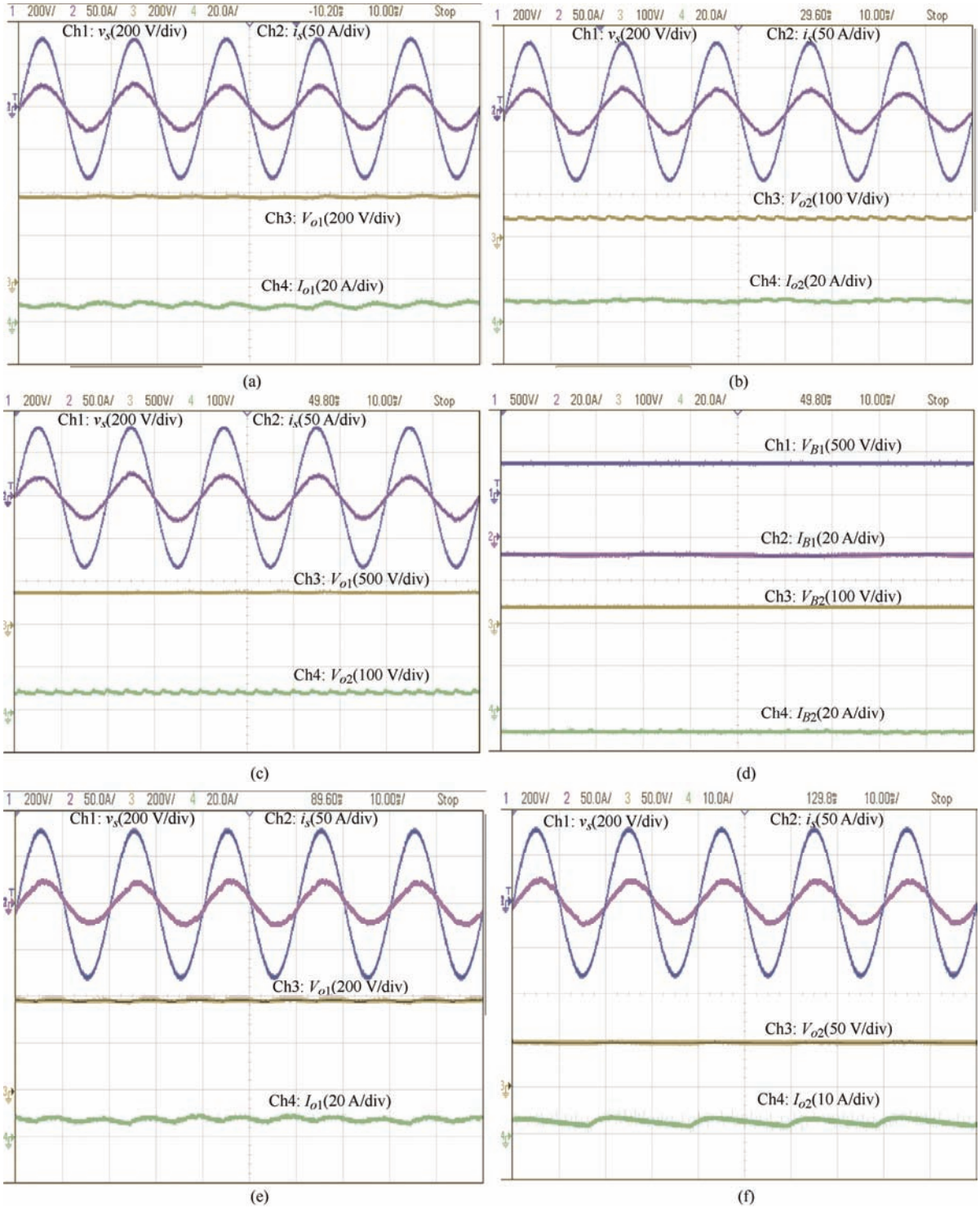
Fig. 8 Dynamic results of the dual output resistive load

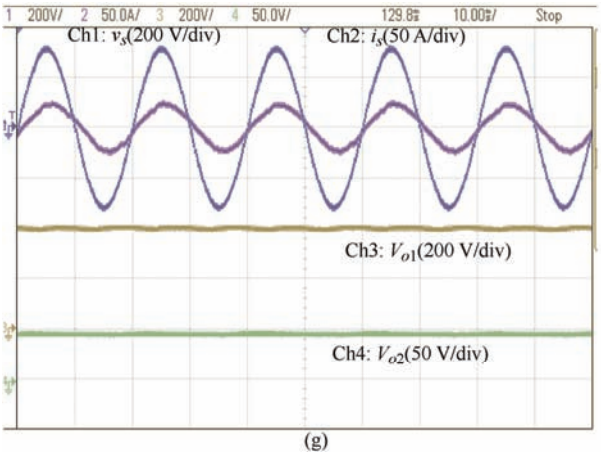
### 6.2 Test results

To validate the simulation results of the proposed system, a prototype model was developed in the laboratory with the same specifications, and its control scheme is implemented in the controller (d-SPACE 1104) with a sampling time of 40 μs. A Fluke power quality analyzer in a single phase (43 B) and an

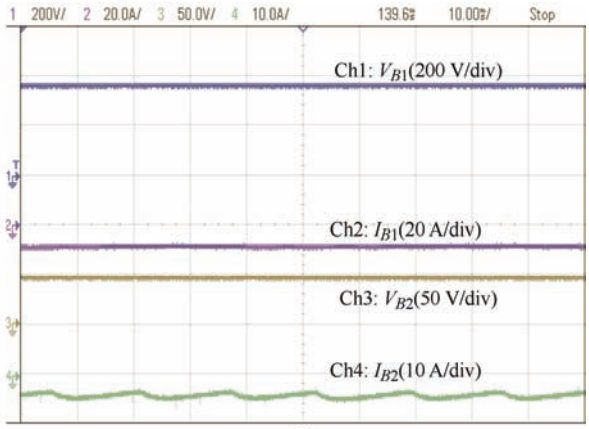
Agilent four-channel DSO-X-2004A digital oscilloscope were used to measure the test waveforms under four different operating modes.

Fig. 9 demonstrates the supply voltage and current ($v_s$, $i_s$), output voltages of the HV and LV sides ($V_{o1}$, $I_{o1}$, $V_{o2}$, $I_{o2}$), and the HV and LV battery voltages and currents ($V_{B1}$, $I_{B1}$, $V_{B2}$, $I_{B2}$). The performance of the dual battery charger is presented in Fig. 9 under four different operating modes of the HV and LV batteries (a-d) CC-CC, (e-h) CC-CV, (i-l) CV-CV, and (m-p) CV-CC. Fig. 9 presents the HV and LV batteries with constant voltages of 400 V and 48 V in the CV mode and constant currents of 8 A and 10.4 A in the CC mode, respectively. It also demonstrates that the supply voltage and current are in the same phase for all four operating modes that satisfy the unity PF operations.

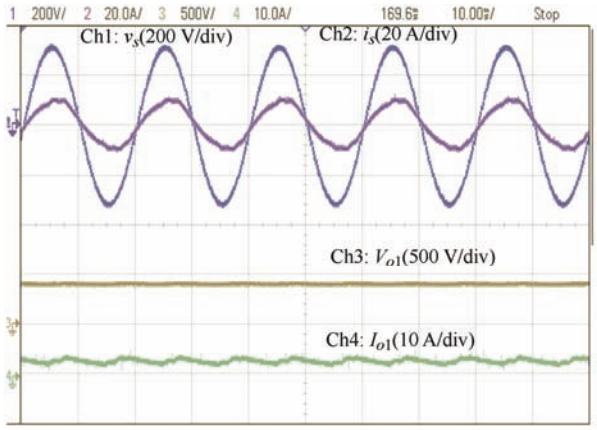



Ch1: $v_s$(200 V/div)
Ch2: $i_s$(50 A/div)
Ch3: $V_{o1}$(200 V/div)
Ch4: $V_{o2}$(50 V/div)

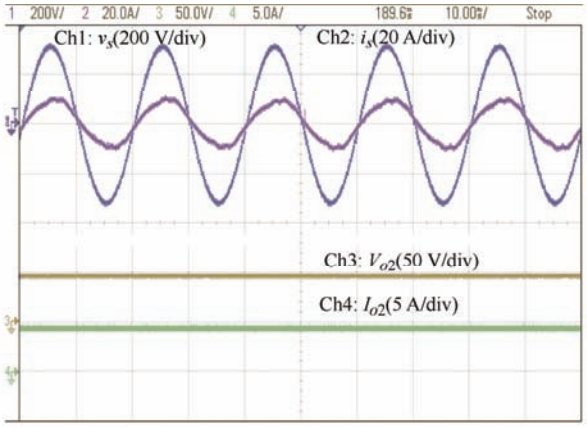
(g)


Ch1: $V_{B1}$(200 V/div)
Ch2: $I_{B1}$(20 A/div)
Ch3: $V_{B2}$(50 V/div)
Ch4: $I_{B2}$(10 A/div)

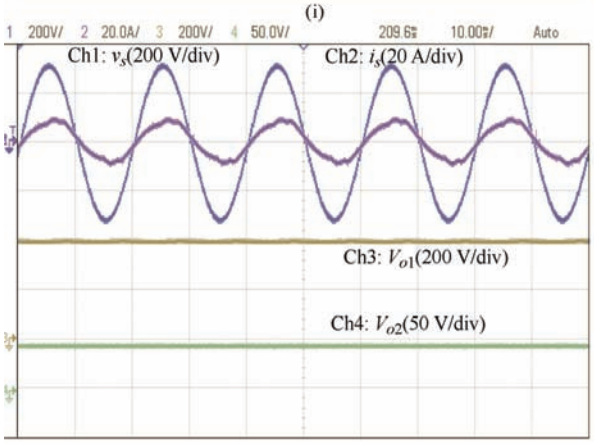
(h)


Ch1: $v_s$(200 V/div)
Ch2: $i_s$(20 A/div)
Ch3: $V_{o1}$(500 V/div)
Ch4: $I_{o1}$(10 A/div)

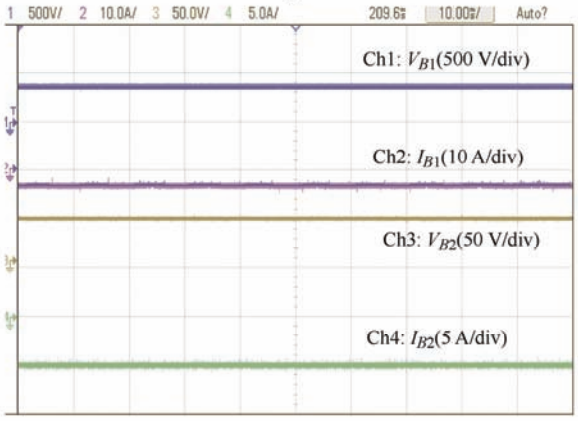
(i)


Ch1: $v_s$(200 V/div)
Ch2: $i_s$(20 A/div)
Ch3: $V_{o2}$(50 V/div)
Ch4: $I_{o2}$(5 A/div)

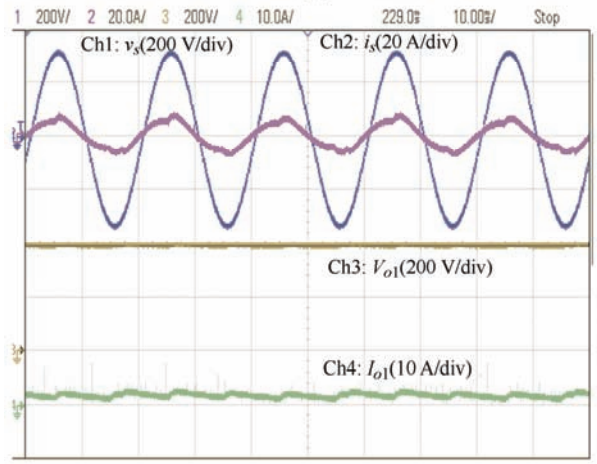
(j)


Ch1: $v_s$(200 V/div)
Ch2: $i_s$(20 A/div)
Ch3: $V_{o1}$(200 V/div)
Ch4: $V_{o2}$(50 V/div)

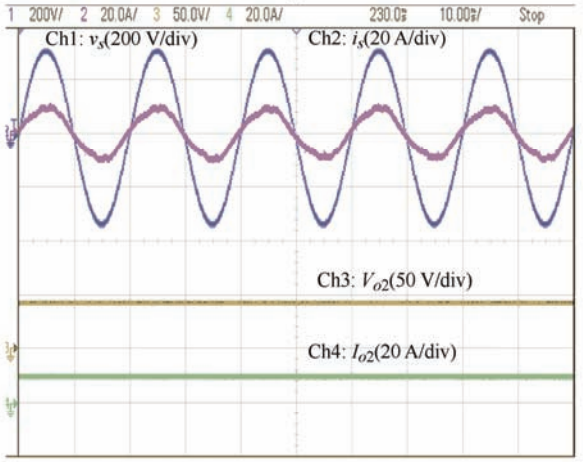
(k)


Ch1: $V_{B1}$(500 V/div)
Ch2: $I_{B1}$(10 A/div)
Ch3: $V_{B2}$(50 V/div)
Ch4: $I_{B2}$(5 A/div)

(l)


Ch1: $v_s$(200 V/div)
Ch2: $i_s$(20 A/div)
Ch3: $V_{o1}$(200 V/div)
Ch4: $I_{o1}$(10 A/div)

(m)


Ch1: $v_s$(200 V/div)
Ch2: $i_s$(20 A/div)
Ch3: $V_{o2}$(50 V/div)
Ch4: $I_{o2}$(20 A/div)

(n)

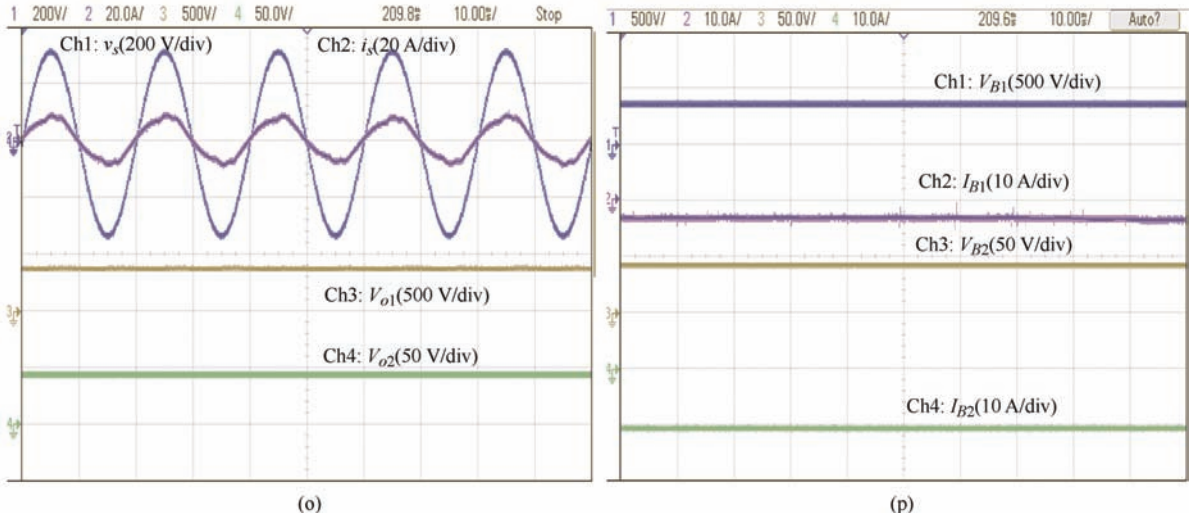
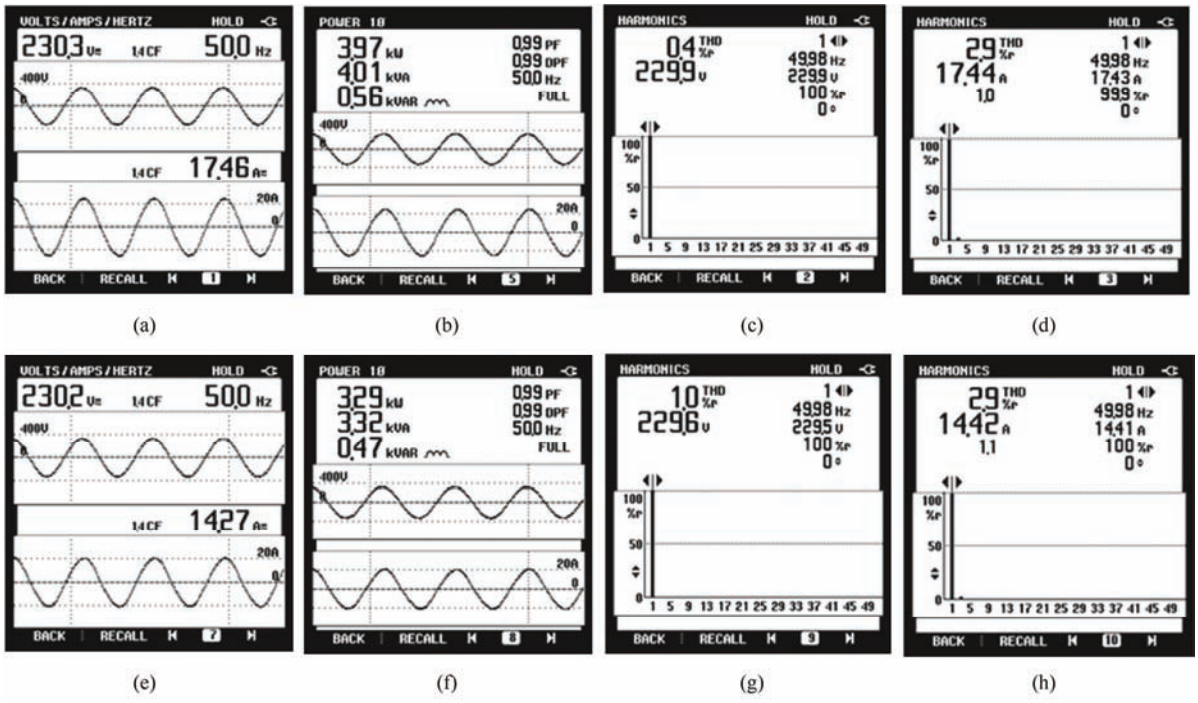



Fig. 9 Experimental waveforms of the voltages and currents of the dual battery charger in four different operating modes at a supply voltage of 230 V

Test results of the power quality analyzer shown in Fig. 10 demonstrate the supply voltage and current, active power, and reactive power at the supply side, and the THD of the supply voltage and current for the four different operating conditions: (a) CC-CC mode, (b) CC-CV mode, (c) CV-CC mode, and (d) CV-CV mode. Fig. 10a presents the results of when both batteries were operated in the CC mode. The peak input current was 17.4 A and 3.97 kW, and the THD values in the supply voltage and current were 0.4% and 2.9%, respectively, at a 230 V supply voltage.

Fig. 10b presents the results of when the HV battery was charging in the CC mode and the LV battery was charging in the CV mode. It indicates that the THD values for the supply voltage and current were 1% and 2.9%, respectively. Similarly, Fig. 10c presents the results of when both batteries were charged in the CV mode. The THD values of the supply voltage and current were 1% and 4.8%, as shown in Fig.10c. Fig. 10d presents the results for the HV battery charging in the CV mode and LV battery charging in the CC mode. The THD values of the supply voltage and current were 1% and 3.4%, respectively, as shown in Fig. 10d.



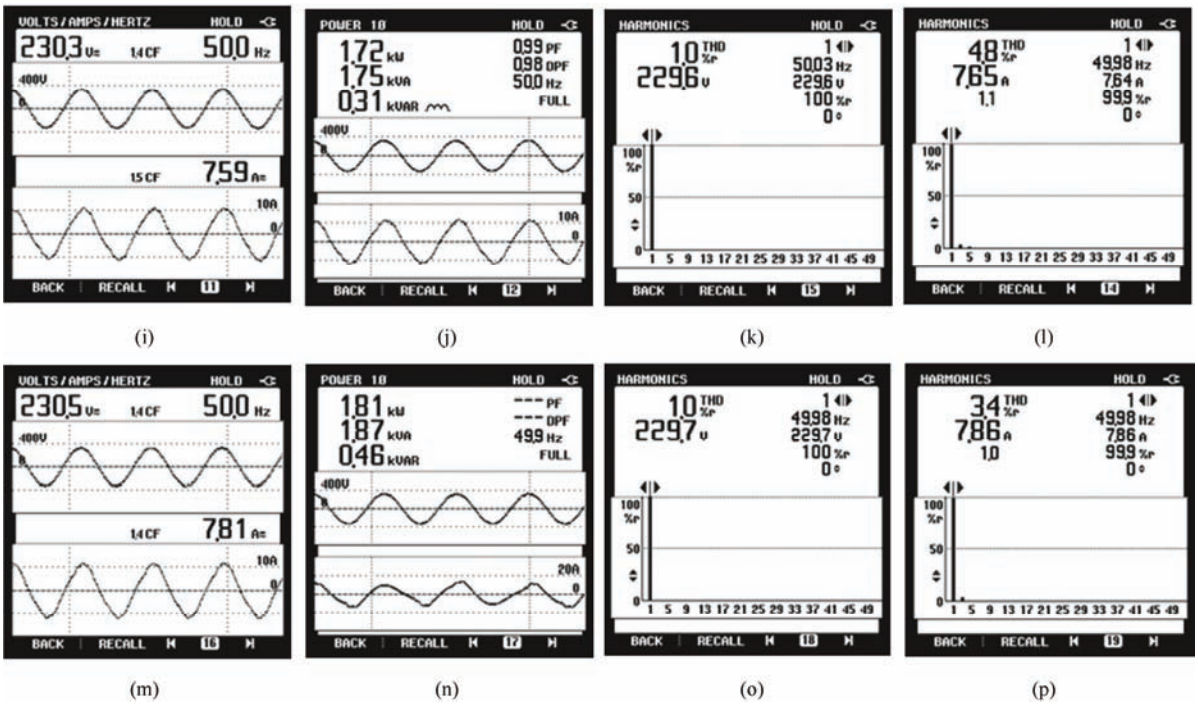
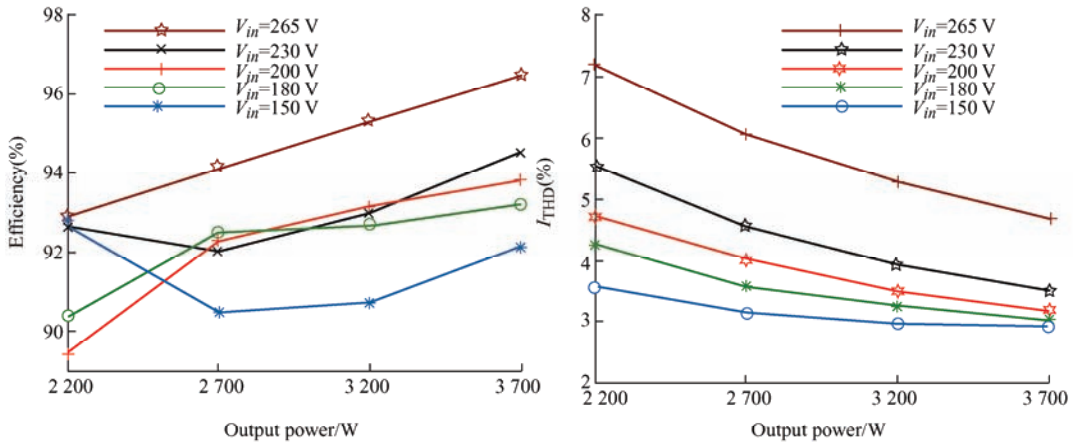



Fig. 10 Experiment results of the supply voltage and current, active and reactive power, THD(%) across the supply voltage, and current at the 230 V supply voltage in different operating modes

The performance of the proposed charging system is demonstrated in Fig. 11a and Fig. 11b with respect to the efficiency and input current THD.

Fig. 11a and Fig. 11b present the efficiency versus output power curve and THD versus output power curve, respectively, for a wide variation in the supply voltage (150-265 V). Fig. 11a and Fig. 11b present the system efficiency of 94.5% and input current THD of 3.67% at a 230 V supply voltage for the total HV- and LV-side output power of 3 700 W.




(a) Efficiency versus output power

(b) THD versus output power with a wide variation in the supply voltage (150-265 V)

Fig. 11 Performance graphs

### 6.3 Performance of the integrated boost-SEPIC fly-back converter-based dual battery charger

The proposed integrated system demonstrates an improved efficiency and satisfies the input current THD limit of the IEEE-519-2014 standard. Tab. 3 presents a comparison of the integrated SIDO with the individual converters with respect to the number of the component counts and their control sensor requirements, switch and diode stresses, losses, and efficiencies. The power quality indices with wide variations in the supply voltage of the proposed charger for four possible operating modes of the HV and LV batteries are listed in Tab. 4. At a nominal supply voltage of 230 V, Tab. 4 demonstrates that the power factor

approximate unity and THD in the supply current is less than 5% in the CC-CC and CC-CV modes.

**Tab. 3 Comparison of integrated SIDO converter with individual conventional converter**

| No. | Parameters | Individual conventional converter (SEPIC+BOOST+FLY-BACK) | Integrated SIDO converter |
|---|---|---|---|
| 1 | No. of components | 3 switches+3 diodes+3 inductors+4 capacitors | 2 switches+3 diodes+2 inductors+4 capacitors, lower component count (share common input inductor and input supply) |
| 2 | Input and output requirement | 3 inputs for 3 outputs individually | 1 input for 2 outputs |
| 3 | Control sensors requirement | 6 sensors (3 for sensing 3 output voltages regulation, and 3 current sensors for the PFC at input side) | 3 sensors (2 sensors for regulation of 2 output voltages and 1 current sensor for PFC with one output voltage at the input side). Here, no extra sensor requirement for PFC with the other output voltage. Easy control |
| 4 | HFT | HFT only used for fly-back output requirement, which is independent of the other two converter inputs and outputs. Therefore, HFT is not reliable | By adjusting the number of turns, HFT can adjust the output voltage according to the demand through the proposed topology. Therefore, it can also be used for EV auxiliary supply, and it is reliable |
| 6 | Switch & diode voltage stress (at 230 V supply voltage) | $V_{Sw1}=V_{o1}=400$ V (boost)<br>$V_{Sw2}=V_{in}+V_{dc}=406.5$ V (SEPIC)<br>$V_{Sw3}=V_{in}+V_{o2}\frac{N_1}{N_2}=460$ V (flyback)<br>$V_{d1}=-V_{o1}=-400$ V (boost)<br>$V_{d2}=-(V_{in}+V_{dc})=-406.5$ V (SEPIC)<br>$V_{d3}=-\left(V_{in}+V_{o2}\frac{N_2}{N_1}\right)=-373.75$ V (flyback) | $V_{Sw1}=V_{o1}=400$ V<br>$V_{Sw2}=V_{dc}+V_{o2}\frac{N_1}{N_2}=250$ V<br>$V_{d1}=-V_{o1}=-400$ V<br>$V_{d2}=-(V_{in}+V_{dc})=-406.5$ V<br>$V_{d3}=-\left(V_{dc}+V_{o2}\frac{N_2}{N_1}\right)=-129$ V |
| 7 | Efficiency | More switches, more switch stress; therefore, more switching losses and less efficiency | Less switches, less switch voltage stress; therefore, less losses and efficiency=95% with a wide input voltage variation (150-265 V) |
| 8 | THD | Less than 5% | Less than 5% for each operating mode |

**Tab. 4 Performance indices of the integrated dual battery charger at different operating modes**

| No. | Supply voltage/ V | Dual (HV and LV) batteries charging operation modes | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | CC-CC | | | CC-CV | | CV-CV | | CV-CC | |
| | | PF | $n$(%) | THD (%) | PF | THD(%) | PF | THD (%) | PF | THD(%) |
| 1 | 150 | 0.99 | 93.00 | 2.87 | 0.98 | 2.91 | 0.99 | 3.18 | 0.98 | 2.99 |
| 2 | 180 | 0.99 | 94.20 | 2.83 | 0.99 | 3.13 | 0.98 | 3.75 | 0.98 | 3.30 |
| 3 | 200 | 0.99 | 94.58 | 2.93 | 0.99 | 3.35 | 0.99 | 4.12 | 0.989 | 3.44 |
| 4 | 230 | 0.99 | 94.90 | 3.08 | 0.99 | 3.65 | 0.99 | 4.84 | 0.99 | 3.97 |
| 5 | 265 | 0.99 | 96.50 | 3.72 | 0.99 | 4.32 | 0.99 | 5.49 | 0.99 | 5.07 |

Tab. 3 presents the variation in efficiency with the variation in the input voltage for the CC-CC operating mode. It can be observed that the proposed charging system achieved a 95% efficiency at a 230 V nominal supply voltage.

## 7 Conclusions

In this study, an SIDO integrated converter was proposed for on-board dual EVs battery charging, capable of simultaneously charging both 2-wheeler and 4-wheeler batteries. In contrast to conventional converters, the proposed integrated converter provides a continuous input current and employs fewer components. Therefore, the proposed converter is more desirable for simultaneously charging the HV and LV batteries. Furthermore, the proposed integrated converter utilizes the common switch between the boost and SEPIC converters at the input side to

provide a power factor of unity, which eliminates the requirement of one current sensor for the PFC. This design approach enhances the compactness of the converter. In addition, the HFT used at the step-down side, connected through the SEPIC-fly-back converter to isolate the battery from the supply side, ensures a reliable and safe operation for a light EVs battery charging system. A wide range of supply voltages (150-265 V) was considered to ensure that the charger design was secure and consistent. The results were analyzed under steady-state and dynamic conditions using Matlab & Simulink, demonstrating an efficiency of 95% and an input current THD of less than 5%.

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