Stability Analysis and Efficiency Improvement of a Multi-converter System Using Multi-objective Decision Making

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Abstract: Multi-converter system is mainly used in advanced automotive systems. Different converters and inverters are taking part in automotive systems to provide different voltage levels in a multi-converter system. It involves constant voltage load (CVL), constant power load (CPL) and other loads. The CPL in such systems offers negative impedance characteristic and it creates a destabilizing effect on the main converter. The effect of destabilization can be reduced by increasing the CVL or inserting parasitic components. Attempts have been made by authors to improve the stability by using parasitics of different components such as switch, diode and inductor. Influence of insertion of parasitics including the series equivalent resistance of the filter capacitor and variation in CVL on the performance of main converter is mathematically analyzed and conflicting behavior between system stability and efficiency is observed. The optimum solution between these two functions is obtained by using multi-objective decision making (MODM) by varying parasitics of different components and CVL. An attempt has been made to demonstrate the effect of CVL load and the parasitics on the stability and efficiency of the main converter, experimentally.

Keywords: Multi-converter system, constant power load (CPL), stability, parasitic elements, efficiency and multi-objective decision making (MODM)

1 Introduction

A multi-converter system has number of power electronic converters based on the need of converters in automotive applications. Such systems are used in telecommunication, electric vehicles (EVs), hybrid electric vehicles (HEVs), modern aircraft, international space station (ISS), on sea and undersea vehicles, etc. They are mostly of the DC type and comprise several converters.

The block with dotted line in Fig. 1 shows a DC-DC converter (considered as the main converter in our work) supplying different types of loads, that is, CPL, CVL and other DC-DC converters operating with reduced voltage.

When tightly regulated power electronic converters are controlled to regulate the voltage in a multi-converter system shown in Fig. 1, they behave as constant power load (CPL). In addition, they offer negative impedance characteristic at the output terminal of the main converter. In such a load, the voltage and current at the converter input terminal are in inverse relation, leading to positive instantaneous impedance ($V/I > 0$) but negative incremental impedance ($\mathrm{d}V/\mathrm{d}I < 0$).

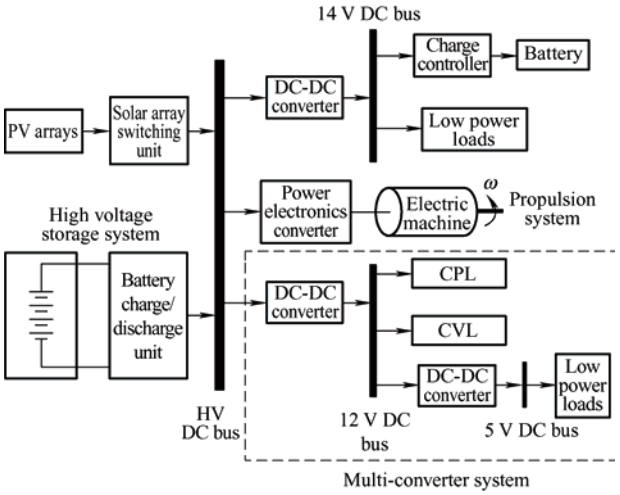

Fig. 1 A tightly regulated DC-DC converter supplied by the main DC-DC converter

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The destabilizing effect resulting from the negative impedance nature of CPL in a multi-converter system leads to instability of main converter, which has been addressed in Refs. [1-5]. The stability of DC-DC multi-converter system for DC distributed power system, telecom power supply system, electric vehicles, DC microgrid is analysed, reviewed and detailed by researchers [3, 6-7].

Some researchers have suggested relocating the poles from the right half to the left half of S-plane in Refs. [8-12] to make the system stable. Fundamentally, the systems loaded by CPL are unstable in open loop operation. It can be made stable by closing the loop. Several methods to obtain the stability of a main converter by closing the loop are suggested in Refs. [13-17]. It is suggested to obtain converter stability using the pole placement technique by shifting undesirable poles from the right half to the left half of S-plane [5, 13]. Various quantities such as output power, voltage, current and the states of system are used as feedback to obtain the stability. Current mode control is suggested for the main converter loaded by CPL in Ref. [14]. Stability is achieved with this technique by using peak current mode control and valley current mode control. The pulse alignment technique discussed in Ref. [15] entails regulating the output voltage of the main converter by tracking the output voltage from low to high output power as shown in Fig. 2a. The Power alignment control method using state space averaging is discussed in Ref. [16]. This technique suggests duty ratio control using power as a feedback quantity to control output voltage of CPL loaded main converter as shown in Fig. 2b.

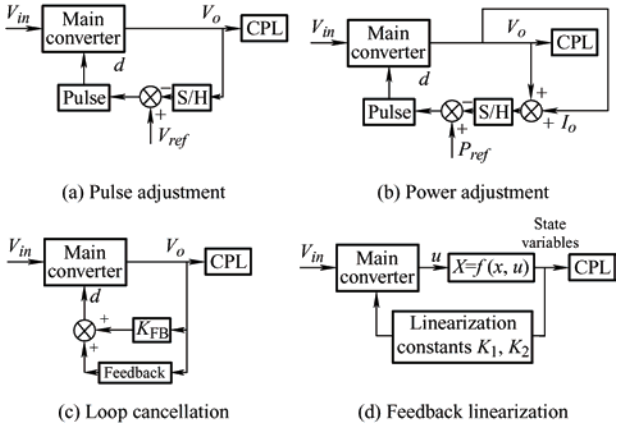


Fig. 2 Various closed-loop control methods to make a system stable

The method of loop-cancellation is discussed in Refs. [12, 17] for enhancing the stability of conventional DC-DC converters loaded by CPL. The tuning of feedback gain by introducing a feedback loop in the system to shift poles in left hand side of the S-plane by eliminating the CPL loop as shown in Fig. 2c. In Ref. [18], an attempt is made to stabilize the converter loaded with CPL using feedback linearization technique. The feedback of state variables is utilized to achieve the system stability by taking corrective actions, as shown in Fig. 2d. However, this technique is sensitive to load variation and the system may lose stability because it is designed with a fixed load consideration. A method to analyze and control the converter loaded by CPL using sliding mode control and feedback linearization technique have been presented in Ref. [2]. In this technique system, stability is improved by the large-signal phase plane analysis. It is claimed in Ref. [8] that the sliding mode duty ratio controller make the system stable, even under significant variation in source voltage and load.

The instability originated owing to CPL loads in the DC microgrid is analyzed in Ref. [19], and optimal placement of CPL at different buses have been obtained using particle swarm optimization technique. The instability resulting from CPL is addressed for DC-DC converter in Ref. [20] and an immersion and invariance parameter estimator technique was proposed to solve the same problem. In Refs. [21-22], the impacts of instability in more electric aircraft (MEA) and DC microgrids are studied. The novel droop controller technique is utilized to take care of instability issues in more electric aircraft (MEA) and DC microgrids resulting from CPL loads.

The robust controllers are studied and utilized to overcome the instability problem in multi-converter system [23]. The negative instability behaviour due to CPL is studied in Ref. [24] and the researchers suggested utilizing the v^2-P droop control technique to eliminate instability due to CPLs. The virtual resistance damping technique is used in Ref. [25] to overcome the stability issue of the bipolar DC systems loaded with CPL.

In Ref. [1], the necessary and sufficient conditions

are obtained for stability of a buck converter supplying a CPL and a CVL. In many cases, an ideal lossless model is assumed for the stability analysis, whereas here the parasitic effects of components are considered for model precision and the system is analysed in Refs. [9, 26]. The state space averaged model for main converter with CVL and parasitics are derived in Ref. [9]. It is observed that the parasitics of the converter components improves the system stability. The enhancement in converter stability is studied mathematically for the buck converter supplying both CVL and CPL considering parasitic effect in Ref. [26]. The control-to-output transfer functions have been obtained for continuous conduction mode (CCM) and discontinuous conduction mode (DCM) modes to address the problem of stability.

In Refs. [10-11], the parasitics of inductor and capacitor playing an important role in shifting the poles in left half of the S-plane to stabilize the system were analyzed. In Ref. [10] the capacitor parasitic resistance r_{Cf} is considered and it is evaluated that it adds a zero in right half of the S-plane. The stability of a main converter is analyzed for resistive load using transfer function approach with consideration of capacitor parasitic in Ref. [11]. In this case, the dynamic response is verified for converter operation in CCM. In Ref. [27], the researchers presented the study and analysis of the effect of components' (diode, switch, inductor and capacitor) parasitics on system stability and stated that the influence of capacitor parasitic r_{Cf} is more compared to other system parasitics on system stability.

In this paper, it is attempted to analyse and study the effect of parasitic elements including r_{Cf} on efficiency and stability of a buck converter operated in open loop loaded by CPL and CVL. Both system stability and efficiency are mathematically analyzed by considering the parasitics of diode, switch, inductor and capacitor. Since parasitic elements are lossy components, system efficiency is compromised while attempting to improve the stability. It raises conflicting behaviour of the system and demands to find trade-off between the efficiency and stability of main converter. In this work optimum operating conditions are obtained using multi-objective decision making (MODM) technique.

The paper is structured as follows: Section 2 presents the stability analysis of the buck converter. Section 3 analyses DC-DC converter loaded by CPL with parasitics of diode, switch, capacitor and inductor operated in CCM. Section 4 presents the proposed method using MODM to obtain optimum values of CVL and parasitic elements to determine trade-off between two conflicting objective functions of stability and efficiency. The experimental investigation is given in Section 5. Finally, the conclusions are drawn and presented in Section 6.

2 Stability analysis of buck converter considering parasitics of components loaded by CPL in parallel with CVL

In this work, an attempt has been made to analyse the parasitics effect of circuit components and CVL on system stability. Further analysis has been done to explore the individual effect of parasitic elements. This is done to determin which element can provide better stability without compromising much on the efficiency.

In this study, in addition to r_Q, r_D, and r_L the equivalent series resistance r_C of the capacitor is also considered for stability analysis. Fig. 3 shows the system with parasitics elements r_Q, r_D, and r_L along with r_C. As a result, the output voltage and capacitor voltage are not the same. Thus the output equation is given by

$$v_o = v_{C_f} + r_{C_f}\left[i_{L_f} - \frac{P}{v_o} - \frac{v_o}{R}\right] \tag{1}$$

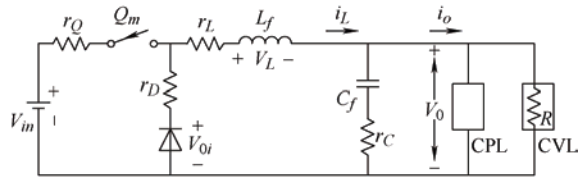


Fig. 3 The main converter loaded by CPL in parallel with a CVL with all parasitic elements

Small disturbances are considered in duty ratio $d = D + \hat{d}$, output voltage ($v_o = V_o + \hat{v}_o$) and state variables ($i_{L_f} = I_{L_f} + \hat{i}_{L_f}$, $v_{L_f} = V_{L_f} + \hat{v}_{L_f}$) for the small-signal analysis of the converter. To simplify the analysis, no perturbation is assumed in input voltage ($\tilde{v}_{in} = 0$), and hence $v_{in} = V_{in}$. The average values of duty ratio d and output voltage v_o are D and V_o, respectively; $\tilde{d}$ and $\tilde{v}_o$ are small signal variations of

d and v_o respectively. With these assumptions, Eq. (1) can be modified as follows

$$\tilde{v}_o = \frac{r_{C_f}}{1-\frac{P}{V_o^2}r_{C_f}+\frac{r_{C_f}}{R}}\tilde{i}_{L_f} + \frac{1}{1-\frac{P}{V_o^2}r_{C_f}+\frac{r_{C_f}}{R}}\tilde{v}_{C_f} \quad (2)$$

The control-to-output transfer function of the system considering CPL-CVL, parasitic resistances r_Q, r_D, r_L, and r_C can be derived as

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{K(s+K_1)}{s^2+K_2 s+K_3} \quad (3)$$

where

$$K = \left[\left(\frac{r_D-r_Q}{L_f}\right)I_{L_f}+\frac{v_{in}}{L_f}\right]\left(\frac{r_C}{1-\frac{Pr_C}{V_o^2}+\frac{r_C}{R}}\right)$$

$$K_1 = \frac{1}{r_C C_f\left(1-\frac{Pr_C}{V_o^2}+\frac{r_C}{R}\right)} - \frac{\frac{P}{V_o^2}-\frac{1}{R}}{C_f\left(1-\frac{Pr_C}{V_o^2}+\frac{r_C}{R}\right)}$$

$$K_2 = \frac{1}{L_f}\left(\mu+\frac{r_C}{1-\frac{Pr_C}{V_o^2}+\frac{r_C}{R}}\right) - \frac{\frac{P}{V_o^2}-\frac{1}{R}}{C_f\left(1-\frac{Pr_C}{V_o^2}+\frac{r_C}{R}\right)}$$

$$K_3 = \frac{1}{L_f C_f\left(1-\frac{Pr_C}{V_o^2}+\frac{r_C}{R}\right)^2} - \frac{1}{L_f}\left(\mu+\frac{r_C}{1-\frac{Pr_C}{V_o^2}+\frac{r_C}{R}}\right)\left(\frac{\left(\frac{P}{V_o^2}-\frac{1}{R}\right)}{C_f\left(1-\frac{Pr_C}{V_o^2}+\frac{r_C}{R}\right)}\right)$$

$$\mu = r_L + Dr_Q + (1-D)r_D$$

The roots of transfer function Eq. (3) are located in the left-half of the S-plane. It indicates that the system is stable. By applying R-H criteria to Eq. (3), the maximum value of stability P_{st} is derived and is given by

$$P_{st} < \frac{\left[\left(\frac{r_D-r_Q}{L_f}\right)I_{L_f}+\frac{V_{in}}{L_f}\right]r_C V_o^2 C_f + \frac{V_o^2}{R} + \frac{\mu V_o^2 C_f}{L_f} + \frac{r_C \mu V_o^2 C_f}{L_f R} + \frac{r_C V_o^2 C_f}{L_f}}{1+\frac{r_C \mu C_f}{L_f}} \quad (4)$$

The effect of variation in parasitic r_Q, r_D, r_L, and r_C on the stability region of the main converter loaded by CPL in parallel with CVL is verified through simulation study using Matlab/Simulink and results are presented in Fig. 4. The specification of the main converter, CPL and CVL considered for analysis are given in Tab. 1.

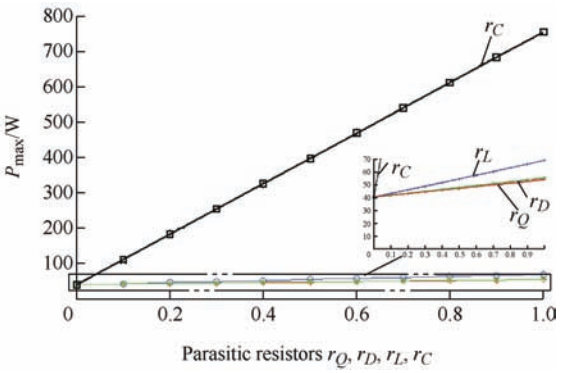


Fig. 4 Stability region of buck converter loaded with CPL-CVL with parasitics r_Q, r_D, r_L, and r_C

Tab. 1 Specification of buck converter

Parameter	Value
Input voltage V_{in} and output voltage V_o/V	24, 12
Total output power P_o/W	100
Rated output of CPL P_{CPL} and CVL P_{CVL}/W	50, 40
Inductor L_f/μH	504
Capacitor C_f/μF	100
Switching frequency f_s/kHz	20
ON-state drain-to-source resistance of the device R_{DSON}/Ω	0.044
ON-state resistance of diode R_{FD}/Ω	0.067 5
Inductor resistance R_{DCR}/Ω	1.945 6
ON-state resistance of capacitor r_C/Ω	0.017 5

Variation in the r_Q, r_D, r_C, and r_L can be realized by connecting control switches Q_Q, Q_D, Q_L, and Q_C across each parasitic elements. It is found that r_L and r_C can be varied independent of main switch duty ratio D and it is discussed in detail in Ref. [27].

The effect of variation in r_Q, r_D, r_L, and r_C on system stability is also studied, and the results are presented in

Fig. 4. Though variation in r_C offers a larger stability region compared to that of its peers, it is not preferable to vary r_C for the following reasons: ① A high level voltage ripple present in the output voltage of main converter which may lead to high frequency component in input voltage to CPL, and ② zero is added to the right half of the S-plane, which may increase the system's internal instability. Consequently, by considering these conditions, it is preferable to fix the value of r_C to its internal value and control the effective value of r_L, i.e., r_{Leff}. Therefore, r_Q= R_{DSON}, r_D= R_{FD}, r_C= R_{esr} and r_L= R_{DCR}+ r_{Lext} are considered in further analysis, where r_{Lext} is the inductor external resistance connected in series. System stability can be demonstrated by observing movement of poles in the S-plane. It is clearly observed from the zoomed portion shown in Fig. 5 that the poles of transfer function with only P_{CPL}= 75 W are located in the right half of S-plane, which is responsible for system instability. The exact position of pole can also be identified from Tab. 2. Parasitic of system components and P_{CVL} help the system become stable by shifting the poles of the systems to left half of S-plane.

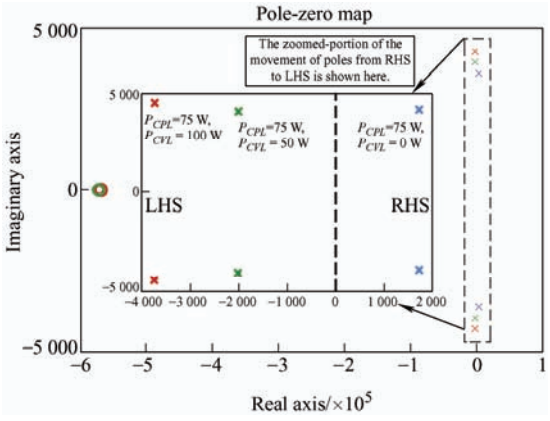


Fig. 5 Pole-zero location for different values of P_{CVL} with constant P_{CPL}

Tab. 2 Pole-zero location for different values of P_{CVL}

Type of loads	Poles of transfer function	Zeros
Only P_{CPL}	$1.0\times10^3\times(1.736\ 1+4.102\ 1i)$ $1.0\times10^3\times(1.736\ 1-4.102\ 1i)$	—
CPL with P_{CVL}=50 W and all parasitics	$1.0\times10^3\times(-2.002\ 8+3.978\ 7i)$ $1.0\times10^3\times(-2.002\ 8-3.978\ 7i)$	$5.714\ 3\times10^5$
CPL with P_{CVL}=100 W and all parasitics	$1.0\times10^3\times(-3.728\ 3+4.418\ 8i)$ $1.0\times10^3\times(-3.728\ 3-4.418\ 8i)$	$5.714\ 3\times10^5$

The higher the value of P_{CVL}, the greater is system stability. The value of P_{CVL} and paracitics are mainly responsible for improvement in stability of system and this requires a study of converter efficiency resulting from the insertion of additional resistance. The effect of presence of parasitic on efficiency and loss calculation of main converter loaded with CPL and CVL is presented in the next section.

The above explanation clearly indicates that the stability limit obtained due to parasitics is appreciable, but considering the parasitics in the system leads to losses in the system. This demands a study of converter efficiency and losses due to insertion of extra resistance. Considering the CPL and CVL applied to main converter, the effect of presence of parasitic on efficiency and loss calculation of main converter is presented in next section.

3 Analysis and conflict behavior between efficiency and stability

The equations for converter losses and efficiency are derived in this section. It is found that the functional behavior of efficiency and stability are conflicting.

3.1 Efficiency and loss calculation of buck converter

The average power dissipated in the parasitic elements of device, diode, inductor and capacitor can be obtained as

$$P_Q = r_Q(D)\left(I_{L_f}^2\right) \tag{5}$$

$$P_D = r_D(1-D)\left(I_{L_f}^2\right) \tag{6}$$

$$P_L = r_L\left(I_{L_f}^2\right) \tag{7}$$

$$P_C = r_C\left(I_{C_f}^2\right) \tag{8}$$

where, i_{L_f} and i_{C_f} are the average inductor current and RMS capacitor current, respectively. Considering the average inductor current instead of RMS value is a fair approximation and is verified mathematically. This is possible because of the CCM operation and negligible ripple.

The total power dissipated in device, diode, inductor and capacitor is given by

$$P_T = P_Q + P_D + P_L + P_C = I_{L_f}^2 \times \left[r_L + D\left(r_Q - r_D\right) + r_D\right] + I_{C_f}^2 \times r_C \tag{9}$$

For any output voltage, the equation of converter efficiency can be written as

$$\eta = \frac{P_0}{P_0 + P_T} = \frac{P_{CPL} + P_{CVL}}{P_{CPL} + P_{CVL} + I_{L_f}^2 \times \left[r_L + D\left(r_Q - r_D\right) + r_D \right] + I_{C_f}^2 \times r_C} \tag{10}$$

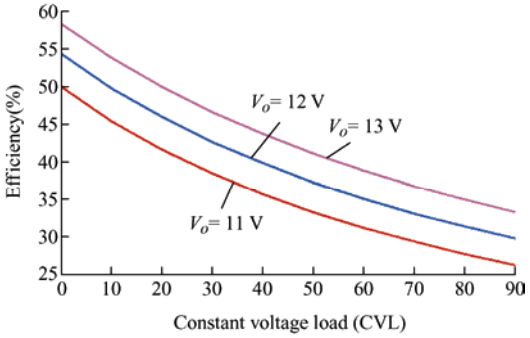
From the above analysis, it can be observed that the system performance in terms of stability and efficiency are affected by the parasitics. System stability is improved by increasing r_L but at the cost of efficiency. Furthermore, system efficiency and stability are also affected by variation in P_{CVL}. Consequently, to obtain the optimum performance of the main converter, it is essential to find out tradeoff between variation in P_{CVL} and r_L at given operating point, as discussed in the next section.

3.2 Analysis of buck converter for stability and efficiency considering parasitics, P_{CVL} and r_L

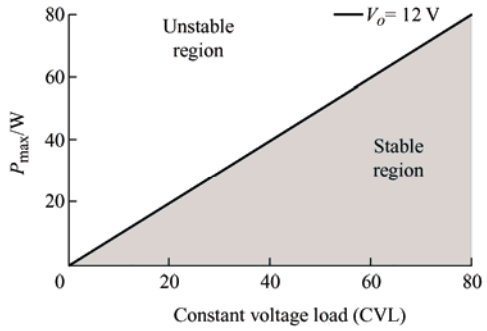
In this paper, it is attempted to analyze effect of parasitic elements r_Q, r_D, r_L, r_C and P_{CVL} on the main converter's performance in terms of efficiency and stability. As in the previous section, the values of r_Q, r_D and r_C are fixed to R_{DSON}, R_{FD} and R_{esr} respectively. Based on the variation in P_{CVL} and r_L, the main converter efficiency and stability are analyzed for the effect of (i) the variation in P_{CVL}, considering r_L constant (ii) the variation in r_L, considering P_{CVL} constant.

3.2.1 Effect of variation in P_{CVL} while considering r_L as constant

The system efficiency and stability analysis are done by increasing P_{CVL} and keeping r_Q, r_D, r_L, and r_C fixed. The results are plotted in Fig. 6a and Fig. 6b, respectively. It is observed that the increase in P_{CVL} reduces the efficiency, but it improves the system stability, and hence, the conflicting nature in terms of efficiency and stability is reflected.



(a) Efficiency by varying P_{CVL} keeping r_L constant



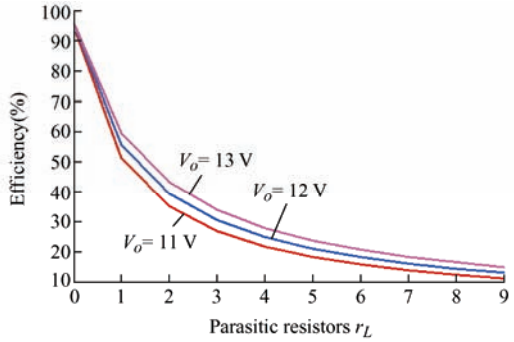
(b) Stability by varying P_{CVL} keeping r_L constant

Fig. 6 Efficiency and stability analysis of the main converter

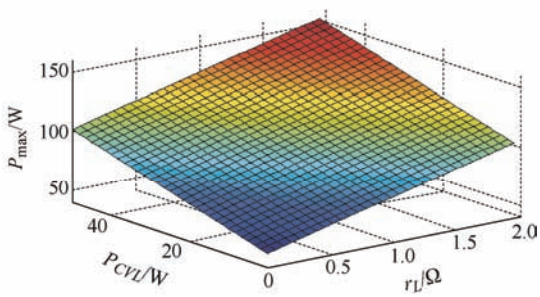
3.2.2 Effect of varying parasitic element r_L while considering constant P_{CVL}, r_Q, r_D and r_C

Similar analysis has been performed for variation in r_L while keeping P_{CVL}, r_Q, r_D and r_C fixed. The result in previous section shows that the system stability is improved by increasing r_L, at the same time, the conflicting nature is observed on system efficiency showing decreasing trend as shown in Fig. 7a. It is mainly due to the occurrence of losses resulting from the insertion of resistance in the circuit. Therefore, it is concluded that increasing the value of r_L improves the system stability but at the cost of efficiency.

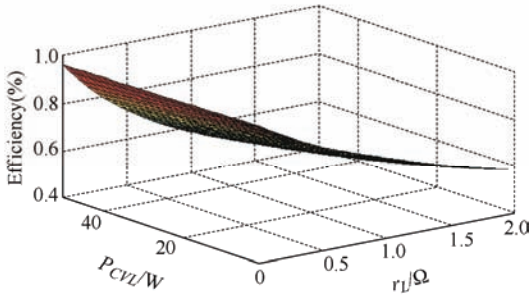
System stability and efficiency are analyzed for a wide range of variation in P_{CVL} and r_L. Figs. 7b and 7c show the surface plot of stability and efficiency, respectively. The improvement in system stability and decrement in the efficiency with the P_{CVL} and r_L can be clearly observed. This conflicting trend in system efficiency and stability evokes the idea to find a tradeoff between the two. The use of multiple objective functions to determine the optimum condition for selection of P_{CVL} and r_L is discussed in the following section.



(a) Efficiency when r_D, r_Q, and r_C are fixed



(b) Stability surface for V_o=12 V



(c) Efficiency surface for V_o=12 V

Fig. 7 Main converter performance

4 Proposed method

The MODM problem mainly address different objectives as a function of various alternatives. Basically, MODM optimization technique is used to obtain optimal decision for trade-offs between two or more conflicting objectives. It basically requires information of multiple conflicting objectives and a set of objective constraints. By using these information, MODM can be implemented in any system to obtain optimum solution [28-31].

Mathematically, the MODM problem is defined as follows

$$\begin{cases} \min\ f_i(\boldsymbol{X}) & i=1,2,\cdots,n \\ \text{s.t. } g_j(\boldsymbol{X}) \leqslant 0 & j=1,2,\cdots,m \end{cases} \tag{11}$$

where $f_i(\boldsymbol{X})$ is ith objective function, $g_j(\boldsymbol{X})$ are constraints and $\boldsymbol{X}$ is decision vector.

Global criterion method (GCM) is one of the approaches to formulate the global objective functions. Here, the global objective function is formulated to obtain an optimum solution in this work. The optimum solution $\boldsymbol{X}^*$ is determined by minimizing a preselected global criterion in the GCM. The preselected global criterion $F(X)$ is minimized such that the sum of the squares of the relative deviations of the individual objective functions from the feasible ideal solution can be minimized. Therefore, $\boldsymbol{X}^*$ is determined by minimizing

$$F(X)=\sum_{i=1}^{k}\left\{\frac{f_i(x_i^*)-f_i(x)}{f_i(x_i^*)}\right\}^2$$
$$\text{s.t. } g_j(X)\leqslant 0 \quad j=1,2,\cdots,m \tag{12}$$

where, k is the number of objectives, $f_i(\boldsymbol{X})$ is the ith objective function and x_i^* is the ideal solution for the ith objective function.

The solution x_i^* is achieved by minimizing $f_i(x)$ subject to the constraints $g_j(x)\leqslant 0$ where $j=1,2,\cdots,m$ [31]. In GCM technique, it is essential to obtain global optimization function. It can be achieved by combining multiple objectives into a single objective function.

An attempt has been made in this work to minimize the conflicting nature of objective functions of efficiency and stability. These objective functions with alternatives P_{CVL} and r_L are given by

$$f_1=\frac{P_{CPL}+x_1}{P_{CPL}+x_1+I_{L_f}^2\left(x_2+D\left(r_Q-r_D\right)+r_D\right)+I_C^2 r_C} \tag{13}$$

$$f_2=\frac{\left\{\left(\frac{r_D-r_Q}{L_f}\right)I_{L_f}+\frac{V_{in}}{L_f}\right\}r_C V_o^2 C_f+x_1+\frac{\mu_s V_o^2 C_f}{L_f}+\frac{r_C\mu_s V_o^2 C_f}{L_f R}+\frac{r_C V_o^2 C_f}{L_f}}{1+\frac{r_C\mu_s C_f}{L_f}}$$
$$\text{s.t.}\quad x_1\leqslant P_{CVL\max} \text{ and } r_{L\min}\leqslant x_2\leqslant r_{L\max} \tag{14}$$

where, f_1 is the objective function of system efficiency, f_2 is the objective function of stability limit, $I_L=I_o=\frac{P_{CVL}+x_1}{V_0}$, $I_C=\sqrt{\frac{\Delta I_L^2}{12}}$ and $\mu_s=x_2+Dr_Q+(1-D)r_D$.

The main converter is expected to remain stable within its operating range for all operating points. Because the converters supply both CVL-CPL loads and the system instability is causes by the CPL load, here it is assumed that the main converter is supplying with a fixed 50% capacity of CPL and the rest of the

power is utilized for supplying the CVL. Therefore, the maximum power of CVL is given by

$$P_{CVL\max} = P_0 - P_{CPL} \tag{15}$$

It is already discussed that the consideration of capacitor parasitic makes the system stable. Let P_C be the stability due to r_C with r_L=R_{DCG}, r_Q=R_{DSON}, r_D=R_{FD} and is given by Eq. (16).

$$P_C = \frac{\left[\left\{\frac{(r_D - r_Q)}{L_f} I_{L_f} + \frac{V_{in}}{L_f}\right\} V_o^2 C_f + \frac{V_o^2 C_f}{L_f} + \frac{\mu C_f P_{CVL}}{L_f}\right] r_C}{1 + \frac{r_C \mu C_f}{L_f}} \tag{16}$$

From Tab. 3, it is observed that the change in P_C is very small for the entire range of P_{CVL}, i.e., from P_{CVL}=0 to P_{CVL}= $P_{CVL\max}$. This supports the conclusion r_C fixed at r_C=R_{esr}.

Now the remaining stability requirement can be obtained by controlling P_{CVL} and r_L. Considering the worst case condition (i.e., P_{CVL}=0), the maximum value of r_L can be obtained using Eq. (17).

$$r_{L\max} = \frac{P_{con} - P_{CVL\min} - \left[(r_D - r_Q) I_{L_f} + V_{in} + 1\right] \frac{V_o^2 r_C C_f}{L_f}}{r_C C_f P_{con} + P_{CVL\min} r_C C_f + C_f V_o^2} - r_D(1-D) - D r_Q \tag{17}$$

Similarly, considering the best case condition (P_{CVL}= $P_{CVL\max}$), the minimum value of r_L is obtained using Eq. (18).

$$r_{L\min} = \frac{P_{con} - P_{CVL\max} - \left[(r_D - r_Q) I_{L_f} + V_{in} + 1\right] \frac{V_o^2 r_C C_f}{L_f}}{r_C C_f P_{con} + P_{CVL\max} r_C C_f + C_f V_o^2} - r_D(1-D) - D r_Q \tag{18}$$

$$F = \left(\frac{f_{1\max} - f_1}{f_{1\max}}\right)^2 + \left(\frac{f_{2\max} - f_2}{f_{2\max}}\right)^2 \tag{19}$$

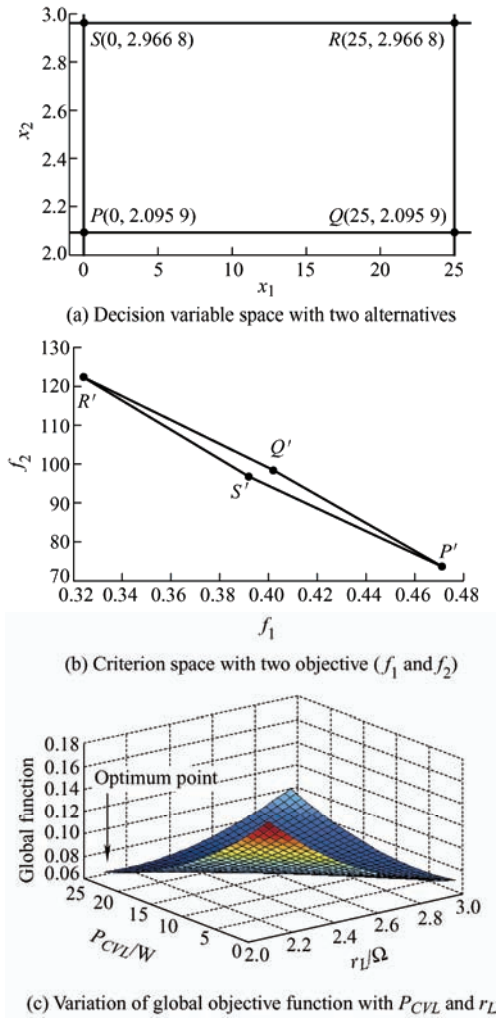
The optimum solution using GCM can be obtained by performing three steps: ① obtaining an ideal solution, ② creating a payoff table, and ③ obtaining the preferred solution.

Tab. 3 Variation of P_C for different values of P_{CVL}

P_{CVL}	r_Q	r_D	r_L	P_C
0	1.945 6	0.067 5	0.044	42.187 5
$P_{CVL\max}$	1.945 6	0.067 5	0.044	43.350 9

4.1 Obtaining the ideal solution

The maximum values of objective functions f_1 and f_2 for given constraints are obtained by plotting, x_1 vs x_2 in a decision variable space as shown in Fig. 8a. The points obtained are P(0,1.230 1), Q(50,1.230 1), R(50,2.966 8) and S(0, 2.966 8). The values of objectives f_1 and f_2 are obtained by substituting these points into Eqs. (13) and (14) and are given in Tab. 4.



(a) Decision variable space with two alternatives

(b) Criterion space with two objective (f_1 and f_2)

(c) Variation of global objective function with P_{CVL} and r_L

Fig. 8 MODM analysis between two conflicting functions r_L

Tab. 4 Objective functions values at decision points

Function	P	Q	R	S
f_1	0.691 4	0.528 3	0.322 7	0.487 9
f_2	49.061 8	99.109 5	147.921 3	97.873 9

4.2 Creating the payoff table

The data in Tab. 3 were utilized to map the solution into the criterion space, the plot is presented in Fig. 8b. Points P', Q', R' and S' in criterion space indicate the value of objective f_1 and f_2, respectively.

Objectives f_1 and f_2 are maximum for the constraint points $P(0,0)$ and $R(50, 1.594\ 2)$, respectively, as shown in Fig. 8c.

The optimum solution is obtained for full range of r_L and P_{CVL} and it is shown in Fig. 9. In correspondence with the optimum value of r_L, P_{CVL}, efficiency and stability for different output voltage of the main converter, the change in position of global point is tabulated in Tab. 5.

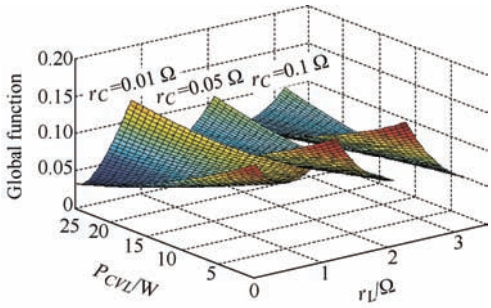


Fig. 9 Variation of global objective function with P_{CVL} and r_L for different value of r_C

Tab. 5 Optimum solution for various output voltage of the main converter

Output voltage v_o/V	Global point	Possible solutions	Optimum value r_L	Optimum value P_{CVL}	Efficiency	Stability
10	0.075 9	1	1.263 9	50	0.234 4	97.756 7
11	0.068 7	1	0.633	50	0.314 7	98.186 7
12	0.060 7	1	0.266 3	50	0.388 4	101.779 6

Here it can be observed that the system operates near the nominal output voltage (v_o=12 V), the optimum point moves towards $P_{CVL\max}$ and $r_{L\min}$. Furthermore, owing to reduction in r_L, the efficiency of the system increases without significantly affecting the system stability. It means, the system efficiency is greater when the output voltage of the system attains its nominal value.

The effect of change in capacitor parasitic r_C is also verified for the full range of r_L and P_{CVL}. Here the output voltage remaines unchanged. The results for different values of r_C are listed in Tab. 6 and are shown in Fig. 9. It appears that the efficiency increases with increasing r_C, however, the fact is that the increase in r_C pushes the global minimum towards $r_{L\min}$, thereby considerably reducing the losses.

Tab. 6 Optimum solution for the same value of C_f with different parasitic values

Capacitor parasitic	Global point	Possible solutions	Optimum value r_L	Optimum value P_{CVL}	Efficiency	Stability
0.017 5	0.060 7	1	2.211 9	50	0.388 4	101.779 6
0.035	0.056 2	1	1.693 9	50	0.451 5	99.275 4
0.052 5	0.050 4	1	1.247	50	0.525 1	99.003 2
0.07	0.043 5	1	0.784 6	50	0.631 6	98.536 0

An attempt has been made to experimentally demonstrate the effect of CVL load and parasitics on the stability and efficiency of the main converter. Details of the hardware and experimental results are presented in the following section.

5 Experimental investigation

A prototype of a multi-converter system was implemented with a 24 V input and 12 V output. In this system, the main converter is a buck converter loaded with a tightly regulated converter that behaves as CPL load. In addition, the main converter is loaded with CVL load. Fig. 10 shows the circuit of the multi-converter prototype. The system specifications for experimental work are listed in Tab. 7.

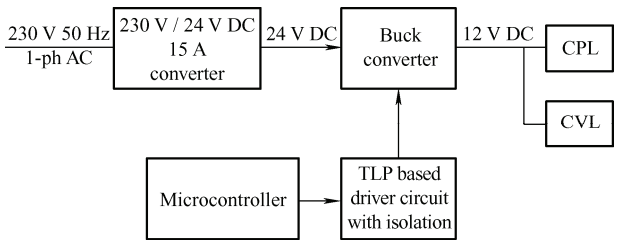


Fig. 10 Main converter loaded with CPL and CVL in multi-converter system

Tab. 7 Buck converter specification used for the experimental investigation

Parameter	Value
Input voltage V_{in} and output voltage V_o/V	24, 12
Total output power P_o/W	40
Rated output of CPL P_{CPL} and CVL P_{CVL}/W	12, 30
Inductor L_f/μH	504
Capacitor C_f/μF	100
Switching frequency f_s/kHz	20
ON-state drain-to-source resistance of the device R_{DSON}/Ω	0.044
ON-state resistance of diode R_{FD}/Ω	0.067 5
Inductor resistance R_{DCR}/Ω	0.335
ON-state resistance of capacitor r_C/Ω	0.017 5

In a practical circuit, gate pulses for main converter are generated using a microcontroller programmed to generate pulse-width modulation (PWM) switching pulses with an adjustable duty ratio for the main converter. The TLP 250 based isolation and driver circuit provide the isolation and amplify the PWM pulses, respectively, to drive the device with ±12 V. The experimental setup of the above system is shown in Fig. 11.

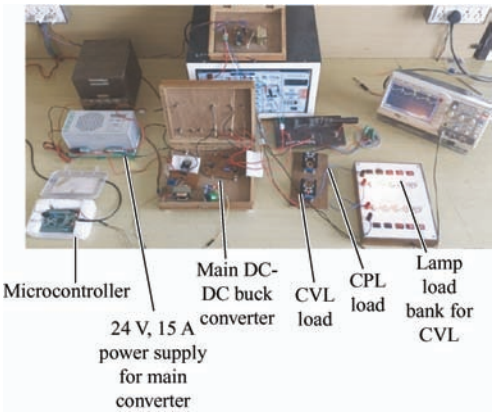


Fig. 11 Practical implementation of a multi-converter system

The converter is loaded with a CPL load and a CVL load. The tightly regulated converter act as a CPL, delivering the fixed load of 10 W. The CVL delivers load in the range of 5 W to 30 W. The experimental investigation the characteristic of the CPL load and the stability of the system has been conducted, and the results are presented in Tab. 8 and Tab. 9, respectively.

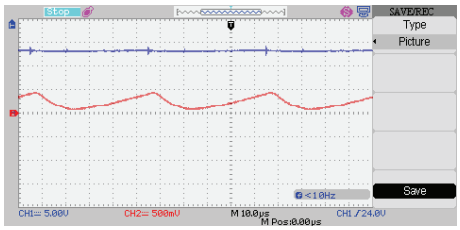
Tab. 8 Efficiency calculation for main converter

No.	P_{CVL}/W	V_o/V	I_{CVL}/A	I_{CPL}/A	$I_0=I_{CP}+I_{CVL}$/A	V_{in}/V	I_{in}/A	$P_o=V_oI_o$/W	$P_{in}=V_{in}I_{in}$/W	Efficiency
1	30.72	9.6	3.2	1.1	4.3	24	3.9	41.28	93.6	0.44
2	30.45	10.5	2.9	1.01	3.91	24	3.5	41.05	84	0.48
3	28.8	11.52	2.5	0.9	3.4	24	3.2	39.1	76.8	0.51
4	27.01	12.3	2.2	0.85	3.05	24	2.7	37.51	64.8	0.57
5	26	13	2	0.8	2.8	24	2.4	36.4	57.6	0.63
6	23.63	13.9	1.7	0.76	2.46	24	2.0	34.19	50.4	0.67
7	15.7	14.4	1.3	0.71	2.01	24	1.7	28.94	40.8	0.71
8	13.77	15.3	0.9	0.66	1.56	24	1.3	23.80	31.2	0.76

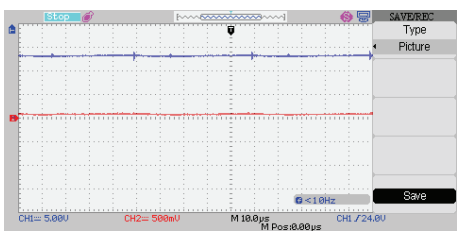
Tab. 9 Stability calculation for main converter

No.	P_{CVL}/W	V_o/V	$f(P_{CVL})$/W	$f(r_L)\|_{vo(fixed)}$/W	Stability= $f(P_{CVL})+f(r_L)$
1	30.72	9.6	30.72	15.19	45.91
2	27.32	10.5	27.32	18.15	48.60
3	26.39	11.52	26.39	21.82	50.62
4	26.7	12.3	26.7	24.84	51.90
5	23.28	13	23.28	27.73	53.73
6	19.03	13.9	19.03	31.66	55.29
7	10.71	14.4	10.71	33.95	52.67
8	6.29	15.3	6.29	38.28	52.05

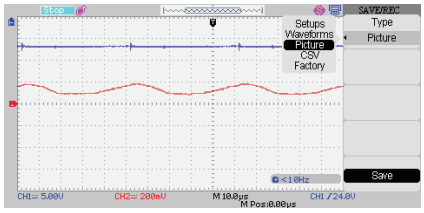
Fig. 12a presents the inductor current with output voltage V_o=13.6 V. Fig. 12b shows the current drawn by CPL load and Fig. 12c shows the current drawn by the CVL load. Fig. 13 shows another set of readings for increased P_{CVL}. In both cases, the product of the current drawn and the terminal voltage remains the same, manifesting the characteristic of a CPL load.



(a) Inductor current of main converter

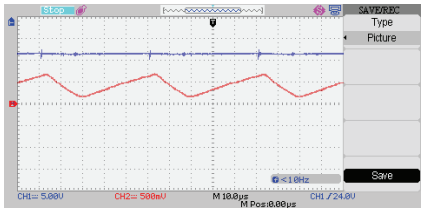


(b) Current drawn by CPL load

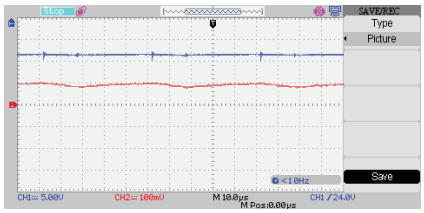


(c) Current drawn by CVL load

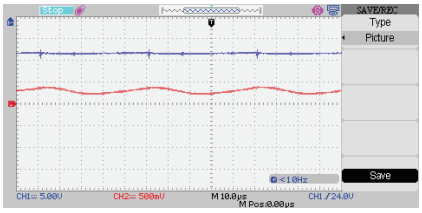
Fig. 12 Main converter performance at V_o =13.60 V



(a) Inductor current of main converter



(b) Current drawn by CPL load



(c) Current drawn by CVL load

Fig. 13 Main converter performance at V_o =11.52 V

Several such readings are obtained and they are given in Tab. 8. The last column of the table also shows the efficiency (P_0/P_{in}) of the system calculated using Eq. (10) at different values of P_{CVL}. The experimental results also show the efficiency decreases with an increase in the CVL load.

The following discussion addresses the effect of parasitic elements on stability in addition to the contribution of CVL load towards the same.

The stability given by Eq. (3) is simplified such that the contribution of P_{CVL} and parasitics can be expressed explicitly as

$$P_{st} < \frac{P_{CVL}\left(1+\frac{r_C\mu C}{L}\right)}{1+\frac{r_C\mu C}{L}} + \frac{\left[\left(\frac{r_D-r_Q}{L}\right)I_L+\frac{V_{in}}{L}\right]r_C V_o^2 C+\frac{\mu V_o^2 C}{L}+\frac{r_C V_o^2 C}{L}}{1+\frac{r_C\mu C}{L}} \tag{20}$$

$$P_{st} < P_{CVL} + \frac{\left[\left(\frac{r_D-r_Q}{L_f}\right)I_{L_f}+\frac{V_{in}}{L_f}\right]r_C V_o^2 C_f+\frac{\mu V_o^2 C_f}{L_f}+\frac{r_C V_o^2 C_f}{L_f}}{1+\frac{r_C\mu C_f}{L_f}} \tag{21}$$

$$P_{st} < f\left(P_{CVL}\right)+f\left(r_L\right) \tag{22}$$

where $f(P_{CVL})$ contributes to stability owing to P_{CVL} and $f(r_L)$ contributes to stability due to r_L while r_Q, r_D, r_L and r_C and V_o remained constant. The contribution to the stability of the system from $f(P_{CVL})$ and $f(r_L)$ and the total stability are computed and given in third, fourth and fifth columns of Tab. 9, respectively. If parasitic elements were absent, the system would have become unstable when the CVL load is reduced beyond 10 W.

From the Tab. 9, it can be observed that the system remains stable even when the CVL load is reduced beyond this critical value. This is due to the contribution of the parasitics. In this experimental work, the stability resulting from r_L is 40 W. For enhanced stability, r_L may be increased by inserting external resistance in series with it.

6 Conclusions

Analysis of the stability and efficiency as functions of r_L and P_{CVL} demonstrated that they are conflicting in nature. An increase in the value of r_C pushes the global minimum towards $r_{L\min}$, which reduces the overall losses, thus improving the efficiency of the system. However, the value of r_C cannot be increased beyond a certain value for two reasons: ① It increases the output voltage ripple and ② high frequency components influence the performance of the CPL load connected to the output. Constant voltage load improves the stability of the system with a decrease in efficiency. This was demonstrated through simulation and experimental studies.

In the absence of parasitics, the CVL load connected to the system contributes to the stability. In this study, a constant power load of 10 W is connected and the system remains stable even when the CVL load is

reduced beyond the critical value of 10 W, owing to the contribution of the parasitics.

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