Second Harmonic Generation Exploiting Ultra-Stable Resistive Switching Devices for Secure Hardware Systems

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***Abstract*—In the era of Big Data and Internet of Things (IoT), information security has emerged as an essential system and application metric. The information exchange among the ubiquitously connected smart electronic devices requires functioning reliably in harsh environments, which highlights the need for securing the hardware root of trust. In this work, by leveraging the uniform nonlinear resistive switching of emerging electroforming-free analog memristive device based on $BiFeO_3$ (BFO) thin film, the security-oriented hardware primitive (SoHP) system is developed and optimized with high-security level. The SoHP system utilizes the distinguishable power conversion efficiency generated at second and higher harmonics in low resistance state (memristor with diodelike behavior) and high resistance state (memristor with high resistive behavior) of memristive devices. By exploring the significant influence of writing bias and operational frequency in sourcing input voltage on the dynamic switching behavior of memristive device, the novel 2-memristor encoding scheme and 1-memristor decoding scheme are developed for SoHP system, which realizes a frequency enhancement of 4000 times in comparison to 1-memristor encoding scheme and 2-memristor decoding scheme. The encoded data bits that generated from physically implemented SoHP system pass diverse statistical test suites (i.e. ENT, BSI, and NIST SP-800.22 statistical test suites), which indicates the high randomness distribution of the encoded data and the high-security level of the proposed memristive encoding system.**

***Index Terms*—Ultra-stable resistive switching, second harmonic generation, hardware security, power conversion efficiency.**

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I. Introduction

With the widespread application of electronic systems in communication devices, the demand for secure hardware and secure data transmission has been dramatically increased. The majority of available classical mathematical or algorithmic cyber-defenses in the software-based security system concentrate on protecting the software part of electronic systems or their communication interfaces, which are not only high-energy consuming, but also vulnerable to brute force and malicious code [1], [2]. With the advent of smart homes, smart cities, smart transportation, and infrastructure, etc, the need for securing the hardware root of trust in the Internet of Things (IoT) becomes incredibly anxious [3], [4]. Several studies on hardware-oriented security applications have demonstrated the robustness of functional systems based on nano-electronic technology and their preliminary security capabilities, i.e. memristors [5]–[7], spin-torque devices [8], [9], phase change materials [10], [11], silicon nanowires [12], [13], and etc.. The memristor, as one promising candidate among nano-electronic devices, have the potential to construct innovative computing systems with nanoscale miniaturization [14], [15] and low-power consumption [16].

In the recent years, forming-free $BiFeO_3$ (BFO) memristors have drawn much attention due to highly uniform switching performance with excellent endurance and retention properties [17]–[19] and their promising applications in neuromorphic computing [16], [20]–[22], reconfigurable Boolean logics [23], [24], and in our previous work [25], we have demonstrated the hardware security system by exploiting the second of harmonic generation functionality of analog BFO memristive devices. In this work, based on the nonvolatile nonlinear switching dynamic of BFO memristive devices, we study the impact of writing bias and operational frequency on the generated second harmonic power efficiency, and further optimized the design schematics of the BFO memristor based security-oriented hardware primitive (SoHP) on PCB board, i.e. SoHP-PCB system with 2-memristor

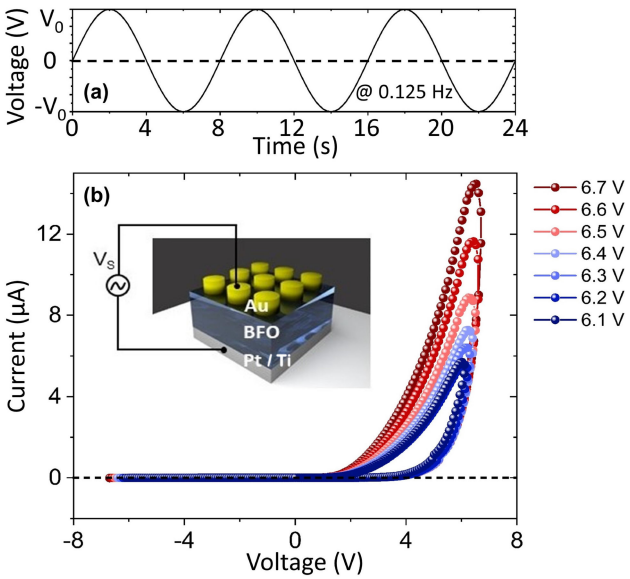

Fig. 1. (a) Sequence of sinusoidal ramping voltage $V_S(t) = V_0 \sin(2\pi f_1 \cdot t)$ with amplitude V_0 ranging from 6.1 V to 6.7 V and frequency $f_1 = 0.125$ Hz and (b) corresponding current voltage characteristics on a logarithmic scale of BFO memristive device with thickness 500 nm and top electrode size 1E5 μm^2. The inset of (b) shows the schematic sketch of the BFO memristive device.

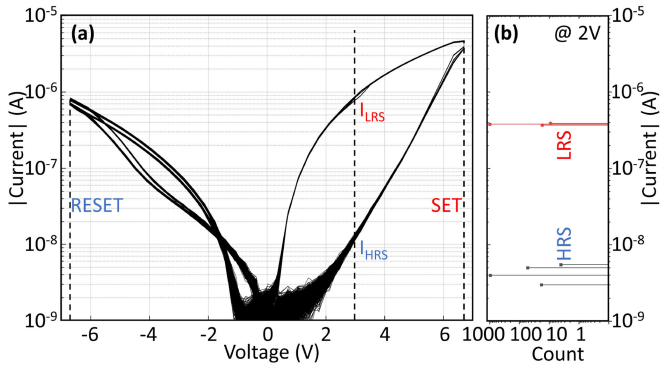

Fig. 2. (a) Endurance tests result for BFO memristor by exploiting 1000 cycles of sinusoidal ramping voltage $V_S(t) = V_0 \sin(2\pi f_1 \cdot t)$ with amplitude $V_0 = 6.7$ V and frequency $f_1 = 0.125$ Hz. The LRS and HRS current are defined at smaller reading bias V_r ($V_{r,max} = 3$ V). (b) Histogram of reading current at $V_r = 2$ V as an example. The concentrated reading currents prove the ultra-uniformity of the Current-Voltage performance of the BFO memristor.

encoding scheme and 1-memristor decoding scheme, which has realized the improvement of encryption speed by 4000 times in comparison to the SoHP implementation in previous work [25].

The work is organized as follows: After the introduction of the ultra-stable switching behavior of BFO memristor in Section I, the writing bias and frequency-dependent power conversion efficiencies of the BFO memristor are analyzed in Section II. By investigating the optimization progress of the laboratory implementation for BFO memristor-based SoHP systems, the optimized circuit block diagram of memristive SoHP system is finalized (Section III). For investigating the security level of the implemented SoHP system, the randomness test result of encrypted data by using NIST SP-800.22 statistical test suite reveals the security level of the optimized memristive SoHP system.

II. High Efficient Second Harmonic Generation Exploiting BFO Memristive Devices

By revealing the nonvolatile nonlinear high uniform switching behavior of BFO memristive devices, high efficient second harmonic can be generated. The writing voltage and frequency dependence of the testing signal play an essential role in the encoding and decoding performance of SoHP system.

A. BFO Memristive Devices With Nonlinear High Uniform Switching Behavior

Polycrystalline BFO thin film with the thickness of 500 nm was deposited by pulsed laser deposition (PLD) on Pt/Ti/SiO_2/Si substrate with Pt/Ti layer thickness of 100 nm /50 nm. The schematic sketch of the Au-BFO-Pt/ Ti MIM structure is depicting in the inset of Fig. 1. The physical mechanism underlying resistive switching of BFO memristive devices is related with the nonvolatile change of flexible barriers at Ti-containing bottom electrode region. Circular Au top electrodes with an area of 1E5 μm^2 and a thickness of 150 nm were fabricated by DC magnetron sputtering at room temperature using a metal shadow mask for the following current-voltage and higher harmonic generation tests. The downscaling of the thickness of BFO thin films, i.e. from 500 nm to 100 nm, has been investigated in our previous work [26]. With downscaled BFO thin film thickness the writing bias of BFO memristive device can be further reduced with maintained switching behavior. Due to its reliable and uniform switching behavior, the BFO memristor with BFO thin film thickness of 500 nm is chosen for the second harmonic generation in this work.

For operating the BFO memristive device, the large writing biases with opposite polarity are required to switch the device into the valid low resistance state (LRS) or high resistance state (HRS) for the application-oriented purpose. As demonstrated in Fig. 1 the current voltage characteristics of BFO memristive device are recorded under the sinusoidal sourcing voltage $V_S(t) = V_0 \sin(2\pi f_1 \cdot t)$ with diverse amplitudes V_0. During the IV testing, the sinusoidal sourcing input voltage (with 80 testing points and 0.1 s time width per testing point) is applied to the top electrode of the memristive device. Thus the testing frequency of sinusoidal sourcing input voltage for recording IV characteristics amounts to 0.125 Hz. As demonstrated in Fig. 2, by applying large positive input bias, e.g. +6.7 V, to the Au top electrode of BFO memristive device, the device is switched to LRS. This process is identified as SET process, thus the LRS current I_{LRS} can be recorded at a small reading bias, e.g. 3 V. By sourcing large negative input voltage, e.g. −6.7 V, to the Au top electrode, the device can be then switched to HRS, and the switching process is identified as RESET process. Thus the HRS current I_{HRS} can be recorded at a small reading bias, e.g. 3 V. The analog hysteresis is recognizable within the positive bias range in the IV characteristics of BFO memristor. It reveals the self-rectifying nonlinear switching behavior of BFO memristive device. The nonvolatile property of BFO memristive device ensures that the device remains in LRS or

HRS under a small reading bias V_r ($V_{r,max} = 3$ V). The Off/On ratio of corresponding analog hysteresis at 3 V under voltage amplitude V_0 of $|\pm 6.7|$ V amounts to 91.60, which is calculated by using the following equation: I_{LRS}/I_{HRS} or R_{HRS}/R_{LRS}. Hence the Off/On ratio is unitless. By applying the sinusoidal sourcing voltage with decreasing voltage amplitudes V_0 from 6.7 V to 6.1 V, the Off/On ratio of analog hysteresis at reading bias 3 V is shrinking due to the decreasing LRS current, i.e. from 91.60 to 25.38. It further reveals that multi-level resistive switching states of BFO memristive device are realizable under different V_0. By applying 1000 cycles of sinusoidal ramping voltage $V_S(t)$ with amplitude $V_0 = 6.7$ V and frequency $f_1 = 0.125$ Hz, the endurance performance of the BFO memristor is explored in Fig. 2. The concentrated reading currents at small reading bias, e.g. at 2 V, in LRS and HRS from 1000 cycles of IV characteristic reveal ultra-uniform switching behavior of BFO memristor in comparison to other types of memristive devices [27]–[29], which fundamentally ensures the stability of the second harmonic generation in the BFO memristor based SoHP system.

The self-rectifying behavior and its nonlinear switching dynamics of BFO memristive device makes it feasible for generating the second and higher harmonics which can be used for hardware-oriented encoding and decoding system with higher security level. As shown in the inset of Fig. 1(b), a sinusoidal sourcing voltage $V_S(t)$ is applied between the Au top and Pt bottom electrodes of BFO memristive device as the excitation stimuli for the second and higher harmonic generation. The power ratio between the average power at k-th harmonics and average source power is defined as the power conversion efficiency P_k/P_s (PCE), which is the crucial parameter for data encoding and decoding procedures. The corresponding second and higher harmonic signals are translated into frequency domain by Fast Fourier Transform (FFT) transformation for further computing the PCE values.

B. Power Conversion Efficiency Based on Memristive Device

For generating the distinguishable second and higher harmonic, the memristive device is initialized to LRS (HRS) by applying single 100 ms writing pulse with pulse amplitude $V_w = +6.7$ V ($V_w = -6.7$ V) to the top electrode of device, and the PCE values at different harmonics are recorded under the sinusoidal sourcing voltage $V_S(t) = V_0 \sin(2\pi f_1 \cdot t)$ with $V_0 = 3$ V and $f_1 = 0.125$ Hz. PCE values are generated and computed based on the circuit topology with BFO memristor in series of a variable linear load resistor R_L (from 100 Ω to 1 GΩ). Take the second harmonic generation as an example, the PCE diagram in Fig. 3 demonstrates the PCE values at 2nd harmonic $P_{L,2}/P_S$ recorded from BFO memristive device in both LRS and HRS under sinusoidal sourcing voltage in dependence of load resistor R_L. Due to an application of large positive writing bias, fixed Ti donors close to the bottom electrode can effectively trap mobile oxygen vacancies in BFO thin film, thus the barrier height near to the bottom electrode becomes non-rectifying and BFO memristive device is in LRS. By applying the large negative writing bias, the mobile donors, i.e. oxygen vacancies, in BFO thin film are redistributed between the top and the bottom electrode. The barrier height near the bottom electrode becomes rectifying and the device is in HRS. It is noteworthy that the barrier height in Au top electrode region remains rectifying under both positive and negative writing biases. Due to the different functional behaviors of BFO memristive device in LRS (diode like behavior) and in HRS (high-ohmic behavior), the distinguishable sets of PCE diagrams can be recorded in both LRS and HRS, thus the input data '0' and '1' can be encoded and transmitted, respectively.

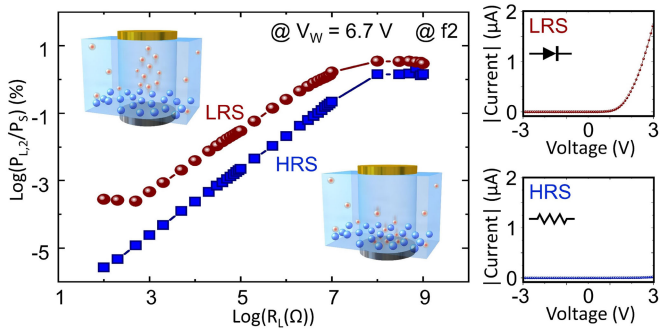

Fig. 3. Power conversion efficiency $P_{L,2}/P_s$ (PCE) curve of the BFO memristor between the average power at second harmonics and average source power under the sinusoidal sourcing voltage $V_S(t) = V_0 \sin(2\pi f_1 \cdot t)$ with $V_0 = 3$ V and $f_1 = 0.125$ Hz and prior to the PCE measurements, the memristor was initialized by writing voltages with pulse amplitude $V_W = 6.7$ V. With the positive writing bias $V_W = 6.7$ V, fixed Ti donors close to the bottom electrode can effectively trap mobile oxygen vacancies in BFO thin film, thus the barrier height near to the bottom electrode becomes non-rectifying and BFO memristor is set in LRS. By applying negative writing bias $V_W = -6.7$ V, the oxygen vacancies, in BFO thin film are redistributed between the top and the bottom electrode. The barrier height near the bottom electrode becomes rectifying and the device is set in HRS.

For the sake of the performance improvement of SoHP system, in this work the study on the PCE diagrams with BFO memristive devices in LRS or HRS in dependence on the sinusoidal sourcing voltage with various amplitudes V_0 is carried out, and their perspective influences on the SoHP system are analyzed. As demonstrated in Fig. 4(a), after the initialization process with pulse amplitude $V_W = 6.7$ V, the PCE value recorded in LRS at 2nd harmonic $P_{L,2}/P_S$ is significantly larger than that in HRS for the specific load resistor R_L (PCE values $\log(P_{L5,2}/P_S)$ in LRS and HRS are -1.51959 and -2.64771, respectively). This is because the BFO memristive device is functioning as a diode in LRS, and as a high-ohmic resistor in HRS. After the initialization process with pulse amplitude $|V_W| = 6.1$ V (Fig. 4(b)), the BFO memristive device is not fully switched to LRS or HRS, and it is predictable that the corresponding Off/On ratio will be smaller than that switched by writing bias $V_W = 6.7$ V. Thus, the hysteresis and nonlinearity of IV characteristics are depressed under initialization pulse amplitude $|V_W| = 6.1$ V, which results in the undistinguishable power ratios between LRS and HRS as shown in (Fig. 4(b)). Only the two clearly distinguishable sets of power ratio curves in LRS and HRS can be used for designing the hardware-oriented security primitives.

As next, the PCE diagrams recorded under various V_W are analyzed. As shown in Fig. 4(d), we exam the opening area between PCE curves in LRS and HRS by evaluating the minimal

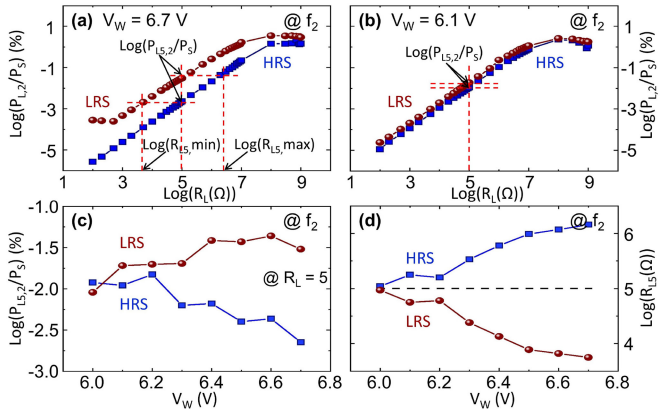

Fig. 4. Comparison of PCE curves of BFO memristive device in both LRS and HRS at 2nd harmonic under sinusoidal input voltage with amplitudes $V_0 = 3$ V and prior to the PCE measurements, the device was initialized by writing voltages with pulse amplitude (a) $V_W = 6.7$ V and (b) $V_W = 6.1$ V. (c) Interface PCE values $\log(P_{L5,2}/P_S)$ and (d) load resistor range for detecting LRS and HRS with $R_{L5,min} < R_L$ and $R_{L5,max} > R_L$ with $R_L = 100\ k\Omega$ at 2nd harmonic in dependence on sinusoidal input voltage.

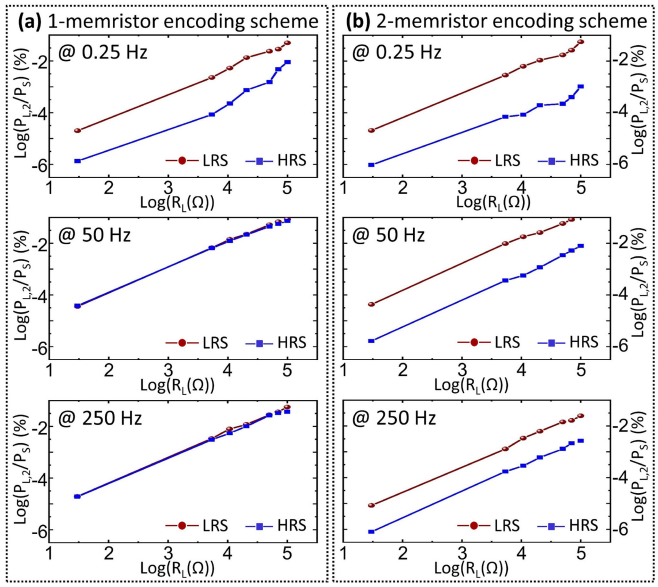

Fig. 5. Frequency dependent power conversion efficiency diagrams in (a) one-memristor encoding scheme and (b) two-memristor encoding scheme. The PCE curves in both LRS and HRS under sinusoidal input voltage with voltage bias of $V_0 = 3$ V and frequencies f = 0.25 Hz, 50 Hz, and 250 Hz are examined. The memristive devices were initialized by the writing bias with amplitude $|V_W| = 6.7$ V.

and maximal PCE values at $R_L = 100\ k\Omega$, i.e. $\log(P_{L5,min})$ and $\log(P_{L5,max})$, respectively. $\log(R_{L5})$ values, difference between $\log(P_{L5,max})$ and $\log(P_{L5,min})$, in LRS and HRS at $V_W = 6.0$ V are 4.97 and 5.04. The cross points between the load resistor at $\log(R_L) = 5$ and PCE curves at 2nd harmonic are defined as interface PCE values $\log(P_{L5,2}/P_S)$ in both LRS and HRS, respectively. The interface PCE values are analyzed in Fig. 4(c) in dependence on the pulse amplitudes of writing voltages V_W, i.e. the Off/On ratio in the corresponding resulted IV characteristics. With decreasing pulse amplitude V_W, the corresponding PCE values in LRS and HRS at 100 $K\Omega$ $\log(P_{L5,2}/P_S)$ converge at $V_W = 6.03$ V, which reveals decreased nonlinear dynamics in IV characteristics of memristive device. As illustrated in Fig. 4(a), the load resistor region used for encoding input data is defined between the minimum load resistor value in LRS $\log(R_{L5}$,min) and maximum load resistor value in HRS $\log(R_{L5}$,max). The minimum and maximum load resistor values $\log(R_{L5}$,min) and $\log(R_{L5}$,max) at 2nd harmonic in dependence on pulse amplitude of writing voltage V_W are derived from PCE diagrams and plotted in Fig. 4(d). With decreasing V_W, the opening area between $\log(R_{L5}$,min) and $\log(R_{L5}$,max), which is used for encoding input data, decreases. Thus the encoding system is theoretically no longer functioning if the pulse amplitude lower than $V_W = 6.03$ V according to the crossing point in Fig. 4(d).

In the SoHP system, the frequency of input sinusoidal voltage $V_S(t)$ is the key parameter which limits the encoding and decoding velocity. Thus the impact of the input sinusoidal voltage $V_S(t)$ is experimentally investigated for the SoHP-system. In Fig. 5(a) the frequency influence on 1-memristor encoding scheme is demonstrated. In 1-memristor encoding scheme, the load resistor R_L is connected in series with one single BFO memristive device, which is continuously switched between LRS and HRS according to the input data. We can see that at 0.25 Hz, the opening area between LRS and HRS PCE curves can be adopted in the SoHP system, but at 50 and 250 Hz, LRS and HRS PCE curves become indistinguishable, which can not be used anymore. Such phenomenon is caused by the intrinsic high frequeny switching property of memristive devices, i.e. the input voltage at high frequency eliminates the hysteresis characteristic of the memristive devices.

For the sake of high encrypting and decrypting efficiency, the 2-memristor encoding scheme is developed and the PCE diagrams are recorded as demonstrated in Fig. 5(b) under input sinusoidal voltage $V_S(t)$ with frequencies 0.25 Hz, 50 Hz, and 250 Hz, respectively. In the 2-memristor encoding scheme, the load resistor R_L was separately connected in series with two BFO memristive devices, which are permanently switched to LRS and HRS under pulse amplitude $V_W = 6.7$ V and -6.7 V, respectively. The average power ratio over load resistor was recorded under the sinusoidal testing input voltage $V_S(t) = V_0 \sin(2\pi f_1 \cdot t)$ with amplitude $V_0 = 3$ V at frequencies $f_1 = 0.25, 50$ and 250 Hz, which is insufficient to corrupt the well-defined LRS or HRS memristive states. The power ratio efficiency $P_{L,2}/P_S$ is then demonstrated in Fig. 5(b). In the 2-memristor encoding scheme, under the input voltage testing with amplitude 3 V, the LRS memristor remains rectifying and working as a diode device, whereas the HRS memristor functions as high resistive resistor (as shown in Fig. 3). Thus it is expectable that the distinguishable PCE curves can be recorded even at an elevated frequency, e.g. at 250 Hz, in Fig. 5(b). Therefore, the nonvolatile high uniform rectifying switching behavior of BFO memristor plays a role in generating distinguishable PCE curves over the memristor, which maintains the opening area between LRS and HRS PCE region under input sinusoidal voltage with high frequency. Thus the 2-memristor encoding scheme is adopted in the circuit design of the encoder in the SoHP system as demonstrated in Fig. 6(b).

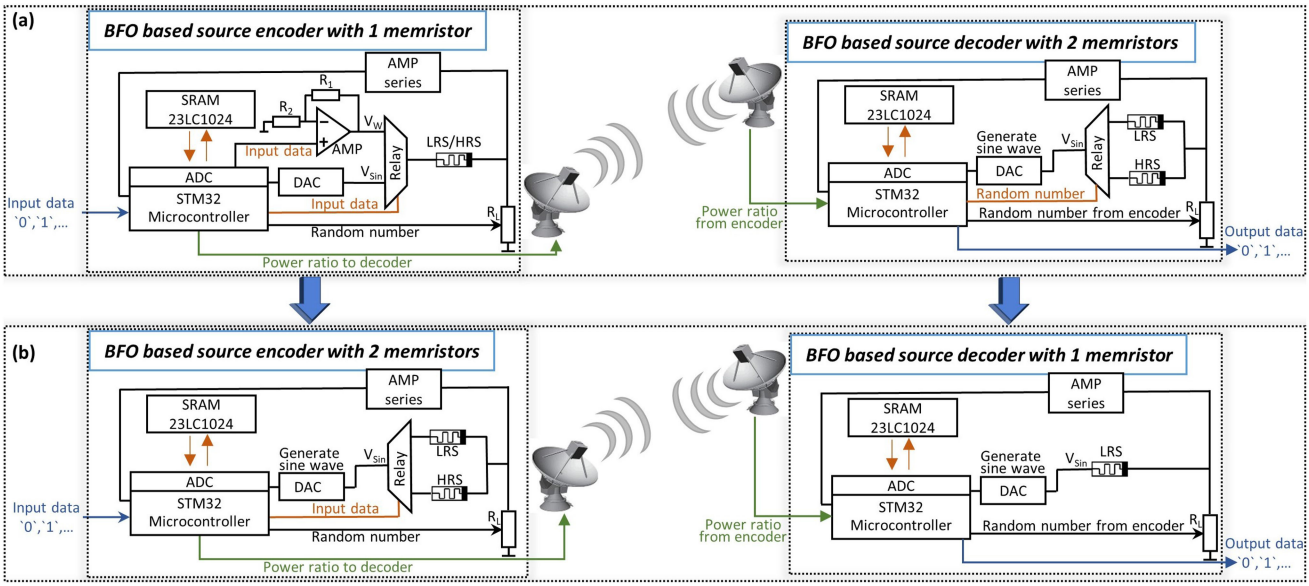

Fig. 6. Block diagrams of BFO memristor based SoHP systems: (a) The SoHP system with 1-memristor encoding scheme and 2-memristor decoding scheme requires one BFO memristor continues switchable between LRS and HRS during data encryption, and requires two BFO memristors with well-defined LRS and HRS in the decoder. (b) The improved SoHP system with 2-memristor encoding scheme and 1-memristor decoding scheme requires two BFO memristors with well-defined LRS and HRS in the encoder and one BFO memristor in LRS in the decoder which enables the higher frequency implementation of data encoding and decoding processes. Both encoders encrypt the input binary data into modulated data by measuring the power ratio $P_{L,2}/P_S$ (between the average source power and the 2nd harmonic power) on the memristor with ADC via an amplifier series. At the same time, a sinusoidal voltage generated by DAC as the excitation signal is applied on the corresponding memristive device, under the control of STM32 microcontroller.

III. BFO Memristor Based Security-Oriented Hardware System

With nonvolatile switching performance, the memristor was proposed to be applied to various fields: next generation nonvolatile resistive memories [30]–[32], neuromorphic system [33], [34], chaotic circuits [35], [36], and etc. In this work, we extend the application of memristor for higher harmonic generation to security-oriented applications.

The block diagrams for constructing BFO memristor based SoHP systems with 1-memristor encoding scheme and 2-memristor encoding scheme are illustrated in Fig. 6(a) and Fig. 6(b), respectively. The SoHP system with 1-memristor encoding scheme in Fig. 6(a) requires two BFO memristors with well-defined LRS and HRS in the decoder, whereas the SoHP system with 2-memristor encoding scheme in Fig. 6(b) requires one BFO memristors in LRS in the decoder, which enables the higher frequency implementation of data encoding and decoding.

The 1-memristor encoding scheme of SoHP system is advanced based on the system design in Ref. [25]. The BFO memristor in 1-memristor encoding should be continuously switched between LRS and HRS according to the input binary data '0' and '1', respectively. The encoding process is designed as follows: The input binary data are firstly stored in the embedded SRAM to coordinate the speed difference between the data reception and the data encoding. The single one BFO memristor is connected in series with load resistor R_L, resulting in a series M-R_L circuit. For the transmission of the input binary data '0' ('1'), the memristive device has to be correspondingly set to LRS (HRS) by applying writing voltage with pulse amplitude $V_W = +6.7$ V and $V_W = -6.7$ V to the top electrode of device via an amplifier. The sine wave source voltage $V_S(t)$ is activated by a MC controlled digital to analog converter (DAC), and applied to the M-R_L circuit for generating second and higher harmonics. The relay determines, based on the input binary data, whether the writing voltage V_W or the excitation sinusoidal voltage $V_S(t)$ is applied to the memristor: If the input binary data is '0' ('1'), the memristor is first set in LRS (HRS) by the writing voltage V_W, then switched memristor accesses excitation sinusoidal voltage $V_S(t)$ generated by DAC. The power at second harmonic $P_{L,2}$ over load resistor R_L is then extracted by an analog to digital converter (ADC) integrated inside STM32 MC with adopting an amplifier series and transformed into the frequency domain by FFT transformation. The encrypted power ratios at second harmonic $P_{L,2}/P_S$ are transmitted via an antenna to the BFO memrsitor based decoder. In the 1-memristor encoder scheme, the continuous switching process of BFO memristor between LRS and HRS is the bottleneck for the encoding velocity. For the sake of high encrypting efficiency in the SoHP system, the 2-memristor encoding scheme is proposed (Fig. 6(b)).

In the optimized 2-memristor encoding scheme, two BFO memristors are utilized, which are set to LRS and HRS respectively by applying writing voltage with pulse amplitude $V_W = +6.7$ V and $V_W = -6.7$ V to the top electrode of device, before transmission of the input data. Here the relay determines the selection between the memristors in LRS and HRS according to the DAC converted input binary data: If the input data is '0', the memristor in LRS accesses to the circuit, otherwise for '1', HRS memristor is selected. In this way, the second and higher harmonic signals are generated by utilizing pre-defined LRS or HRS memristor in series with load resistor R_L upon a sinusoidal voltage source $V_S(t)$. The flowchart in

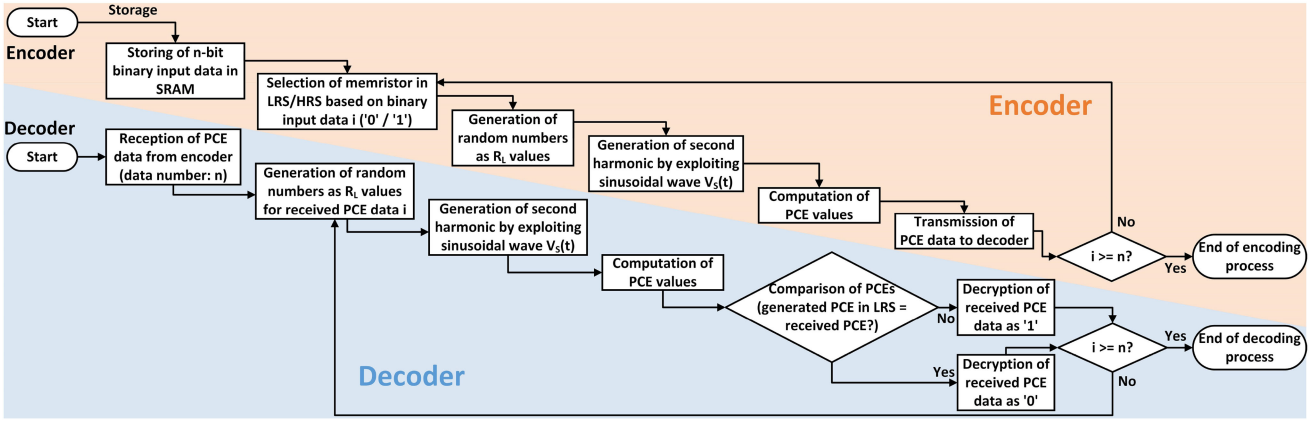

Fig. 7. Flowchart for depicting the encryption and decryption processes of n-bit input data of 2-memristor encoder scheme and 1-memristor decoder scheme in the SoHP-PCB system.

Fig. 7 (marked with orange background color) illustrates the aforementioned encryption process for the 2-memristor encoder scheme. In the encoding process of each bit of input data, the switching process of the BFO memristor is omitted, and the encoding time is not limited by the switching process of the BFO memristor anymore. The encoding time is extremely shortened in the optimized 2-memristor encoding scheme. Thus without the requirement of the memristive switching process, it highlights the potential of 2-memristor encoding scheme in terms of high efficiency encoding: the encoding frequency of SoHP system with 2-memristor encoding scheme can reach 1 kHz, which is 4000 times higher than 1-memristor encoding scheme. The 1 kHz encoding frequency of improved 2-memristor encoding scheme is further limited by the operation frequency of the analog circuitry STM32 MC, DAC and ADC. It is thus expectable with more advanced electronic components bring even higher frequency. Eventually, the encrypted power ratios at second harmonic $P_{L,2}/P_S$ in the encoder are transmitted from sender to the receiver via an antenna.

At receiver, the SoHP system with 2-memristor decoding scheme (Fig. 6(a)) [25] has been optimized and upgraded to 1-memristor decoding scheme (Fig. 6(b)). Instead of using two BFO memristive devices in 2-memristor decoding scheme, which are permanently set to LRS and HRS, respectively, the single one BFO memristor in LRS is utilized in 1-memristor decoding scheme. The 1-memristor decoding scheme simplifies the data decrypting process, while ensuring the functionality of the decoder. The same random sequence of load resistor values for R_L is generated simultaneously by the random number generator integrated inside STM32 MC. Thus the secondary power efficiency is computed according to the second harmonic signal generated from series combination circuit of LRS BFO memristor and load resistor R_L. By comparing the secondary power efficiency with the received one from encoder, the output binary data of the decoder is determined: '0' is transmitted, if the power efficiencies are equal to each other; otherwise, data '1' is transmitted. The aforementioned decryption process for 1-memristor decoding scheme is depicted in Fig. 7 (marked with blue background color). Without the selection process between LRS and HRS memristors realized by relay, the design of 1-memristor decoding scheme simplifies the functional structure of the decoding circuit, boosts the decrypting efficiency and shrinks the system cost in terms of power consumption and operation latency. The 2-memristor encoding scheme and the 1-memristor decoding scheme (Fig. 6(b)) are adopted in the final version of SoHP-PCB system, and its laboratory realization is demonstrated in Fig. 8.

The three-step optimization approaches for implementing the BFO memristor based security-oriented hardware primitive (SoHP) system is illustrated in Fig. 8, including SoHP system exploiting off-the-shelf devices (SoHP-OTSD) (Fig. 8(a)), SoHP system exploiting microcontroller (SoHP-MC) (Fig. 8(b)), and integrated SoHP system on PCB board (SoHP-PCB) (Fig. 8(c)). Each implementation of the SoHP system consists of the encoder and decoder schemes based on BFO memristors. The SoHP-OTSD implementation is based on the system block diagram Fig. 8(a)), where the combined design of a MC based hardware system controlled by LabVIEW software with the support from off-the-shelf Keithley 2400 source meter is adopted. In the MC based hardware system of SoHP-OTSD version, the memristive devices are connected with the load resistor in series as the basic circuit topology. The LabVIEW software is responsible for providing the excitation source signal via the Keithley 2400 source meter and extracting the power efficiency at second harmonic $P_{L,2}$ over load resistor, which is used for data encryption and decryption according to input binary data. Both SoHP-MC (Fig. 8(b)) and SoHP-PCB implementations (Fig. 8(c)) are sharing the same circuit topology, i.e. consisting of 2-memristor encoding and 1-memristor decoding schemes with higher operational speed. For the sake of higher integrality of the encryption system, the off-the-shelf devices (LabVIEW and Keithley 2400) from SoHP-OTSD implementation have been substituted by the STM32 microcontroller (MC) with required DAC, ADC and a couple of operational amplifiers in order to convert the measuring voltage range. The further SoHP-PCB implementation is integrated into a custom-made electronic PCB board with size of 80 $mm \times 68$ mm to bestow the SoHP system a higher level of integration and stability. In comparison to SoHP-OTSD, the optimized SoHP-MC and SoHP-PCB with 2-memristor encoding scheme and 1-memristor decoding scheme has improved the frequency from 0.25 Hz to 1 KHz, thus the encryption/decryption speed is increased

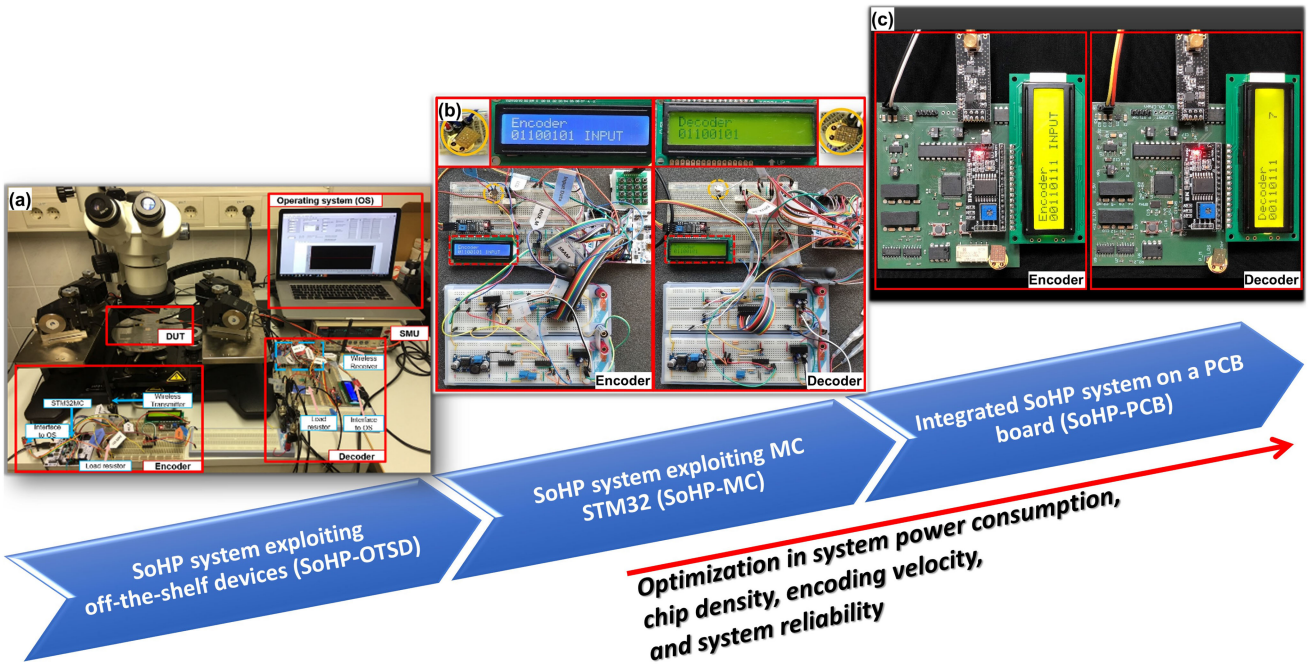

Fig. 8. Three-step optimization of system power consumption, chip density, encoding velocity, and system reliability for a BFO memristor based security-oriented hardware primitive (SoHP) system: (a) SoHP system exploiting off-the-shelf devices (SoHP-OTSD); (b) SoHP system exploiting microcontroller STM32 (SoHP-MC); (c) Integrated SoHP system on a PCB board (SoHP-PCB). The first version SoHP-OTSD adopts the combined design of a hardware system and a LabVIEW software system with the support from off-the-shelf Keithley 2400 source meter. For higher encryption/decryption speed and the integrability of the system, the off-the-shelf devices (LabVIEW and Keithley 2400) are substituted by the STM32 microcontroller and other electronic components, in the improved version SoHP-MC. The final version SoHP-PCB bestows the SoHP system a higher level of integration and stability.

by 4000 times. By omitting the switching process of the BFO memristor for each bit of input data in the encoding scheme and simplifying the decoding scheme, the power consumption of the SoHP system is substantially reduced. The video of encryption and decryption processes for optimized SoHP-PCB system is provided as supplementary material. The encrypted data are transferred from the encoder through a wireless transceiver to decoder. Note that, the further higher operational frequency than 1 KHz is possible, if the electrical peripheral circuits, i.e. MC, DAC and ADC with higher operating frequency are adopted.

Randomness is a probabilistic property and the properties of a random sequence can be characterized and described in terms of probability [37]. For a cryptographic algorithm or system, the randomness of its encrypted sequence is an important aspect of its security. For testing the security level of the SoHP system, a randomness test has been executed with the NIST SP-800.22 statistical test suite [38], which is one of the most reliable randomness test suit currently with 15 tests utilized for the evaluation of random number generator (RNG). Fig. 9 depicts the randomness test results for the hardware oriented SoHP-PCB security system with writing bias $V_W = 6.7$ V and sinusoidal frequency $f_1 = 0.125$ Hz at second harmonic. In the specific statistical test for randomness, 5.12×10^7 power ratio data transferred between the security system with the bit stream with the length of 5.12×10^5 are analyzed. According the NIST publication [38], the output of the statistical test called P-value represents the level of randomness: Data sequence with higher P-Value P (maximal 1) indicates higher level of randomness. Given the significance level $\alpha = 0.01$, a test is interpreted as

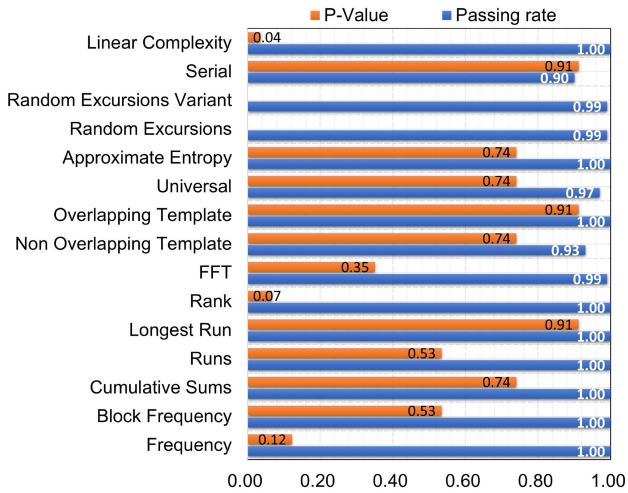

Fig. 9. Randomness test result of NIST SP800-22 for the hardware oriented security system. All 15 tests with P-Value ≥ 0.01 (significance level) pass the randomness test. The larger P-Value (maximal 1.00) of the PCE data sequence, which are recorded from the SoHP system, indicates the improved randomness. The passing rates (blue) are calculated by NIST test suite for 5.12×10^7 PCE data transferred between the hardware oriented security system with the bit stream of 5.12×10^5 bit length.

follows:

$$\begin{aligned} P &< \alpha \quad \text{the test is failed} \\ P &\geq \alpha \quad \text{the test is passed} \end{aligned} \tag{1}$$

All 15 tests with P-Value $P \geq 0.01$ (α) are considered passed. The passing rates (blue) are calculated by NIST test suite for

100 PCE data sequences as demonstrated in the Fig. 9. The test results provide evidences for the strong randomness of the encrypted data and for the extremely low possibility of the BFO memristor-based security system being cracked. Beside the higher security level, the flexible freedom parameters and the low power consumption performance grant the BFO memristor-based SoHP system a wide application potential in various fields. Moreover, for further randomness verification of the encrypted data, two more randomness tests have been conducted, i.e. the ENT (A Pseudorandom Number Sequence Test Program), which is an entropy estimator and the BSI's (German Federal Office for Information Security) statistical test suite, which puts an emphasis on forward/backward secrecy and other security properties. The extensive detailed results of the BSI suite and ENT random number sequence test are exhibited as supplementary materials. The encrypted data from BFO memristor based SoHP system have passed the NIST, ENT and BSI test suits.

IV. Summary and Outlook

In this work, the high efficient security-oriented hardware system by exploiting the emerging electroforming-free $BiFeO_3$ (BFO) based ultra-stable memristive devices has been developed. With the help of untra-stable switching behavior of BFO based memristive devices, the impact of writing voltage V_W on the switching dynamics and on the efficiency of second harmonic generation is revealed, i.e. the larger the V_W, the more distinguishable PCE curves in both LRS and HRS can be generated. In SoHP system, the PCE curves in LRS and HRS are used for encoding binary input data '1' and '0'. Based on the BFO memristor in LRS with diode-like behavior and in HRS with high resistive behavior, the SoHP-PCB system with 2-memristor encoding scheme is developed, and alleviates the issue of limited operating frequency caused by the unswitchable memristive dynamic behavior at elevated frequency. The operating frequency of SoHP system is thus improved by 4000 times (from 0.25 Hz to 1 kHz). Furthermore, the design of 1-memristor decoding scheme simplifies the functional structure of the decoding circuit, boosts the decrypting efficiency and shrinks the system cost in terms of power consumption and operation latency. The PCB implemented SoHP system has passed all 15 statistical randomness tests of NIST SP-800.22 test suite, which proves the random distribution of encrypted data and highlights its high security level.

A clear benefit of the proposed hardware security solution over software-based system lies in its insensitivity to malicious code and brute force attacks. It is also noteworthy that not only BFO memristive devices, but also other types of memristive devices with nonlinear analog switching behavior can be applied in the proposed SoHP system. The analysis of the energy efficiency of the designed system is highly dependent on the operational efficiency of the applied memristive devices. Compared to a logic-level EXOR cipher (implemented in hardware or software) followed by transmission of the ciphertexts, the BFO memristor-based SoHP system is an integrated solution that avoids overheads for synchronization and contains more freedom parameters, due to their influence on the PCE map, i.e. pulse amplitude of writing voltage V_W, maximum sine wave amplitude V_0 and harmonic k, which give the SoHP system degrees of freedom that are not available for the standard solution. Additionally, being a hardware encryption device, the SoHP system can be encapsulated to prevent tampering, whereas software or hardware implementations of the EXOR cipher can be prone to physical attacks (die-channel analysis and fault injections). For even higher frequency applications, the current SoHP system can be combined with a linear-feedback shift register, reaching a generation rate in the GHz range. The proposed memristor based SoHP system with high security level is suitable for communication encryption in the daily communication equipment, i.e. mobile phone and laptop, etc., as an embedded implant system.

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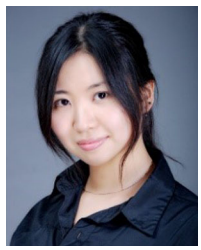

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