SiQAD: A Design and Simulation Tool for Atomic Silicon Quantum Dot Circuits

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Abstract—This paper introduces SiQAD, a computer-aided design tool enabling the rapid design and simulation of computational assemblies of atomic silicon quantum dots. SiQAD consists of several simulation tools: a ground state electron configuration finder, a non-equilibrium electron dynamics simulator, and an electric potential landscape solver for the exploration of field-driven modulation with electrodes. Simulations have been compared against past experimental results to inform the electron population estimation and dynamic behavior. Fundamental logic building blocks and circuits suitable for this platform have been designed and simulated, and a clocked wire has been demonstrated. This work paves the way and provides the first set of open design tools for the exploration of the emerging design space of atomic silicon quantum dot circuits.

Index Terms—Computer aided design, quantum dots, silicon dangling bonds, simulation, SiQAD.

I. INTRODUCTION

RECENT advancements in scanning probe microscopy have enabled the precise creation and erasure of silicon dangling bonds (DBs) on the hydrogen passivated silicon 100 2×1 (H-Si(100)-2×1) surface [1]–[3]. These DBs have tightly confined orbital wavefunctions with energies that fall within the silicon substrate's bulk band gap [4], [5], and can be considered as zero dimensional quantum dots with at most two occupying electrons [6]–[8]. The total number of electrons within ensembles of DBs, as well as their spatial arrangement, are governed by electrostatic interactions [9], [10]. The preferred charge configurations of specific patterns of DBs enable the

creation of logic gates [9], [11], introducing a fundamentally new computational platform technology and unique design space at the atomic scale. Exploration of this prospective technology requires new tools for simulating the behavior of DB patterns.

Here we present SiQAD (**Si**licon **Q**uantum **A**tomic **D**esigner), a computer-aided design (CAD) tool that provides an environment for the design and simulation of DB circuits, thus enabling rapid prototyping of DB designs before they are physically fabricated. This paper is organized as follows: Section II provides the technical background on DB quantum dot circuits; Section III introduces SiQAD's capability for circuit design and simulation, and describes the software architecture of the CAD tool; Section IV provides detailed explanations and simulation results of the three included simulation tools; Section V presents new DB logic gates and circuits created using SiQAD, as well as design rules gathered in the process.

II. BACKGROUND

Silicon DBs are fabricated by desorption of individual hydrogen atoms from a hydrogen-terminated silicon surface using the probe of a scanning tunneling microscope (STM); H-Si bonds are broken by applying a voltage pulse at a hydrogen site, leaving behind a valence orbital as depicted in Fig. 1(a) [3], [12]–[14]. Hydrogen sites are located atop silicon atoms with locations discretely defined by the lattice structure, allowing the creation of DBs at atomically precise locations as illustrated in Fig. 1(b). There are three charge states that a DB can host: the unoccupied positive state (DB+), singly occupied neutral state (DB0), and doubly occupied negative state (DB−). Since the charge transition levels between these states exist within the band gap as illustrated in Fig. 1(c), they are considered electrically isolated from the bulk [8], [15] and allow for discrete electron population by manipulating the relative energetic positions between the bulk Fermi energy and the charge transition levels [6], [7], [16], [17]. A number of factors contribute to band bending, including inter-DB Coulombic interactions [6], [9], external fields such as the contact potential of the tip of a nearby STM or atomic force microscope (AFM) [16], [18], and charged subsurface dopants [19]. This band bending shifts the charge transition levels with respect to the bulk Fermi level. The charge occupation of a DB changes when its charge transition level crosses the Fermi level due to changes in the energy landscape; local charge defects or dopants can affect the energies at which this happens

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(a) Surface of H-Si(100)-2×1 with DB.

(b) DB layout.

(c) Schematic of DB energy level diagram.
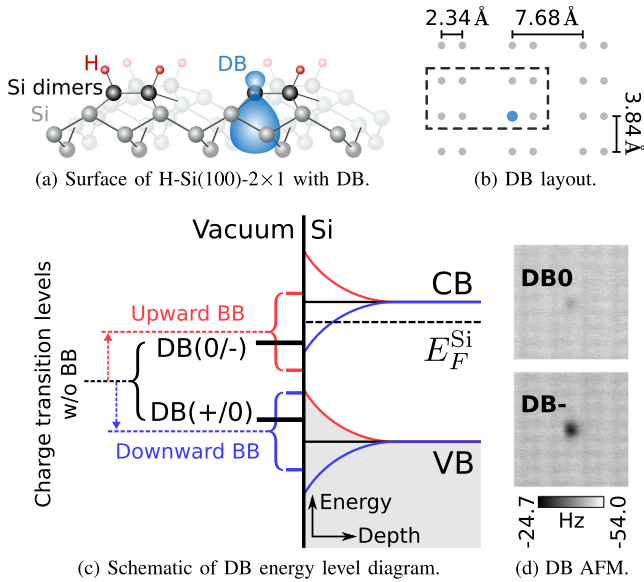
(d) DB AFM.

Fig. 1. (**a**) Desorbed hydrogen leaves a valence orbital, shown in blue, in H-Si(100)-2 × 1 with mid-gap charge states. (b) Schematic top view of the surface where the highlighted area represents the region in (a). The blue dot represents a DB and the smaller gray dots represent hydrogen locations where DBs can be created. (c) Schematic of the DB energy level diagram illustrating the mid-gap DB positive to neutral (+/0) and neutral to negative (0/-) charge transition levels. The red, blue, and black states represent upward band bending, downward band bending, and no band bending respectively. VB and CB represent the valence and conduction bands, and E_F^{Si} denotes the bulk Fermi energy. (d) AFM images of a DB in DB0 (singly occupied) and DB− (doubly occupied) states. Contrast can be used to directly imply the charge state of DB ensembles.

(a) STM images of the OR gate [9].

(b) AFM images of the OR gate [9].
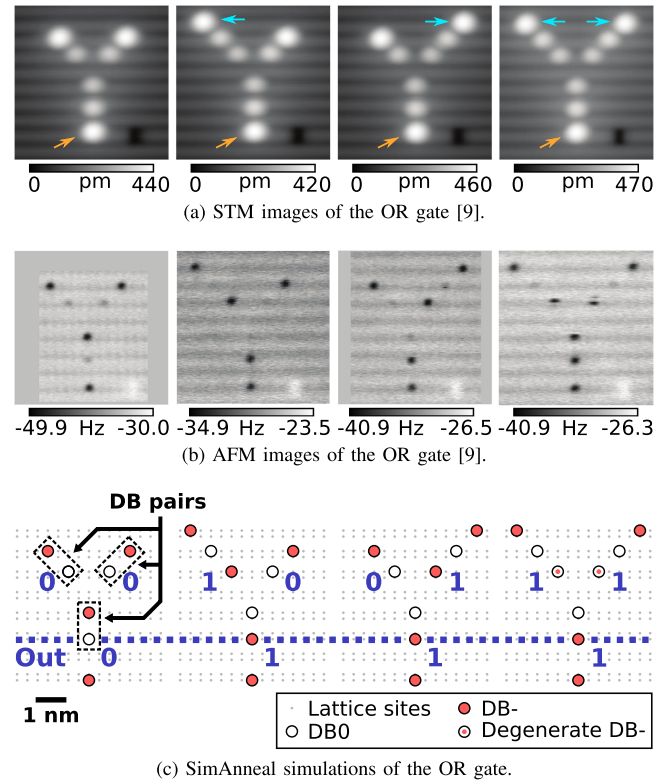
(c) SimAnneal simulations of the OR gate.

Fig. 2. A DB OR gate made of three pairs of binary dots studied in [9] toggled through all necessary truth states with perturbers. The logical output of the gate is determined by the charge state of the DB labeled 'Out': 0 and 1 for DB0 and DB− respectively. (a) STM images of the OR gate revealing all DB locations in white. The presence of perturbers at the top of the device (indicated by blue arrows) change the input state. The output perturber (indicated by orange arrows) acts to prevent a charge from occupying the lower output dot unless sufficiently repelled by charges in the upper half of the device. (b) Constant height AFM images revealing charge localization in the structure as the darker DB sites. (c) Simulated annealing results of the OR gate with the output perturber moved one lattice site lower for more reliable simulated performance. These charge configurations can be reached by a range of simulation parameters (ref. Fig. 5). Unfilled and fully-filled DBs are singly and doubly occupied respectively, while partially-filled DBs indicate shared charges in degenerate states. The radially placed DB pairs are also labeled. (a) and (b) initially appeared on Springer Nature, Nature Electronics, [9] (Huff *et al.*, Binary atomic silicon logic), © 2018.

through proximity based gating effects [19]. The charge states can be measured via AFM with examples included in Fig. 1(d).

The potential of DBs as building blocks for computational logic circuits has previously been demonstrated [9], where a binary OR gate that consists of 3 radially placed DB pairs as shown in Fig. 2(a) was proposed. Each DB pair conveys a single bit of information via the location of one negative charge within. The input logic states are actuated by the presence of *perturbers*, which are peripheral DBs energetically favored to remain in the DB− state regardless of the state of other DBs in the circuit. The output is given by the charge state of a particular DB. The charge states were measured via AFM in [9] exhibiting a tendency to relax to the system's ground state, as shown in Fig. 2(b). A simulated version of the OR gate is also shown in Fig. 2(c), with details to follow in Section IV-A.

Additionally, non-equilibrium charge dynamics were investigated in [10] via AFM experiments on a six DB structure shown in Fig. 3(a), which was designed to be energetically frustrated such that an electron has the tendency to localize on either of the innermost DBs. A "hopping" of the electron among those sites was observed as the structure was scanned, with each localization persisting over multiple line scans as shown in Fig. 3(b). In [10], the persistence is attributed to a stabilization of the charge states by lattice relaxation [20], [21], presenting an additional energetic barrier between the degenerate states that prevents elastic tunneling. The tip influence and thermal fluctuations likely contribute to overcoming this barrier. We were

able to simulate the ground state and the hopping phenomena of the frustrated ground states as shown in Fig. 3(c)–3(d), which will be discussed in Section IV-B.

The potential to construct nanometer-scale logic circuits from atomic DBs makes this technology a promising candidate for advancing the work in circuit miniaturization and power reduction. Further, the use of silicon substrate opens up possibilities to integrate DB circuits with existing infrastructures for silicon complementary metal-oxide-semiconductors (CMOS) devices. This is a new design space with largely unknown design rules and constraints; many more logic gates and circuit components still await investigation. The SiQAD project aims to reduce the barrier for the research community to explore this platform technology, as well as to develop design rules that will allow for effective design of complex circuits and systems at the atomic scale.

(a) AFM scan.

(c) Average occupation.

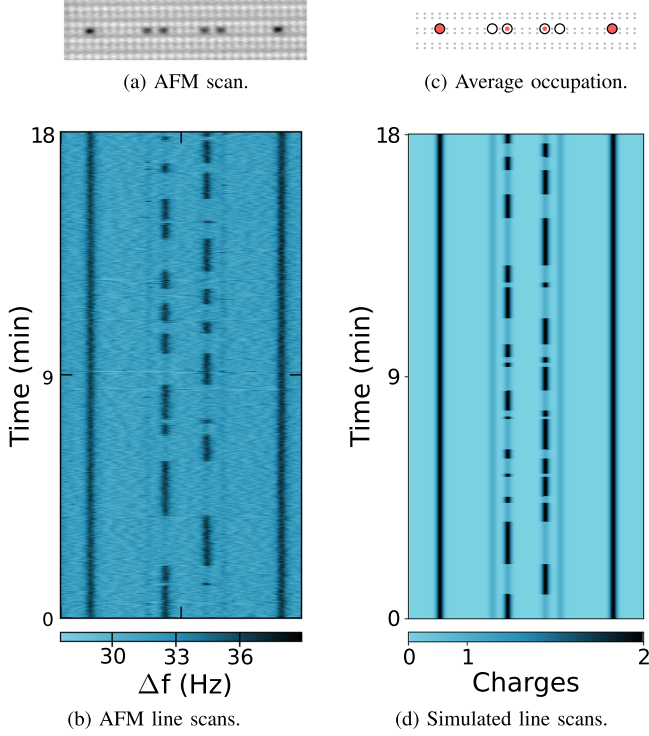(b) AFM line scans.

(d) Simulated line scans.

Fig. 3. Six DB symmetric structure studied in [10]. (a) AFM image of the structure, with two DB pairs in the middle and one perturber on each side. (b) Sequence of AFM line scans performed at 4.5K, repeatedly scanning back and forth along the center-line of the structure with a high tip-sample separation to reduce the tip influence. One charge is shared approximately evenly between the two inner DBs (ref. Fig. S3 in [10]) and is observed to maintain its occupancy over multiple line scans. (c) Simulated average occupation with SimAnneal with parameters $\mu_- = -0.08$ eV, $\epsilon_r = 5.6$, and $\lambda_{\text{TF}} = 5$ nm (ref. Section IV-A). (d) Dynamic simulation of the structure using HoppingDynamics with the Mott Variable Range hopping model with 800 line scans over 18 minutes showing similar results to (b). Reprinted Fig. 3(a) and 3(b) with permission from M. Rashidi *et al.*, Phys. Rev. Lett., 121, 166801, 2018 [10]. Copyright 2018 by the American Physical Society.

III. SiQAD Overview

SiQAD is a CAD tool that enables the design and simulation of DB circuits through an intuitive graphical user interface (GUI) and a modular simulation back-end. The GUI is written in C++ with the Qt cross-platform application framework [22] and provides tools for DB layout design, simulation management, as well as multi-layer electrode placement.

The SiQAD GUI communicates with simulation engines through a custom simulation application programming interface (API). Simulation engines may utilize this API via a provided class structure which supports engines developed in C++ or Python. The general procedure of a simulation upon user invocation is as follows: 1) SiQAD exports a file containing the simulation parameters as well as the DB and electrode designs; 2) the desired simulator is invoked with user-configurable command line arguments; and 3), result files generated by the simulator are read and parsed by SiQAD, with supported result types displayed in the GUI. Currently supported result visualization types include DB charge state configurations and electrostatic landscape results. Simulation engines may also instruct SiQAD to perform design actions such as the creation, movement, and

removal of design objects through an instructions API. Three simulation tools are included with the initial release of SiQAD, with their features and functionalities detailed in the proceeding section. Additional engines can be implemented and incorporated through the provided APIs.

The source code and binaries of SiQAD and associated simulation tools are publicly available at [23]. The open-source tools allow the research community to modify or contribute additional functionalities, supporting the future growth of SiQAD as a DB circuit design platform.

IV. Simulation Engines

Three simulation engines are officially included in the initial release of SiQAD, each with different purposes and capabilities as detailed below:

SimAnneal: simulated annealing algorithm for finding metastable low energy charge configurations.

HoppingDynamics: non-equilibrium electron hopping dynamics simulation intended for capturing the experimentally observed hopping behavior in [10].

PoisSolver: electrostatics solver which solves the generalized Poisson's equation to find the electric potential landscape arising from clocking electrodes in the system.

In SiQAD's simulation setup interface, multiple simulations can be chained in sequence and inter-engine data flow can be facilitated. This is particularly useful for directing electrostatic landscape results generated by PoisSolver to SimAnneal or HoppingDynamics.

A. SimAnneal: Low Energy Charge Configuration Simulator

1) Working Principle: SimAnneal is a heuristic algorithm for simulated annealing which attempts to find the ground state metastable charge configuration for given DB layouts. The energy of a charge configuration, $\vec{n}$, is given by

$$E(\vec{n}) = \sum_i V_i^{\text{ext}} n_i + \sum_{i<j} V_{ij} n_i n_j \tag{1}$$

where V_i^{ext} is the total contribution of external potential sources at the ith DB with the exception of influences from other DBs, n_i is the charge state at each DB with possible values $n_i \in \{-1, 0, +1\} \mapsto \{DB-, DB0, DB+\}$, and V_{ij} is the strength of the Coulombic interaction between DB sites. SimAnneal consists of two major components, *surface hopping* and *population control*, that contribute to finding low energy stable charge configurations.

During the surface hopping phase, attempts are made to hop electrons or holes to neutral sites, with these hops being accepted via an acceptance function. Past analyses of experimental results have fitted the inter-DB charge interaction to the screened Coulomb potential [9], [18], of the form

$$V_{ij} = \frac{q_0}{4\pi\epsilon} \frac{1}{r_{ij}} e^{-r_{ij}/\lambda_{\text{TF}}} \tag{2}$$

with r_{ij} the distance between the DBs, λ_{TF} the Thomas-Fermi screening length, and $\epsilon = \epsilon_0 \epsilon_r$ where ϵ_0 is the vacuum permittivity and ϵ_r is the effective dielectric constant at the surface. The
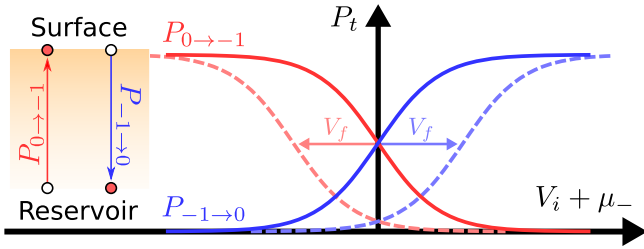
Fig. 4. Population update probabilities for electrons to hop on or off DB sites as a function of the local potential. V_f introduces an artificial barrier between the surface and the reservoir, which increases over the course of the annealing schedule to restrict hopping and fix the surface charge population. A similar mechanism is used for holes.

dielectric constant affects the strength of electric fields, while the screening damps charge interactions at a distance exponentially.

The population control phase assesses the effect of band bending on the charge transition levels (Fig. 1(c)) and updates the electron population in an attempt to produce electron configurations that satisfy the following conditions: DB sites should be doubly occupied when the DB(0/-) charge transition level is below the Fermi level, vacant when the DB(+/0) charge transition level is above the Fermi level, and singly occupied otherwise. Band bending effects that contribute to all DBs approximately equally, such as those due to spatially broad inhomogeneity, are captured in a chemical potential, $\mu_- = E_s - E_F^{Si}$, where E_s is the DB(0/-) charge transition level of a single isolated DB and E_F^{Si} is the bulk Fermi level; μ_+ is the DB(+/0) charge transition level equivalent, which can be expressed as $\mu_+ = \mu_- - \mathcal{E}$ where $\mathcal{E}$ is the potential between the charge transition levels taken to be 0.59 eV [19]. Other environmental band bending effects, such as those due to modulation fields and stray charged dopants, can be encapsulated in V^{ext}. Local band bending effects for individual DB sites are expressed as

$$V_i = -V_i^{ext} - \sum_j V_{ij} n_j. \tag{3}$$

For each SimAnneal iteration, electrons hop between DB sites and an imaginary reservoir that can provide or contain any number of electrons according to a heuristic method inspired by Fermi-Dirac distribution:

$$P_{0 \to n_i}(V_i) = P_t(-n_i(V_i + \mu_{n_i}))$$

$$P_{n_i \to 0}(V_i) = P_t(n_i(V_i + \mu_{n_i}))$$

$$\text{where } P_t(V_{offset}) = \frac{1}{1 + e^{(V_{offset} + V_f)/(k_B T)}}. \tag{4}$$

Here, $P_{from \to to}$ indicate the transition probabilities between charge states for the ith DB; V_f is the *freeze out* potential, an artificial energy barrier between the reservoir and DB sites which is increased in each iteration to gradually inhibit hopping and tends to fix the number of electrons at the surface; and $k_B T$ is an artificial thermal energy that decreases over the course of the simulation according to the annealing schedule. Direct transitions between DB− and DB+ are not allowed in this

model. Fig. 4 illustrates the role of V_f in the population update mechanism.

At the end of the annealing schedule, the metastability of generated results are evaluated based on the following criteria: *population stability*, where the charge state of each DB must be consistent with the energetic position of the charge transition levels relative to the Fermi energy after accounting for band bending; and *configuration stability*, where no lower energy charge configurations exist that can be reached within a single hop event. The lowest energy metastable state observed is presented to the user in SiQAD.
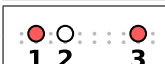
Note that this heuristic method assumes that the charge system is given sufficient time to relax to the ground state; actual tunneling rates between the DB and external charge sources are not considered. This makes SimAnneal well-suited for fast prototyping of DB layout designs, but not for real-time dynamic field-modulated simulations. The inclusion of physical intuition in this ground state finder through the hopping and population update mechanisms allows SimAnneal to be much more efficient in exploring the problem space than random bit-flip methods found in generic simulated annealing algorithms. For comparison, alternative ground state finders using quadratic unconstrained binary optimization (QUBO) have also been explored via a two-state approximation (DB0 and DB−). SimAnneal consistently outperformed all tested QUBO solvers under the two-state approximation, including Isakov et al.'s SimAn [24], D-Wave's Qbsolv [25], and D-Wave's quantum processing unit [26].

With DB configurations designed with extreme compactness, or fabricated on surfaces with very strong Coulombic interactions (very low ϵ_r), ground states given by Eq. (1) may contain DB− and DB+ sites at close proximity and still satisfy metastability conditions. However, no such experimental results have been observed. The lack of such observation may be due to the influence exerted by the AFM or STM scanning probes, or it may be an indication of missing metastability conditions in the ground state model. This will be further considered in future work, but does not affect the intended purposes of the simulation tool at the DB densities and parameters considered for logic design in this work.

2) Simulation Results: Physical parameters across separately prepared silicon surfaces may differ for many reasons [9], with examples including differences in doping level, slight deviations from preparation procedure, and bulk or surface defects. In the context of the ground state simulation model, variations in ϵ_r, λ_{TF}, μ_-, and μ_+ may result in different ground state charge configurations for the same DB layout.

We first verify SimAnneal's simulation results using a set of experimental results with known physical parameters. On a surface found to have $\epsilon_r = 5.6$, $\lambda_{TF} = 5$ nm, and $\mu_- = -0.231$ eV, the DB(0/-) transition levels in a biased DB pair depicted in Table I were measured and analyzed in [9] (ref. Fig. 2 in [9] for experimental results). The raw experimental data was reanalyzed in this work using the same analysis procedures in [9] and compared against simulation results as shown in Table I. SimAnneal produced identical ground state charge configurations, and returned V_i values (ref. Eq. (3)) that matched closely with those

TABLE I
LOCAL POTENTIALS OF BIASED DB PAIR

Setup	Method	V_i at each site		
		V_1	V_2	V_3
1	Measured (eV)	0.0	–	–
	SimAnneal (eV)	0.0	–	–
	Diff (%)	0.0	–	–
1 2	Measured (eV)	0.0	0.280	–
	SimAnneal (eV)	0.0	0.287	–
	Diff (%)	0.0	2.50	–
1 2 3	Measured (eV)	0.055	0.407	0.054
	SimAnneal (eV)	0.056	0.378	0.056
	Diff (%)	1.82	−7.13	3.70

extracted from experimental data. Note that the V_i values given for the unbiased DB pair is for the left-occupied degenerate state.

Proceeding to the OR gate structure from [9], the experiments were conducted on a separate surface from that of the biased DB pair from Table I. As mentioned at the beginning of this Simulation Results section, there exists physical property variations despite the employment of similar surface preparation procedures. Without making physical alterations to the OR gate, SimAnneal is only able to reproduce the experimental charge configurations across all input combinations at $\lambda_{TF} > 9$ nm and $\epsilon_r > 10$ with very narrow ranges of ϵ_r values for each λ_{TF} value. While we do not completely preclude the possibility of the silicon surface coincidentally satisfying those parameters, the experimental charge configuration could also have been influenced by the AFM tip or nearby non-uniformities such as the bright spots near the output perturber seen in the AFM images.

Although we have reservations over the operational parameter range for an exact replication of the OR gate, we were able to achieve a much larger operational range simply by moving the output perturber down by one lattice site (2.34 Å). The much increased operational range is a highly desirable feature, ensuring gate robustness across a broader range of surface physical parameters. To avoid confusion, we denote the OR gate from [9] as "OR_{Huff}" and the modified version "OR_{Mod}". Fig. 2(c) shows the simulated ground state charge configurations for OR_{Mod} which are achievable with a wide range of ϵ_r and λ_{TF} values at various μ_- values. This is shown in Fig. 5, which sweeps across the parameter set $\{\epsilon_r, \lambda_{TF}, \mu_-\}$ to find the operational range for each input combination as well as the operational intersection. The sweep bounds of $\{\epsilon_r, \lambda_{TF}\}$ were chosen to encompass their values fitted in past experimental results [9], [18], [27]. For each input combination, we observe a contiguous operational window of ϵ_r and λ_{TF} combinations at each μ_- value where the desired charge configuration is achieved; changes in μ_- translates the boundaries of these operational windows along the ϵ_r axis in log-log scale.

Different implementations of the same gate may operate over different ranges of parameters. Physical parameter sweeps of an alternative OR gate design (OR_{Cmpt}) with more compact DB placements than OR_{Huff} have been performed as shown in Fig. 6. At the same μ_- value, the operational range of OR_{Cmpt} encompasses ϵ_r values that are greater than those of OR_{Mod}.
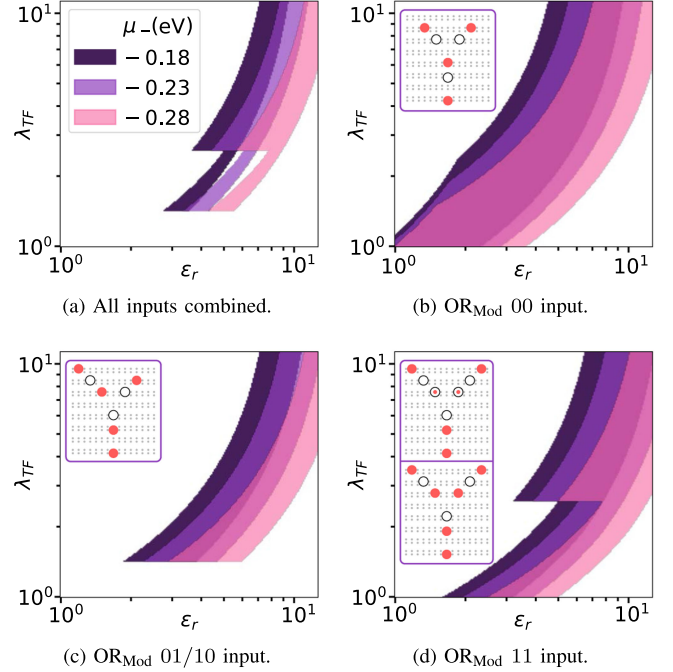

Fig. 5. Operational ranges of OR_{Mod} acquired by sweeping the physical parameter set $\{\epsilon_r, \lambda_{TF}, \mu_-\}$. Shaded regions indicate parameter sets which lead to the operational ground state shown at the top left of each sweep plot. Changes in μ_- leads to a horizontal translation of the plots in log-log scale.

This shift in operational range, which corresponds to a reduction in Coulombic repulsion, agrees with the intuition that a more compact version of OR_{Mod} would prefer to operate under conditions with weaker inter-DB interaction.

Distinctive features can be observed at the boundaries of the operational ranges in Figs. 5–6. To aid the interpretation of these boundaries, maps delimiting changes in ground state charge counts for each input combination of OR_{Mod} have been included in Fig. 7. The ground state charge population tends to decrease in the direction of rising λ_{TF} and falling ϵ_r, and tends to increase in the opposite direction. This agrees with the intuition that stronger inter-DB repulsion makes it unfavorable for neutral DBs to acquire new charges of the same sign. Two types of boundaries have been identified from these maps: *population* and *interaction boundaries*. The former is dependent on both ϵ_r and μ_- and involve a change in preferred population, causing the operational ground state to cease functioning; the latter is only dependent on λ_{TF} and involve a change in preferred ground state with the same population. A detailed analytical model of these boundaries is under development and will be presented in a future publication.

Lastly, Fig. 3(c) shows the simulated ground states of the six DB symmetric structure from [10]. The perturbers on both sides are always doubly occupied, exerting an inward bias on the electron occupying the sites in-between. One electron is equally shared between the two inner DBs. This is in agreement with the experimental results of [10] shown in Fig. 3(b), where the middle electron hops between the inner DBs. Like OR_{Mod}, the same ground state can be achieved for the six DB symmetric structure under a variety of $\{\epsilon_r, \lambda_{TF}, \mu_-\}$ parameters. Although
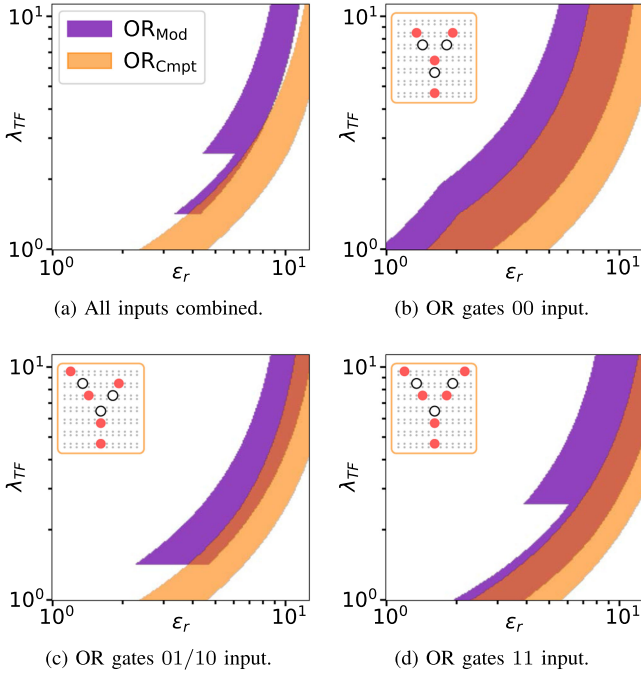
(a) All inputs combined.

(b) OR gates 00 input.

(c) OR gates 01/10 input.

(d) OR gates 11 input.

Fig. 6.   Operational ranges at $\mu_- = -0.23$ eV for OR_{Mod} and an alternative design, OR_{Cmpt}, which is shown at the top left of each sweep plot. The compactness of the alternative design allows OR_{Cmpt} to function in surfaces with weaker Coulombic interactions due to higher dielectric constant.

V_i values for the structure were presented in [10] (ref. Fig. 2 d in [10]), the estimated physical parameters used in that model predated the fitting done in [9] and [18], making it not a definitive benchmark to reproduce.

B. HoppingDynamics: Non-Equilibrium Dynamics Simulator

1) Working Principle: HoppingDynamics is a non-equilibrium electron dynamics simulator that treats electron transitions via hopping rates. The simulator is generalized to allow for various forms of hopping rates depending on the choice of hopping model. Two hopping models have been implemented: Mott Variable Range hopping [28] and Marcus hopping [29]. HoppingDynamics only accounts for the DB0 and DB− states since they are presented as the predominant charge states used for logic in [9] with the electrostatic energy of charge configurations taken to be of the form in Eq. (1). The rate of hopping for a charge from the ith (DB−) to jth (DB0) site is taken to be of the form

$$\nu_{ij} \propto e^{-2\alpha r_{ij}} \eta(\Delta G_{ij}) \tag{5}$$

with r_{ij} the distance between the DBs, ΔG_{ij} the change in Gibbs free energy associated with the hop, α the spatial decay of the hopping rate, and η some function of ΔG_{ij}. The change in Gibbs free-energy is taken to be

$$\Delta G_{ij} = \Delta E_{ij} + \rho_i \tag{6}$$

with ΔE_{ij} the change in Eq. (1) associated with the change in charge state and ρ_i an additional "self trapping energy," added to capture the DB− level deepening due to lattice relaxation and taken to be equal for all occupied sites.

If the average hopping rate, ν_0, between two degenerate DBs at some distance r_0 is known, the hopping rates can be expressed as

$$\text{Mott} : \nu_{ij} = \nu_0 e^{-2\alpha(r_{ij}-r_0)} e^{-\Delta E_{ij}/k_B T} \tag{7a}$$

$$\text{Marcus} : \nu_{ij} = \nu_0 e^{-2\alpha(r_{ij}-r_0)} e^{-\Delta E_{ij}[\Delta E_{ij}+2(\rho_i+\lambda_0)]/4\lambda_0 k_B T} \tag{7b}$$

where λ_0 is a reorganization energy. At each instant in time, a hop from i to j occurs with probability $P_{i\to j} = \nu_{ij}dt$. A spatial decay of $\alpha = 1$ nm^{-1} is assumed, with ν_0 and r_0 taken from the combined AFM line scans in [10]. Future experimentation will be used to refine the calibration of the hopping rates.

Charge population can be modeled by including additional channels for hopping to and from the surface DBs. As an example, charges hop from DB− sites to the bulk and from the bulk to DB0 sites with respective rates $\nu_{i,B}$ and $\nu_{B,i}$:

$$\nu_{i,B} = \nu_B f(-(V_i + \mu_-) + \rho_i) \tag{8a}$$

$$\nu_{B,i} = \nu_B f(V_i + \mu_-). \tag{8b}$$

Here, ν_B is an attempt frequency and f some function of the energy difference between the Fermi level and the DB(0/-) charge transition level. In these results, f is taken to be a logistic function and ν_B is sufficiently high such that surface-bulk transitions are, from the computational standpoint, immediately allowed once the DB(0/-) charge transition level passes the Fermi level.

2) Simulation Results: The six DB symmetric structure from [10] has been simulated with HoppingDynamics. DB charge states were measured according to a tip scanning at 8.9 nm/s for 800 line scans to match the experimental time scales with the tip influence ignored. An example result is shown in Fig. 3. Like the experimental results from [10], the structure always contains 3 doubly charged sites with similar hopping between the two innermost DBs. The OR gate results were also simulated. Identical results to SimAnneal were achieved for OR 00, 01, and 10. For OR 11, hopping between the two half filled DBs in Fig. 2(c) was observed.

C. PoisSolver: Electrostatics Solver

1) Working Principle: Electron occupation on the surface may be controlled by shifting the DB charge transition levels with respect to the bulk Fermi level. The control of Fermi levels demonstrated so far involves either doping [19], which cannot be changed after fabrication, or AFM tip-induced band bending [10], [16], which is not scalable to device-wide modulation. We envision that future DB circuits will rely on buried or suspended electrodes with controllable potentials to adjust the surface electron population, allowing fine control of information flow. Sections of the circuit may be switched 'off' by applying a voltage that induces upward band bending on the surface until the desired DBs reach the DB0 state; they may be switched 'on' by inducing downward band bending until the necessary electron population has been reached. In order to better understand the behavior of the DBs under the influence of electrodes,
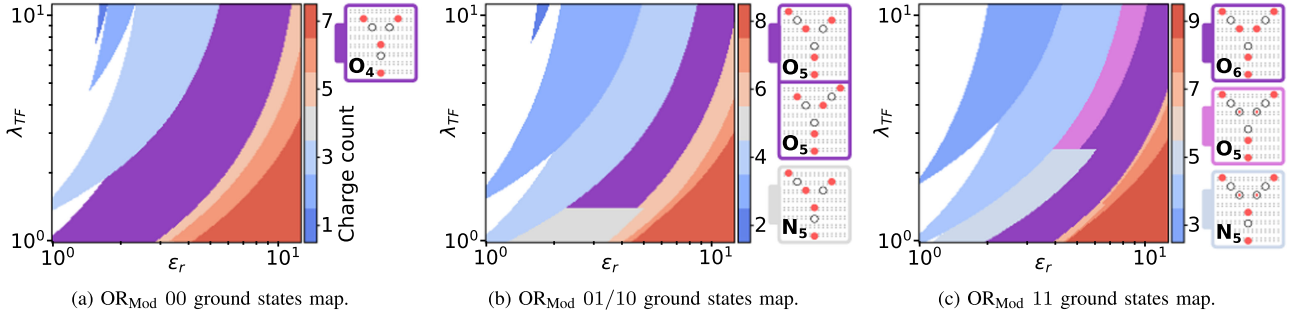
(a) OR_{Mod} 00 ground states map.

(b) OR_{Mod} 01/10 ground states map.

(c) OR_{Mod} 11 ground states map.

Fig. 7. Map of ground state charge populations of OR_{Mod} acquired by sweeping the physical parameter set $\{\epsilon_r, \lambda_{TF}\}$ at $\mu_- = -0.23$ eV. Notable charge configurations are depicted next to each map with their frame colors matching the corresponding region on the map. They are labeled O_n or N_n indicating whether the state is operational or non-operational and its charge count n. Regions colored white have no metastable ground state unless coexistence of DB− and DB+ states at close proximity are allowed; they are denoted "null regions" in this work. (a) OR_{Mod} 00 sweep map showing an operational region, O_4, that stretches through the entire λ_{TF} sweep range; the bordering regions to the left and right have a respective decrease and increase in charge count. We denote these borders "population boundaries". A null region also borders the lower left side of O_4, indicating significant upward band bending exerted by charged DBs. (b) OR_{Mod} 01/10 sweep map showing an operating region similarly sandwiched by population boundaries, with an extra horizontal boundary at the bottom not seen in OR_{Mod} 00. The neighboring state below the horizontal boundary, N_5, has the same charge count but a different ground state charge configuration due to changes in DB interaction distance. These horizontal borders are denoted as "interaction boundaries". (c) OR_{Mod} 11 sweep map showing an interaction boundary between O_5 and N_5, as well as a slight protrusion of N_5 into O_6. This indicates that different ground states sharing the same charge count (in this case, O_5 and N_5) do not necessarily share the same population boundaries.

the effect of the electrodes on the surface potential must be quantified.

PoisSolver, a finite element method solver supporting multiple electrostatics approximation models was implemented in Python using the FEniCS software package [30]–[36]. The simulation engine is able to account for user-defined design parameters, most notably the geometrical dimensions of the sample and the electrodes, and the resolution of the finite element mesh. The physical scope of the simulation includes the silicon substrate and its doping profile, the silicon surface, the dielectric above the surface, and the electrodes. The ground plane is set to be at the bottom of the simulated bulk.

Upon invocation of the simulator, a mesh is defined and generated according to the provided geometry and resolution, and the generalized Poisson's equation is solved over the mesh. Variable mesh generation is implemented such that the mesh contains finer detail at material boundaries (e.g. electrodes and silicon surface), while other areas will have a coarser mesh. The mesh definition is then passed to Gmsh to generate the appropriately formatted mesh for simulation [37]. When the computations are complete, the potentials are written to a file which can be used in other engines. A two-dimensional slice of the potential is extracted and displayed to the user in a color map. For time-varying clocking fields, the electrode potentials are adjusted with each simulation time step, and PoisSolver is used to recompute the potential landscape.

PoisSolver offers four physical models, the nonlinear Poisson-Boltzmann Equation (NPBE) [38], the linearized Poisson-Boltzmann Equation (LPBE) [38], the Poisson's equation (PE), and Laplace's Equation (LE). Using the NPBE, the movement and effect of mobile charges in the bulk can be accounted for in electric potential simulations. Linearizing the NPBE about 0 V reference results in the LPBE, also commonly known as the Debye-Hückel approximation used for electric field screening analysis. At the silicon surface, the potentials for a clocked system solved by the linear models each have a different offset

from those solved by the NPBE. The offset in the LPBE is due to the model being valid only for small values of electric potential, specifically when $\sinh(\frac{qu}{kT}) \approx \frac{qu}{kT}$. The difference between the PE model and the NPBE can be attributed to the PE neglecting charge migration. For the LE model, the constant offset is attributed to both the internal potential of the semiconductor due to graded doping and charge migration. The LE model can be made to match the PE model closely by considering the built-in potential of a non-uniformly n-doped semiconductor, something that the PE model inherently accounts for. The inclusion of multiple models allows for rough estimates using the linear models, saving the costly non-linear model for verification. Detailed description of the PoisSolver electrostatic models and a variety of simulation results will be presented in a future publication.

2) Simulation Results: In order to investigate field-modulated information flow via buried electrodes, an inverting DB wire structure was implemented in SiQAD with sinusoidally clocked 4-phase electrodes located 100 nm below the surface, as illustrated in Fig. 8. The mesh generated by PoisSolver and the electric potential of the cross-section are shown. An electrode clocking amplitude of 0.6 V was chosen to produce a ± 100 meV potential waveform at the surface in order to provide the appropriate amount of band bending to control DB states between DB0 and DB−. Simulation results of the clocked inverting wire using HoppingDynamics can be seen in Fig. 9.

V. DB LOGIC GATE DESIGNS

Using SiQAD, DB implementations of common logic gates including the AND, XOR, NAND, and XNOR gates have been designed and simulated as shown in Fig. 10. Like the wire and OR gate from [9], these logic gates represent bit information through the locations of charges in DB pairs. The charges at the inputs default to the logic 0 position, and tend to take the logic 1 position in the presence of input perturbers. In these designs, the
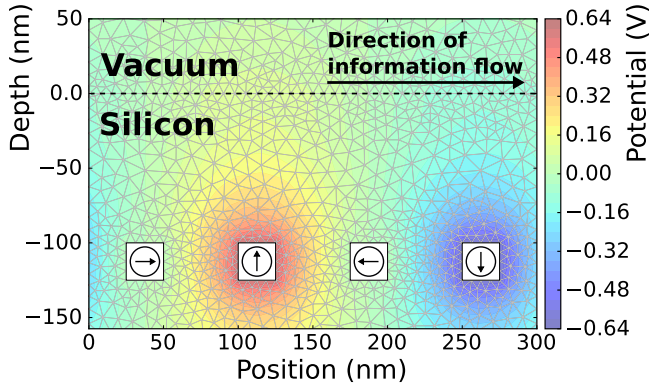
Fig. 8. A schematic of a buried electrode system with dimensions that are realistic for fabrication. The mesh was generated by PoisSolver, which was then used to solve for the potential landscape of the cross-section. The electrodes (white squares) have time-varying potentials in the form of sinusoidal functions, each with a $\frac{\pi}{2}$ phase offset from the nearest one to the left. These phases are indicated by the phasor inside each electrode.
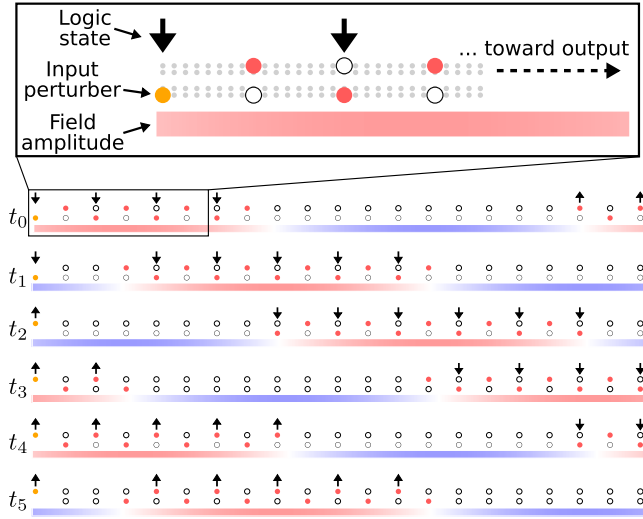

Fig. 9. Signal packet propagation using population clocking in an inverting wire. Shaded field amplitudes indicates the ± 100 meV surface potential waveform achieved using 4-phase electrodes 100 nm below the surface. The arrows indicate the logical state of the inverting wire. Note that by changing the input perturber during the depopulated phase between t_1 and t_2, two signal packets of opposite polarization are generated. To visualize the dots and packets for illustration, it was necessary to use electrodes 4 nm wide and separated by 8 nm. Similar results are achieved for larger electrodes. Lattice sites are omitted from the time-stepped visualization, but the spacing between DB pairs remain consistent with that shown in the magnified panel.

input combinations 01 and 10 are equivalent due to symmetry; the output logic states of the proposed gates are thus controlled by the count of logic 1 inputs. A change in the output state as a result of incrementing the count of input 1 s is viewed as crossing a *threshold*. Two types of thresholds have been identified, each exploiting a different physical phenomenon: the *push threshold*, where Coulombic repulsion leads to a reconfiguration of charges in the gate; and the *pop threshold*, where a shift in charge population occurs in the gate due to local potential changes influenced by the inputs. In the proposed logic gate designs, these thresholds are altered by varying the distances between

(a) AND gate.
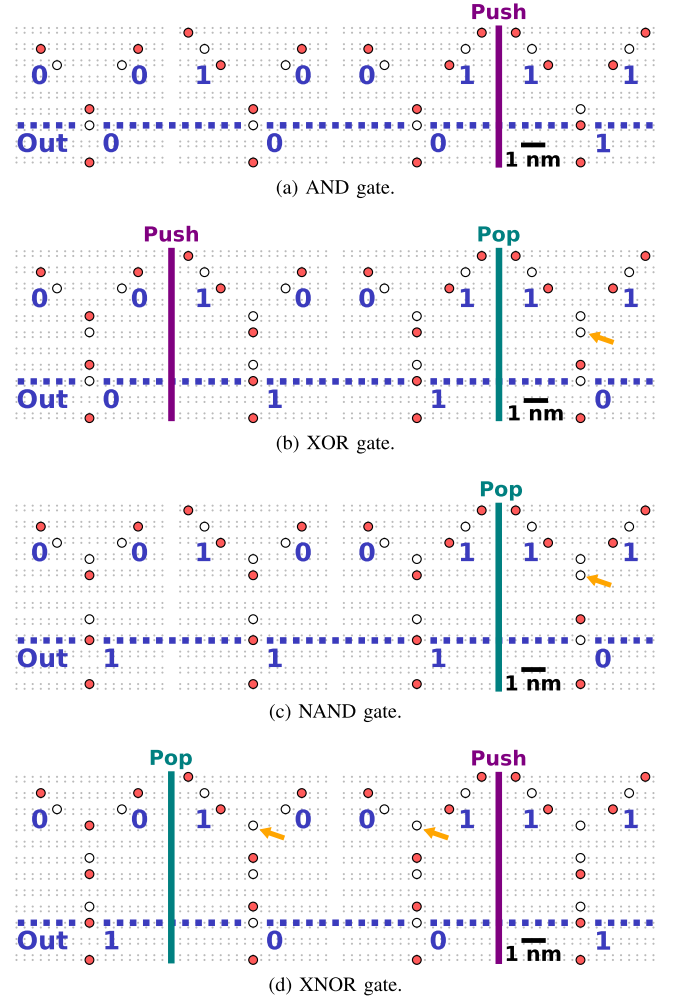
(b) XOR gate.

(c) NAND gate.

(d) XNOR gate.

Fig. 10. DB logic gate implementations designed in SiQAD with different logic behaviors achieved by tweaking the distances between the input and output DB pairs. Simulation results are produced by SimAnneal with $\mu_- = -0.28$ eV, $\epsilon_r = 5.6$, and $\lambda_{\mathrm{TF}} = 5$ nm. The inputs are at logic 0 by default; the addition of perturbers force those inputs to logic 1. Push and pop thresholds, where changes in the input states lead to changes in output states, are indicated. The orange arrows indicate locations where a charge has been ejected as a result of crossing the pop threshold.

the radially placed DB pairs that construct the gate. The push threshold is employed in the AND, XOR, and XNOR gates where Coulombic repulsion from inputs push the output to logic 1; the pop threshold is employed in the XOR, NAND, and XNOR gates where a charge is ejected from the gate output, leaving subsequent DB pairs to logic 0. When integrating these gates into circuit designs, modifications are often required to account for the local upward band bending arising from additional negative charges in the vicinity. The sensitivity of these logic gates to changes in surface parameters will be further investigated using an analytical operational boundary model in future work.

Using a combination of gates, a 2-input multiplexer has been designed in SiQAD as shown in Fig. 11; also included in the multiplexer is a fan-out design with one output inverted. Going further, the largest DB binary logic circuit designed thus far is a half-adder consisting of 72 DBs shown in Fig. 12. A
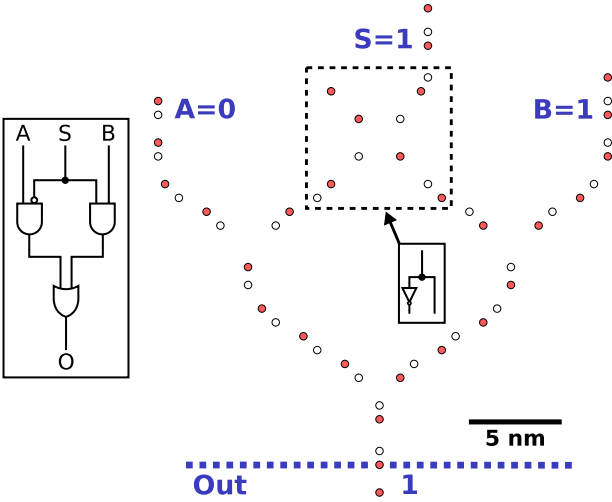
Fig. 11. A 2-input multiplexer designed with SiQAD and simulated using SimAnneal with $\mu_- = -0.32$ eV, $\epsilon_r = 5.6$, and $\lambda_{TF} = 5$ nm. The multiplexer consists of 2 AND gates, 1 OR gate, and a fan-out which has one inverted output as indicated.
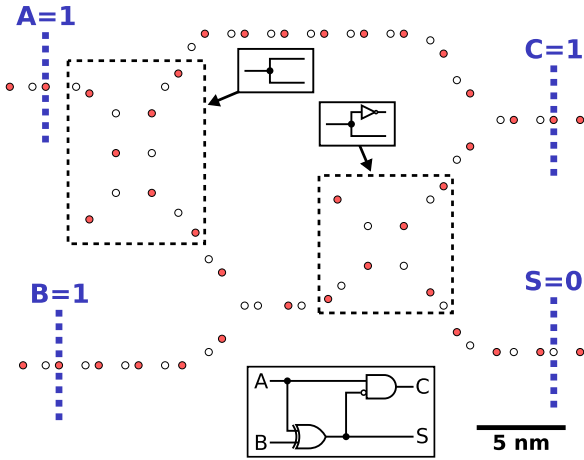

Fig. 12. Ground state simulation of a half-adder using SimAnneal with $\mu_- = -0.32$ eV, $\epsilon_r = 5.6$, and $\lambda_{TF} = 5$ nm. **A** and **B** are the inputs to be summed; **S** and **C** are the sum and carry respectively. All possible combinations in the truth table are satisfied.

Fig. 13. Crossover circuit allowing two binary dot logic wires to cross. Simulated using SimAnneal at $\mu_- = -0.31$ eV, $\epsilon_r = 5.6$, and $\lambda_{TF} = 5$ nm.

crossover circuit has also been designed and simulated as shown in Fig. 13. These circuits were simulated with a higher empirical chemical potential in order to achieve more compact designs; in practicality, electrode-based field-modulation is expected to be used to control the surface electron population through local band bending. It is important to note that the Y-shaped layout for logic gates employed here is only one of many possible ways to implement logic on the Si-DB physical platform; alternatives, such as quantum-dot cellular automata (QCA) [6], [39], are also worth further exploration.

VI. CONCLUSION

Motivated by recent developments in DB quantum dots, which have shown their potential to serve as emerging building blocks for atomic-scale logic circuits [9]–[11], we have developed SiQAD to enable the exploration of this new computational
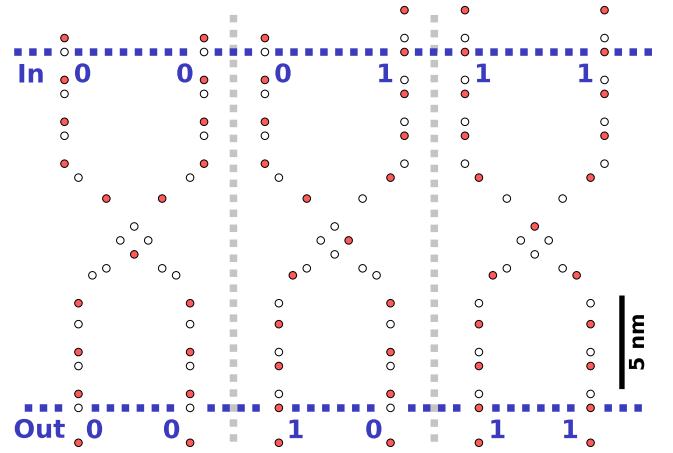
paradigm via the design and simulation of DB circuits. DB layouts from previous works have been recreated in SiQAD, with simulation results showing similar ground state charge configurations. By sweeping through key physical parameters in the ground state model, DB logic gates have been found to be operational under a range of physical parameters. The insights gained from SiQAD's ground state simulation capabilities have been used to propose additional DB logic gates and circuits, laying the groundwork for future logic designs on this platform. Furthermore, capabilities to perform charge dynamic simulations in DB systems as well as electrostatic landscape simulations with clocking electrodes enable the exploration of prospective clocked DB systems.

With an intuitive interface and integrated simulation tools, SiQAD is positioned to facilitate future investigations into this novel computational platform technology at a time when limitations to CMOS scaling have become evident. SiQAD's design and simulation functionalities will continue to be refined and improved. We encourage readers to follow this project's development at [23].

VII. CONTRIBUTION

K.W. initiated and guided the development of SiQAD. S.N., J.R., and H.N.C. developed SiQAD's GUI and simulation engines, as well as prepared the manuscript. R.L. contributed to SimAnneal and circuit designs. L.L., T.H., M.R., W.V., T.D., R.W., and K.W. contributed towards the interpretation of experimental results as well as the development of physics models. Additionally, T.H. provided Fig. 1(d) and conducted the reanalysis of experimental data shown in Table I. All authors reviewed and commented on the manuscript. We would like to thank the peer reviewers for their constructive feedback.

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