Experimental and Simulation Study of Silicon Nanowire Transistors Using Heavily Doped Channels

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***Abstract*—The experimental results from 8 nm diameter silicon nanowire junctionless field-effect transistors with gate lengths of 150 nm are presented that demonstrate on-currents up to 1.15 mA/μm for 1.0 V and 2.52 mA/μm for 1.8 V gate overdrive with an off-current set at 100 nA/μm. On- to off-current ratios above 10^8 with a subthreshold slope of 66 mV/dec are demonstrated at 25 °C. Simulations using drift-diffusion which include density-gradient quantum corrections provide excellent agreement with the experimental results. The simulations demonstrate that the present silicon-dioxide gate dielectric only allows the gate to be scaled to 25 nm length before short-channel effects significantly reduce the performance. If high-K dielectrics replace some parts of the silicon dioxide then the technology can be scaled to at least 10 nm gatelength.**

***Index Terms*—Electronic transport, 1D, junctionless transistor, scattering mechanisms, silicon nanowire, simulations.**

I. Introduction

Silicon nanowires have a multitude of potential applications, including transistors [1], [2], semiconductor memories [3], photovoltaics [4], thermoelectric generators [5], biosensors [6], colour selective photodetectors [7] and qubits [8]. The use of nanowires in commercial products, however, has to date been limited. A major challenge for transistor nanoelectronic applications is that, as transistor dimensions are reduced, it is difficult to maintain a low off-current (I_{off}) whilst simultaneously maintaining a high on-current (I_{on}). High I_{on} is fundamental for high gain and/or high speed in any transistor technology and is therefore one of the key parameters requiring optimisation.

Reducing I_{off} is significantly harder when transistor critical dimensions reach levels where quantum mechanical tunnelling, short channel effects [9] and statistical variability [10], [11] can be significant. A single gate in a MOSFET transistor becomes unable to provide sufficient electrostatic control to fully deplete carriers in the transistor channel, resulting in increased I_{off} values [12]. A variety of new architectures, including ultra-thin silicon-on-insulator (SOI) [13]–[15], double gate [13], [16], FinFETs [17]–[21], π- [22] / Ω-gate [23], tri-gate [19], junctionless [2] and gate all-around (GAA) nanowire transistors [24], [25] have therefore been developed to improve the electrostatic control of the conducting channel. This is essential since a low I_{off} implies low static power dissipation, and will therefore improve power management in the multi-billion transistor circuits employed globally in microprocessors, sensors and memory.

Here we demonstrate a solution by exploiting the quantum effects of a 1-dimensional (1D) Si nanowire. Whilst 1D devices have been produced in many material systems [26] here we demonstrate 1D nanowires in a scalable, top-down Si technology. According to the scaling theory of localization [27] metallic behavior from high doping can only occur in 3D semiconducting materials and not for systems with lower dimensionality (e.g. 1D nanowire system) where the transistor functionality will be preserved. Also we demonstrate by moving to 1D, a Si nanowire doped well above the 3D insulator-metal transition with high I_{on} whilst simultaneously providing excellent electrostatic control for a low I_{off} and a ratio between the two of 10^8.

Conventional MOSFETs running in inversion have a drain current, I_D, that improves with reduced gate-length L_g, since $I_D \propto \frac{\mu}{L_g}(V_g - V_T)^2$ where μ is the mobility, V_g is the gate voltage and V_T is the threshold voltage. As the dimensions of these conventional transistors are reduced, however, higher doping in the channel is required to suppress short channel effects, which in turn reduces the mobility, thus reducing I_{on}. The large vertical electric field required to form an inversion layer also significantly reduces the mobility, through interface roughness scattering [2]. A substantial volume of research is therefore focused on investigating new high-mobility channel materials to improve the drive current at lower voltages [28], [29]. Alternatively, the problem can be circumvented by developing a range

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of flat-band devices, such as the junctionless transistor [2]. This has a 3D wire-like channel rather than planar channel of MOSFETs, and acts as a gated resistor that pinches-off the carrier density of the wire by the application of a gate voltage. It is a normally-on device but by selecting a gate metal with an appropriate work-function, it can become a depleted, normally-off device. When switched on, and assuming flat-band conditions, I_D is due to the resistive behaviour of the channel and is given by

$$I_D = \frac{q\mu N_D A}{L_g} V_D \quad (1)$$

where q is the electronic charge, N_D is the channel doping density, A is the channel conducting area and V_D is the drain voltage. Thus, $I_D (= I_{\text{on}})$ again improves with reduced L_g. The channel doping can also be increased to improve I_{on} as the drive current is directly proportional to the electronic conductivity of the channel, given by $\sigma = q\mu N_D$. However, this cannot be increased arbitrarily because the higher the doping the closer the semiconductor will be to a nearly-metallic system, making the channel depletion for particular cross section very difficult. For P-doped Si, this implies a doping limit of 3.5×10^{18} cm^{-3} [30], although in small devices such as nanowires, surface state traps and donor deactivation [31] can actually reduce the activated carrier density, pushing the critical doping limit above the Mott criteria.

II. Fabrication

The transistors were fabricated from 55 nm SOI wafers from SOITEC with a 145 nm buried oxide. The Si channel was implanted with phosphorus at 15 keV to allow majority of dopants to sit at the bottom part of the channel with a dose of 4×10^{15} cm^{-2} before being annealled at 950 °C for 90 seconds to provide a doping density of 8×10^{19} cm^{-3}. Temperature dependent Hall bar measurements on large samples [32] were used to determine that the activated dopant density was 4×10^{19} cm^{-3}. This is well above the Mott criteria for Si:P, implying that the bulk material is strongly metallic in electronic behaviour [30] which is confirmed by the temperature dependence of the electronic properties [32]. The top Si was then etched to reduce the thickness for the smallest dimension nanowires before a Vistec VB6 electron beam lithography tool was used to pattern the nanowire using hydrogen silsesquioxane (HSQ) resist. Initially HSQ resist was used as an mask to etch 55 nm nanowires with 24, 16 and 8 nm widths, after which via holes were opened in PMMA resist to selectively thin down Si channel. A low damage SF_6/C_4F_8 inductivity coupled plasma etch [33] was undertaken before the resist was stripped and a thermal oxide grown at 950 °C. Optical lithography was then used to define electrical contacts using 20 nm of Ni and 50 nm of Pt after the oxide had been stripped with HF. An anneal in forming gas at 380 °C for 15 minutes was used to alloy the contacts forming NiSi Ohmic contacts with a specific contact resistance of 0.8 Ω-mm. Finally electron beam lithography was used with 400 nm of PMMA resist to lift-off the Al gate.

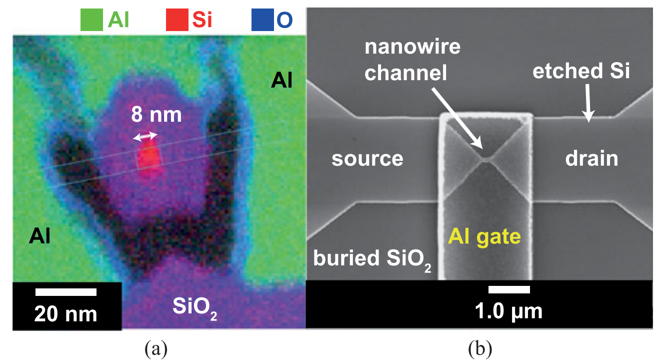

Fig. 1. (a) A cross sectional elemental map of the 8 ± 0.5 nm diameter nanowire with 16 nm SiO_2 thickness extracted from an EELS TEM image. (b) A SEM image of the gate over the top of the Si channel and parts of the source-drain regions. The nanowire length is 150 nm.

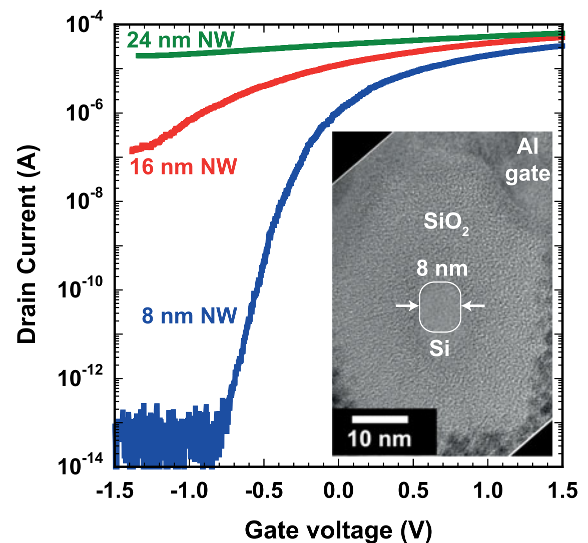

Fig. 2. The drain current, I_D as a function of gate voltage for Si nanowires with three different widths of 8 nm, 16 nm, and 24 nm. The drain voltage, V_D = 1.5 V and all measurements are at 293 K. The insert is an elemental map of a cross-section of the smallest nanowire, measured by TEM-EELS, which was used to determine the nanowire diameter.

The oxidation step resulted in the nanowires being suspended above the buried oxide of the substrate preventing a short gate-length being realised later in the fabrication process as reliable lift-off requires resist significantly thicker than any step height. A wide Al gate was therefore deposited by lift-off of total length of 2 μm but since the nanowire length was 150 nm, the effective gate-length, L_g is 150 nm. The gate oxide of 16 nm equivalent oxide thickness (EOT) for the devices has an integrated deep interface trap density, D_{it} below 10^{10} cm^{-2}eV^{-1} as extracted from measurements on test capacitors fabricated on the same chips. An electron energy loss spectroscopy (EELS) transmission electron microscope (TEM) image of the smallest nanowire with a diameter of 8 ± 0.5 nm is presented in Fig. 1(a) and the lateral geometry of the device is presented in Fig. 1(b). Fig. 2 also provides the TEM image of the 8 nm nanowire. The fabrication techniques and electronic properties of similar,

ungated, larger nanowires including the extraction of D_{it} have been published elsewhere [3], [32], [33].

The distance from source/drain contact to gate edge and Si channel is 4 and 5 μm respectively. Si channel along with source-drain regions were implanted in a single step to 4×10^{19} cm^3. NiSi was used to form ohmic contacts, where each contact had a transfer resistance of 0.3 Ω-mm, sheet resistivity of 60 Ω/m^2 and specific contact resistivity of 1.5×10^{19} Ωm^2. Each contact was designed to have an area of 5×10^{10} m^2 and by combining a square with a triangle narrowing to the nanowire allowed to reduce the access resistance and resulting in each contact having an overall resistance of 3 Ω.

Samples were prepared for TEM analysis using standard 'lift-out' procedures on a FEI Nova Dualbeam Focused Ion Beam system. TEM and STEM were conducted on a JEOL ARM200cF instrument equipped with a cold field emission gun that was operated at 200 kV and a CEOS (probe) aberration corrector. EELS data were collected using a Gatan 965 Quantum ER spectrometer using the Dual EELS [34] and Spectrum Imaging [35] methodologies. Energy dispersive x-ray spectroscopy (EDS) was conducted simultaneously using a Bruker XFlash detector.

The dc current-voltage characteristics were measured using an Agilent B1500 semiconductor parameter analyser at room temperature (293 K) with a Cascade Microtech probe station. For the ac lock-in measurements a constant voltage setup was used consisting of a 77 Hz 0.1 V amplitude ac sinusoidal signal from an Agilent 33521A function generator with a voltage divider (10 MΩ and 1 kΩ resistors) and the current measured using a 1 kΩ resistor with a Stanford Research SR830 lock-in amplifier.

III. Experimental Results

The drain current as a function of gate voltage, measured for nanowires with three different diameters, is presented in Fig. 2. The nanowire diameters were measured by TEM, using the extent of the crystalline lattice observed in cross-section (see Fig. 2) and confirmed using scanning TEM EELS maps, which clearly distinguishes the Si nanowire core from its SiO_2 surroundings, as illustrated in Fig. 1(a). Only the smallest, 8 nm diameter nanowire demonstrated good transistor characteristics, where the gate has excellent electrostatic control of the channel and with I_{on} to I_{off} ratios above 10^8. As the diameter of the nanowire increase to 16 nm then the I_{on} to I_{off} ratio reduces to ∼250 and for the 24 nm diameter nanowire I_{on} to I_{off} is only ∼2.5. For larger nanowire diameter devices (> 40 nm), no significant change in the current with gate voltage was observed. The subthreshold slope for the 8 nm diameter nanowire was 66 mV/dec which is close to the theoretical minimum of 60 mV/dec at room temperature whilst the 16 nm diameter nanowire had a subthreshold slope of 570 mV/dec.

For the 8 nm diameter nanowire the change in threshold voltages extracted at 10 mV and 1.5 V (see Fig. 3) was 159 mV, allowing the drain induced barrier lowering (DIBL) to be extracted as 106 mV/V. This is a relatively high value and is attributed to the thick gate oxide observed in Fig. 1, in addition to the fact that the Al gate is not completely wrapped around the nanowire. Indeed, the EELS map inset in Fig. 1(a) indicates that a void was around the underside of the nanowire rather than a complete wrap-around gate, probably due to resist not being completely developed before the Al gate was deposited (the black U-shaped region around the nanowire oxide). The Al gate directly contacts the nanowire oxide only at the top of the image. An optimised process will improve the DIBL performance in future devices and the simulations presented later in the paper will provide guidance over the required changes to improve performance.

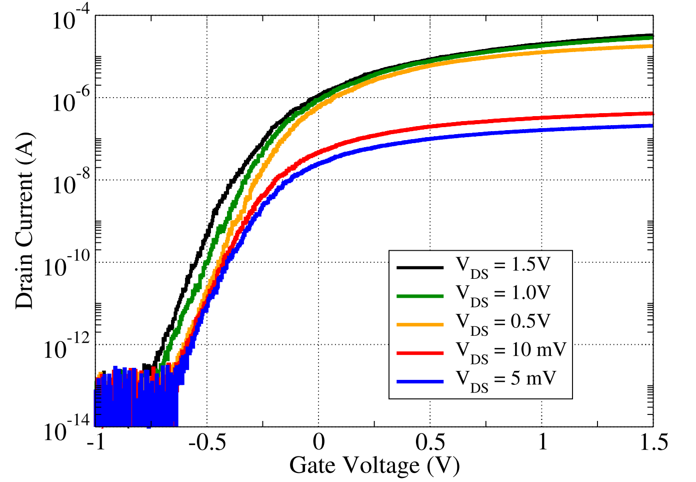

Fig. 3. The experimentally recorded drain current, I_D as a function of gate voltage for the 8 nm Si nanowire for a range of drain currents from 5 mV to 1.5 V at 293 K.

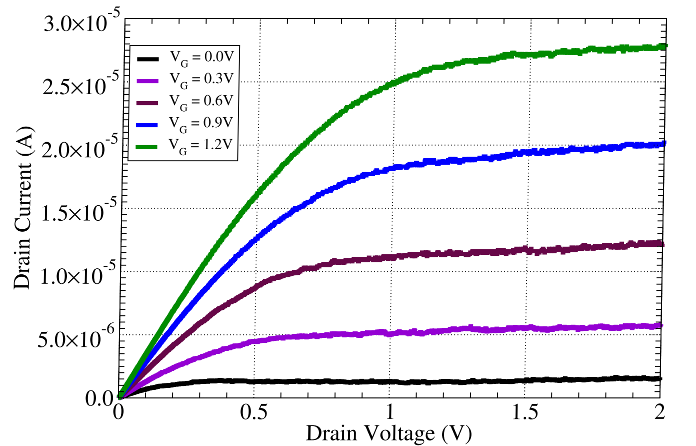

Fig. 4. The transfer characteristics demonstrating the experimentally obtained drain current versus source-drain voltage for a range of gate voltages from 0 V to 1.2 V at 293 K.

Figs. 3 and 4 summarise the variations in nanowire drain current during operation. Fig. 3 presents the dependence on the gate voltage for a range of source-drain voltages, V_{DS} whilst Fig. 4 demonstrates the dependence on drain voltage for a range of gate voltages. The peak transconductance was extracted as 26.5 μS (3.31 mS/μm) at $V_D = 1.2$ V. The raw current-voltage

data of Figs. 3 and 4 suggests that $I_{\rm on}$ is 2.7 times larger than that measured previously for 180 nm gate-length inversion mode Si nanowires with 5 nm diameter [24], although only by considering the gate overdrive voltage from a given $I_{\rm off}$ voltage can an accurate comparison with other results be made. Fig. 3 clearly demonstrates that a different metal with a work function higher then Al is required to achieve $I_{\rm off}$ at zero gate voltage. The threshold voltage as extracted by the transconductance to drain current ratio method is 0.18 V at $V_D = 1.5$ V. Setting the $I_{\rm off}$ at 100 nA/μm with a gate overdrive of 0.5 V produces a drain current of 165 μA/μm for the present 150 nm gate-length nanowires, which is relatively low compared to high mobility, 130 nm gate-length InAs devices with 601 μA/μm [29].

For a junctionless transistor the channel is a doped semiconductor so when the device is switched on the drift mobility in the channel is derived from Ohms law with the Drude model in the relaxation time approximation using (1). A drift mobility of 109 cm^{2}V^{-1}s^{-1}; was extracted from the channel at $V_G = V_D = 1.5$ V using the data in Fig. 2 and (1). Previous larger silicon nanowires in a Hall bar configuration measured with an ac constant current technique of 100 nA produced 70 cm^{2}V^{-1}s^{-1} [32] but those measurements had a geometrical uncertainty of a factor of two. The large experimental uncertainty in measuring the carrier densities in nanowires only allows these mobility results to be stated as comparable due to the large experimental geometrical uncertainty.

Comparing $I_{\rm off}$ at 100 nA/μm with a gate overdrive of 1.0 V, the present 150 nm gate-length nanowires have a drain current of 1.15 mA/μm, which is significantly higher than the 0.61 mA/μm measured previously from 25 nm gate-length Si MOSFETs [36] and the 0.62 mA/ um measured from 50 nm gate-length InGaAs MOSFETs [29]. Higher voltages provide even higher performance: for example, $I_{\rm off}$ at 10 pA/μm with a gate overdrive of 1.8 V, the present 150 nm gate-length nanowires have 2.52 mA/μm drain current. This is significantly higher than the 0.92 mA/μm from 80 nm gate-length high-voltage 3D trigate MOSFETs from a 22 nm system on chip commercial technology [19]. These results indicate that the present nanowires are better for higher voltage applications since the thick gate oxide and low mobility limits the low voltage performance.

IV. Simulations

All simulations in this study are carried out with the drift-diffusion (DD) module of the TCAD simulator GARAND [37]. In this particular case the DD approximation includes density-gradient quantum corrections (DG) [38]. Currently, in order to speed up the simulation, work is ongoing to calibrate the DG correction to the 2D Schrödinger-3D Poisson solver. The 2D Schrödinger solution for nanowires with smaller than 8 nm cross-section could provide a more accurate picture of the quantum confinement effects [39].

Fig. 5 compares the experiment and simulation results demonstrating that a good match between the experimental data and simulation results has been achieved. This good match between the experiment and the simulation is achieved by calibrating the electron mobility. The Masetti model is used to account for the doping dependence of the low field mobility [40], the Lombardi model accounts for surface acoustic limited mobility and surface roughness limited mobility [41], and the Caughey-Thomas field dependent mobility model is used to account for the saturation velocity [42]. Importantly, a correct calibration of the simulation results to the experimental data has been achieved not only for the low drain voltages but also for the high drain voltages. Small discrepancies, however, in the sub-threshold slope (SS) remain due to the fact that the 3D TCAD nanowire model is a smooth device without any source of statistical variability and oxide traps.

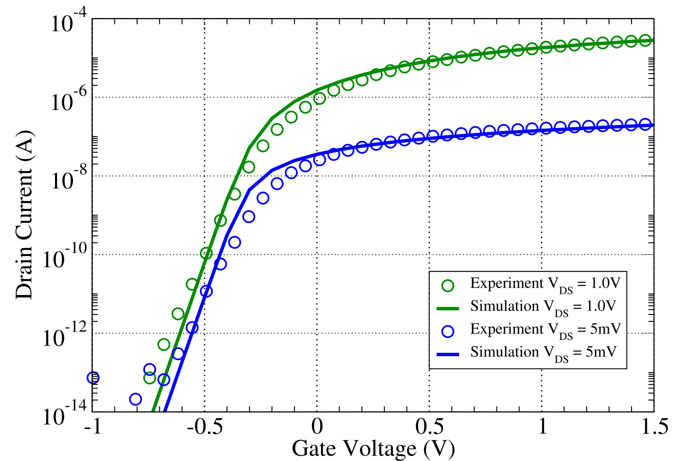

Fig. 5. A comparison between the experimental data (circles) and the simulation for V_{DS} of 1.0 V (green) and 0.005 V (blue).

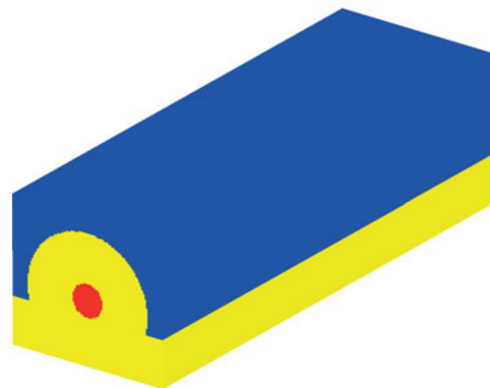

Fig. 6. A 3D view of the nanowire showing the used materials: red is an Si channel, yellow is an SiO_2 oxide and blue is a contact region.

Fig. 6 presents the 3D graphical representation of the simulated device. The simulated structure has identical device dimension and material parameters as the experimental device. Our 3D TCAD model is a junctionless nanowire transistor (NWT) with an 8 nm cross section and a 150 nm channel (gate) length. Guided by the experimental TEM images, we have chosen a 16 nm SiO_2 Ω-shaped gate oxide.

Fig. 7 shows a 2D cut through the middle of the device. As expected, the charge concentration increases as the gate voltage is increased. More importantly, it is visible from Fig. 7 that

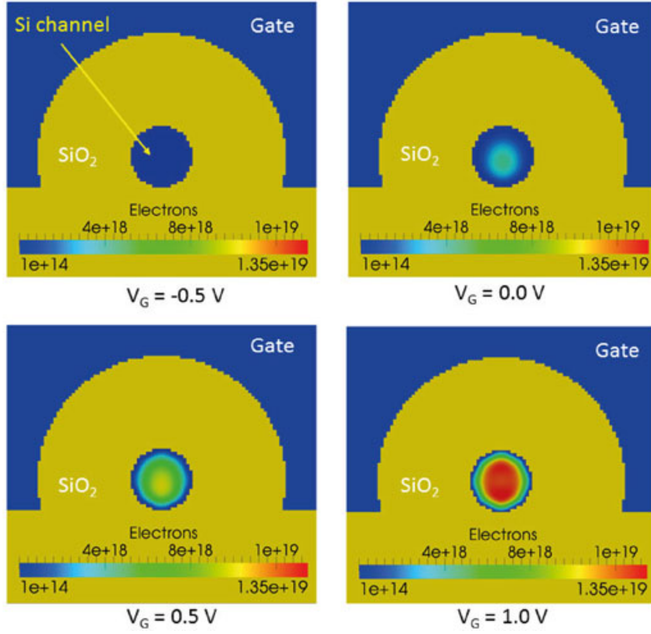

Fig. 7. A cut through the middle of the nanowire showing the cross section of the device. The electron density is shown in the channel region. Yellow is SiO_2 and blue is the contact region at high drain $V_D = 1.0$ V.

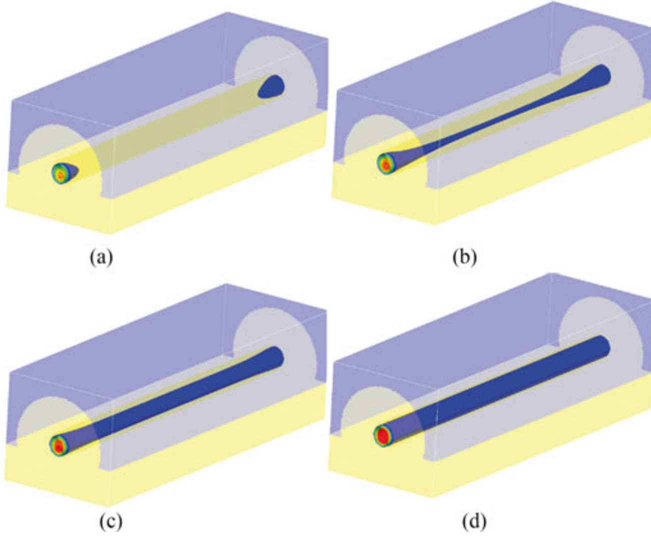

Fig. 8. The 3D electron density profile along the nanowire for $V_{DS} = 5$ mV. (a) $V_g < V_T$, (b) $V_g = V_T$, (c) $V_g > V_T$, and (d) $V_g >> V_T$.

the charge transport is through the middle of the channel, far away from the Si/SiO_2 interface. This observation is consistent with the operational mode of junctionless devices [2], [43]. It is also consistent with interface roughness scattering not being the mobility limiting mechanism for these nanowires as was previously demonstrated with larger nanowires produced by the same process [32]. When the gate voltage is below V_T, the device is in a depletion mode. In the case when the gate voltage is well above V_T, the transistor is in a partial depletion state.

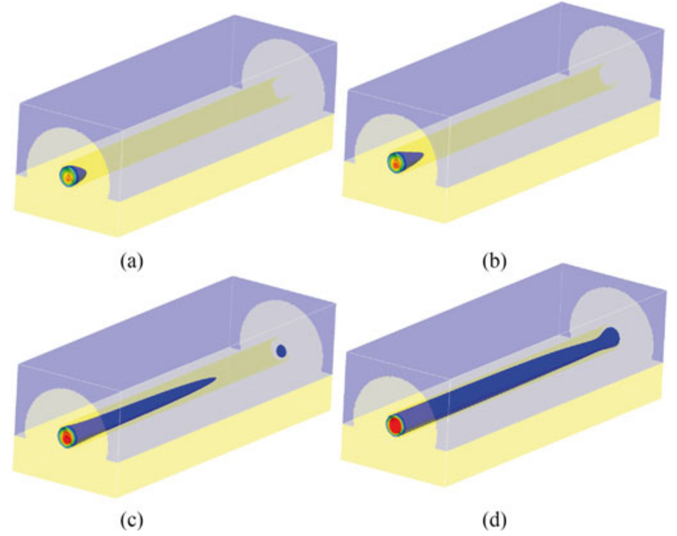

Fig. 9. The 3D electron density profile along the nanowire for $V_{DS} = 1.0$ V. (a) $V_g = -0.5$ V, (b) $V_g = 0.0$ V, (c) $V_g = 0.5$ V, and (d) $V_g = 1.0$ V.

Figs. 8 and 9 confirm the electron transport through the body of the channel. These figures demonstrate the electron charge distribution along the channel for different values of the gate voltage at low and high values, respectively. At the low gate biases the transistor is turned off due to an electrostatic pinch-off (see the top of Figs. 8 and 9). It is clear that the position of this pinch-off depends on the applied drain bias. At the high drain biases (see Fig. 9), the pinch-off region is close to the drain. On the contrary, at the low drain bias (see Fig. 8), the pinch-off is the middle of the device. At the high gate biases (see the bottom of Figs. 8 and 9), well above V_T, the device operates in flat-band conditions and, as a result, the current pathway is through the body of the transistor. As a result, we are confident that our simulation results not only can accurately reproduce the experimental $I_D - V_G$ curves but they also accurately capture the underlying physics in junctionless nanowire devices.

At present the gate length is significantly larger than commercial devices which are presently below 20 nm gatelengths. From the experimental point of view, therefore, it is important to know what is the minimal gate length at which the device will still behaves as a transistor at a particular channel doping concentration. In this case our simulations can provide the most efficient way to explore the numerous combinations of channel doping concentration and gate length.

In order to answer the above question, what is the minimal gate length at which the devicewill still behaves as a transistor at a particular channel doping concentration, three different channel doping concentrations and five different gate lengths are considered. Fig. 10 reveals the $I_D - V_G$ curves for junctionless nanowire devices with a doping concentration of 1×10^{19} cm^{-3} for five different gate lengths. The channel length is kept at 150 nm long while the gate is symmetrically reduced from both ends of the device. For example, in the case of the 10 nm device, the gate is exactly in the middle of the channel covering only 10 nm of the 150 nm long nanowire body. The same

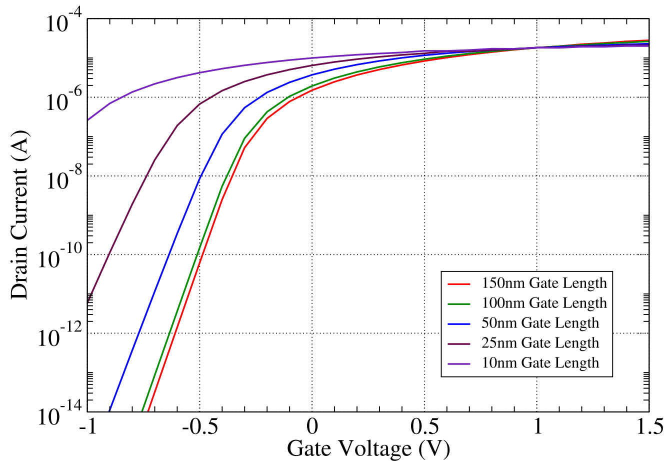

Fig. 10. The drain current vs. gate voltage for a channel doping density of 1×10^{19} cm^{-3}, $V_D = 1.0$ V and Si NWT with a diameter of 8 nm for five different gate lengths: 10 nm, 25 nm, 50 nm, 100 nm, and 150 nm.

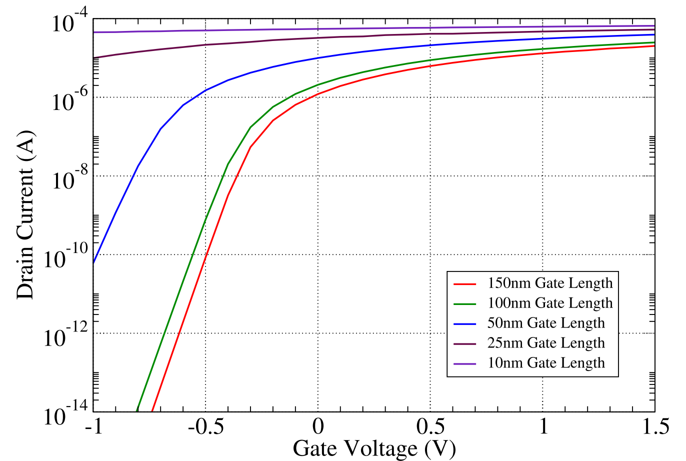

Fig. 12. Drain current vs. gate voltage for a channel doping density of 8×10^{19} cm^{-3}, $V_D = 1.0$ V and Si NWT with a diameter of 8 nm for five different gate lengths: 10 nm, 25 nm, 50 nm, 100 nm, and 150 nm.

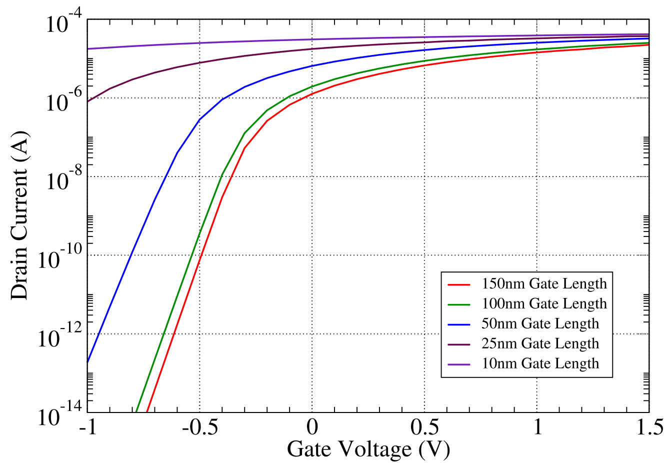

Fig. 11. Drain current vs. gate voltage for a channel doping density of 4×10^{19} cm^{-3}, $V_D = 1.0$ V and SI NWT with a diameter of 8 nm for five different gate lengths: 10 nm, 25 nm, 50 nm, 100 nm, and 150 nm.

approach has been used for all other gate lengths where the gate is kept centered in the middle of the device.

Fig. 10, also demonstrates that for this particular doping concentration of 1×10^{19} cm^{-3} transistor-like behaviour is observed all the way down to the 25 nm length gate. The devices with the 50, 100 and 150 nm gate lengths demonstrate good transistor-like behaviour with a SS of around 61 mV/dec and an $I_{\rm on}/I_{\rm off}$ ratio of around 10^8. The crossings of the $I_D - V_G$ curves at around $V_G = 1.0$ V occur due to the fact that when the gate length is decreased the wire behaves as a resistor. This can be compared to adding two resistors on both sides of the gate where the resistance increases with shortening the gate length.

Fig. 11 reveals similar conclusions to those presented in the previous paragraph for a set of devices where the doping concentration in the nanowire has been increased to 4×10^{19} cm^{-3}. The transistors with the 10 and 25 nm gate length, however, have a worse $I_{\rm on}/I_{\rm off}$ ratio in comparison to the same devices in Fig. 10. The reason being that the doping concentration is increased from 1×10^{19} cm^{-3} to 4×10^{19} cm^{-3} which leads to an increase of V_T. All other devices, however, with the gate lengths of 150 nm, 100 nm and 50 nm show a value of the $I_{\rm on}/I_{\rm off}$ ratio of at least 10^7.

Fig. 12 shows results when the channel doping is further increased to 8×10^{19} cm^{-3}. In this case both the 10 nm and 25 nm devices show almost perfect metallic behaviour with poor SS and little gate modulation. The 150 nm and 100 nm devices, however, keep the 10^8 $I_{\rm on}/I_{\rm off}$ ratio and an almost ideal SS. Hence, controlling the channel doping and the gate length is essential in order to maintain transistor-like behaviour with a good SS and $I_{\rm on}/I_{\rm off}$ ratio. More importantly, our simulation demonstrate that all devices with gate length bellow 10 nm at various channel doping concentrations have a high leakage current and a low $I_{\rm on}/I_{\rm off}$ ratio which cannot satisfy the criteria for scaling.

Improving the device behaviour and decreasing the gate length to below 25 nm can be achieved by introducing high-K materials in the oxide [19], [44]. This leads to a reduction of the effective equivalent oxide thickness (EOT) which in turn leads to an improvement of the electrostatic control of the channel. Indeed, this is clearly visible in Fig. 13 where the 16 nm oxide layer is compared to simulated devices where this oxide is is split into two regions: an 8 nm SiO_2 layer to maintain a low trap state density and 8 nm high-K layer to provide better electrostatic control. Both Al_2O_3 and HfO_2 high-K materials have been modelled and the results compared in Fig. 13. Introducing the high-K material improves the leakage current significantly and shifts the voltage threshold (V_T) to higher gate voltages in comparison to the pure SiO_2 gate oxide material. Also, the device with the highest dielectric constant (HfO_2) has the lowest leakage current and the highest voltage threshold (V_T).

As a next step, it is important to analyse the behaviour of the transistors with various gate-lengths when the EOT of the oxide is significant reduced to allow the gate-length to be scaled below 10 nm. Fig. 14 investigates a range of gate-lengths down to 5 nm when an EOT of 1 nm is achieved using 0.5 nm of

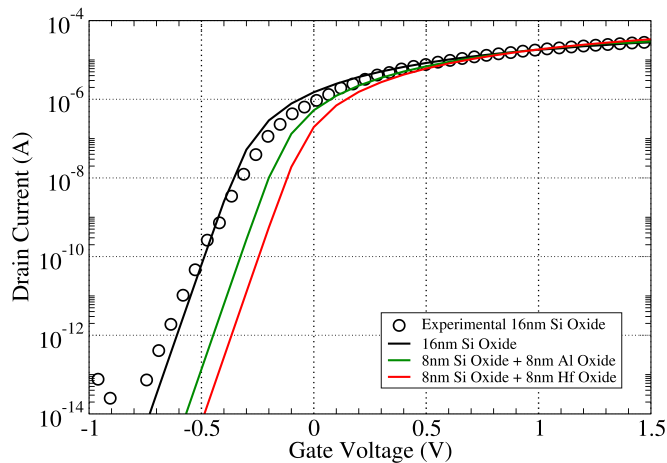

Fig. 13. Drain current vs. gate voltage. Comparison of the experiment and simulation results for a channel doping density of 1×10^{19} cm^{-3}, $V_D = 1.0$ V and Si NWT with a diameter of 8 nm for three types of oxide layers.

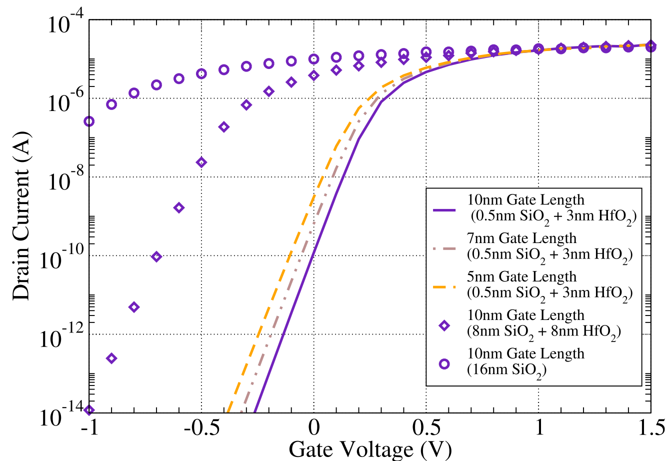

Fig. 14. Drain current vs. gate voltage for a channel doping density of 1×10^{19} cm^{-3}, $V_D = 1.0$ V and Si NWT with a diameter of 8 nm for three different gate lengths: 5 nm, 7 nm, and 10 nm with three different oxide thicknesses: 16 nm SiO_2, 8 nm SiO_2 + 8 nm HfO_2 and 0.5 nm SiO_2 + 3 nm HfO_2.

SiO_2 to reduce the interface state density and 3 nm of the high K material HfO_2. Fig. 14 reveals an important conclusion that even for the transistor with the shortest gate-lengths of 5 nm, 7 nm and 10 nm, it is possible to turn the device on and off when the HfO_2 is added. All devices demonstrate good SS close to the theoretical minima of 60 mV/dec and the $I_{\rm on}/I_{\rm off}$ ratio is greater than 10^8. Hence, introducing the high-K material and decreasing the EOT could indeed improve significantly the device behaviour and allow the technology to be scaled down at least 5 nm gate-lengths.

V. Conclusion

In this paper we report an investigation of junctionless devices from the experimental and computational point of view. Based on our work we can conclude that the junctionless device with an 8 nm cross section and a 150 nm gate length demonstrate excellent transistor-like behaviour with a SS of 66 mV/dec and a 10^8 $I_{\rm on}/I_{\rm off}$ ratio. The gate length can be scaled down comfortably to 50 nm and the wire still retains properties of a good transistor. In order to scale the devices down to 10 nm at this particular cross-section of 8 nm, the only option is to introduce a high-K material as an oxide. Other possible options to improve the device performance is to either decrease the cross-section of the nanowire or to reduce the EOT by decreasing the physical thickness of the SiO_2 and the high-K oxide. Indeed, such experimental and computational work is under investigation. At present the variability and reliability issues in such ultra-scaled junctionless nanowire transistors has yet to be studied and this will be the topic of future investigations.

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