Negative Capacitance for Boosting Tunnel FET performance

Masaharu Kobayashi, *Member, IEEE*, Kyungmin Jang, Nozomu Ueyama, and Toshiro Hiramoto, *Member, IEEE*

***Abstract*—We have proposed and investigated a super steep subthreshold slope transistor by introducing negative capacitance of a ferroelectric HfO_2 gate insulator to a vertical tunnel FET for energy efficient computing. The channel structure and gate insulator are systematically designed to maximize the I_{on}/I_{off} ratio. The simulation study reveals that the electric field at the tunnel junction can be effectively enhanced by potential amplification due to the negative capacitance. The enhanced electric field increases the band-to-band tunneling rate and I_{on}/I_{off} ratio, which results in 10× higher energy efficiency than in tunnel FET.**

***Index Terms*—Energy-efficiency, ferroelectric, negative capacitance, steep slope transistor, tunnel FET.**

I. Introduction

APART from the need of high performance CMOS technology, new high-volume and large-variety of Internet-of-Things (IoT) applications demand low-cost and ultralow-power CMOS technology. IoT devices are expected to operate in the environment without power supply or battery exchange, and use energy-harvesters. In such case, the SoC chip in the IoT device operates at sub-1 μW power consumption. Fig. 1 shows the simple estimation of MCU power consumption [1]– [3]. At high switching frequency, dynamic switching power is dominated, while, at low switching frequency, static leakage power is dominated. Suppose IoT devices operate around MHz range, leakage current already dominates MCU power consumption at low switching frequency and must be suppressed to operate the chip at sub-1 μW and MHz operation.

In order to achieve ultralow power operation, there have been extensive studies on steep subthreshold slope transistors, such as tunnel FET (TFET) [4], [5] and negative capacitance FET (NCFET) [6], [7]. In general, the subthreshold slope (*SS*) of MOS-gate type device is expressed by

$$SS = \left(\frac{\partial \log_{10} I_{ds}}{\partial \psi_s}\right)^{-1} \cdot \left(\frac{\partial \psi_s}{\partial V_g}\right)^{-1}. \quad (1)$$

The first term is a transport term which represents how much current can flow by lowering the potential along the channel.

Manuscript received November 5, 2016; accepted January 16, 2017. Date of publication January 25, 2017; date of current version March 8, 2017. The review of this paper was arranged by Associate Editor Prof. D. Ielmini.

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Digital Object Identifier 10.1109/TNANO.2017.2658688

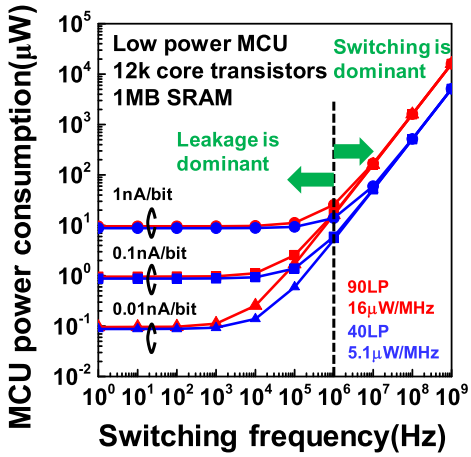

Fig. 1. Estimation of power consumption in MCU with 1 MB SRAM for two different technologies as function of leakage current per bit.

The second term is a voltage divider term which represents how efficiently the surface potential Ψ_s can bend at given gate voltage V_g. In classical MOSFETs, theoretically, the first term is limited by Boltzmann distribution tail in diffusion transport and the second term is limited by voltage divider in series connected capacitor, and thus, the physical limit of SS at room temperature is 60 mV/dec. To overcome this physical limit, TFET improves the first term by utilizing band-to-band tunneling and energy filtering between source and channel band edges. NCFET improves the second term by amplifying Ψ_s due to negative capacitance of ferroelectric gate insulator.

So far, each transistor has pros and cons but is independently studied. For example, tunnel FET suffers from low on-current and limited range of onset of steep subthreshold slope. Negative capacitance is mostly effective around/above threshold. These facts prevent the devices from being a practical solution. However, the combination of these devices' functionalities [8], [9] can provide a solution to realize super steep subthreshold slope transistor (Fig. 2).

In this paper, we propose and systematically investigate a novel hybrid device architecture of TFET and NCFET with ferroelectric HfO_2 gate insulator based on TCAD and analytical simulation. The channel structure and gate dielectric are systematically designed to optimize the I_{on}/I_{off} ratio. The energy efficiency of the relevant devices is benchmarked.

II. Device Structure and Experiments

The basic device structure in this work is a Si planar tunnel FET with a vertical tunnel junction [5], [10], where the source

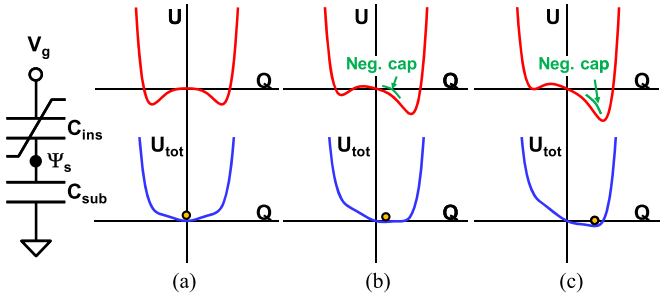

Fig. 2. Calculated free energy of ferroelectric capacitor (top) and total energy of series connection of ferroelectric and normal capacitor. (a) $V_g - V_{fb} = 0.0$ V, (b) $V_g - V_{fb} = 0.03$ V, (c) $V_g - V_{fb} = 0.05$ V.

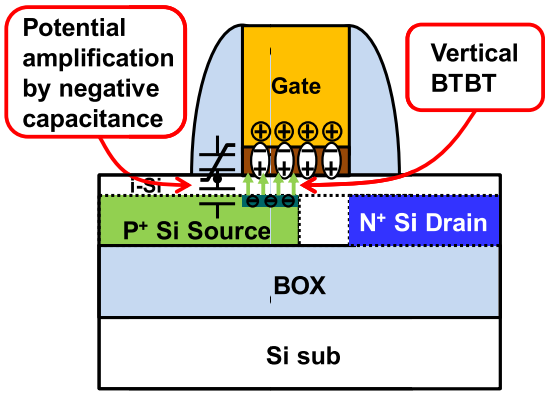

Fig. 3. Schematic of simulated NCTFET. In the simulation, thin interfacial layer and thin field plate layer are inserted for simulation purpose.

is overlapped by the gate and band-to-band tunneling occurs in vertical direction. Vertical TFETs have benefits in that the potential modulation at tunnel junction is more efficient than lateral TFETs and large tunnel current can be obtained through the overlapped area. Tunnel FET can be simulated by TCAD. A basic set of physics of tunneling is specified in the command file, such as dynamic non-local path band-to-band tunneling (BTBT) model with Kane's indirect tunneling model parameters [11]. TCAD is calibrated by fitting the simulated data to the experimental data [12].

Negative capacitance is available in series connection of a ferroelectric and normal capacitor [6]. Such a metal-ferroelectric-semiconductor (MFS) structure can have a stable state in total energy with negative curvature in Landau energy of the ferroelectric as gate bias is applied (Fig. 2). The relationship between polarization charge density and electric field in ferroelectric film are analytically described in Landau equation. Given polarization charge density, electric field across the ferroelectric can be numerically calculated.

Now by combining tunnel FET and NCFET, a hybrid device structure is proposed in Fig. 3. The channel structure is adopted from the vertical TFET, where PIN diode is formed on SOI substrate. A thin intrinsic Si layer is epitaxially grown on PIN diode. Then ferroelectric gate insulator and gate material are put on top of the intrinsic Si layer. We call this type of device as Negative Capacitance Tunnel FET (NCTFET).

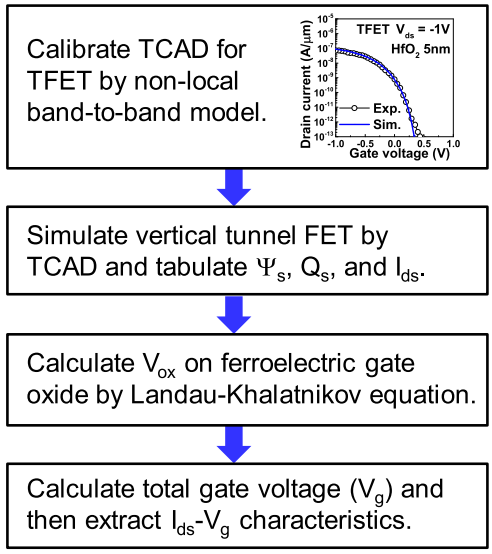

Fig. 4. Simulation flow of the proposed NCTFET with vertical tunneling. The inset shows the TFET calibration result which refers to the experimental data of [12].

The benefit of vertical TFET structure for NCTFET is to be able to obtain large gate-to-substrate capacitance so that ferroelectric gate capacitance can match to realize steep SS. Source and drain contacts are formed outside the gate spacer by etching back the intrinsic Si layer and putting contacts on p+ /n+ source/drain [10]. Contact resistance is not incorporated as source and drain are doped in sufficiently high level.

The simulation method is shown in the flow chart in Fig. 4. First a vertical TFET with standard MOS gate is simulated by TCAD. Potential profile, charge density and drain current are obtained. Next, Landau-Khalatnikov equation is solved to determine the electric field across the ferroelectric gate insulator corresponding to the charge density generated in the substrate. Please note that the dynamic term of Landau- Khalatnikov equation is not considered in this work. Although the finite response time of spontaneous polarization is an important factor when discussing device operation speed [14], the coefficient of the dynamic term of ferroelectric HfO_2 films has not been experimentally determined in detail yet. Therefore, we rather focus on static terms in Landau- Khalatnikov equation, suppose the finite response time can be fast enough for relatively slow application such as IoT device. The charge density is non-uniform across the substrate and it is therefore integrated across the substrate and divided by gate length for averaging. To validate the use of the uniform and single domain ferroelectric capacitor one-dimensional model for ferroelectric gate insulator, a very thin interfacial layer and field plate are inserted between ferroelectric and substrate [15] for simulation purpose. But this field plate can be also used to experimentally detect internal potential [16]. The field plate is the same material as the top electrode and the interfacial layer is high-k dielectric film which can suppress leakage current. Lastly, V_g is determined by Ψ_s and voltage across the gate insulator (V_{ox}).

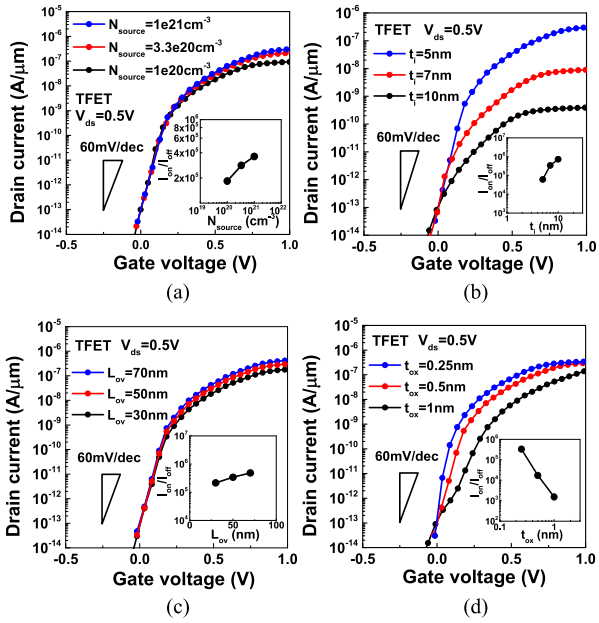

Fig. 5. Simulated $I_d - V_g$ characteristics of TFET varying (a) N_{source}, (b) t_i, (c) L_{ov}, and (d) t_{ox}. The inset shows the summary of dependence on each parameter. I_{on} and I_{off} are taken at $V_{gs} = 0.5$ V and $V_{gs} = 0$ V, respectively.

III. Results and Discussions

In this section, we first design the channel structure and then design ferroelectric gate insulator of NCTFET. Then we benchmark the energy efficiency of NCTFET with relevant devices.

A. Channel Structure Design

There are a number of device parameters to design channel structures. Here we focus on the most critical parameters such as source doping concentration (N_{source}), intrinsic layer thickness (t_i), oxide thickness (t_{ox}) and overlap length (L_{ov}), to design the channel structure with highest I_{on}/I_{off}. For simplicity, TFET is simulated by varying the device parameters above. Nominal parameter values are: $N_{source} = 1e21$ cm^{-3}, $t_i = 5$ nm, $L_{ov} = 50$ nm, $t_{ox} = 0.5$ nm. When one parameter is varied, the other parameters are nominal values. We assume to integrate NCTFET process to a mature CMOS process technology and fix the gate length at 100 nm. V_{th} is tuned by gate workfunction to target $I_{off} = 1e\text{-}13$ A/μm. Fig. 5 shows $I_d - V_g$ characteristics of vertical TFETs varying device parameters.

Fig. 5(a) shows the N_{source} dependence. N_{source} determines how steep tunnel junction to form at PIN diode. As N_{source} becomes high, the electric field at the tunnel junction becomes large, so that tunneling current at on-state is enhanced. For realistic process implementation, $N_{source} = 1e21$ cm^{-3} is chosen.

Fig. 5(b) shows the t_i dependence. The electric field from gate and gate dielectric is drawn from the overlapped source through the intrinsic Si layer. Therefore, thinner t_i induces larger electric field at the tunnel junction and shows higher tunneling current at on-state. $t_i = 5$ nm is chosen for realistic process implementation.

Fig. 5(c) shows the L_{ov} dependence. The overlap between the gate and the source is necessary to realize vertical band-to-band tunneling. As L_{ov} increases, tunneling current at on-state almost linearly increases. This is because vertical tunneling occurs through the area L_{ov} x W_g and tunneling current is proportional to L_{ov} at fixed $W_g = 1\,\mu$m. If L_{ov} becomes too close to gate length, however, source and drain will short. $L_{ov} = 50$ nm is chosen for moderate performance but to avoid the worst case of misalignment and process controllability.

Fig. 5(d) shows the t_{ox} dependence. Please note that the gate insulator in this subsection is a nominal dielectric and not ferroelectric. V_g is divided by the gate oxide and substrate including the tunnel junction. When t_{ox} becomes thin, larger voltage will drop at the substrate and higher electric field will be induced at the tunnel junction at given V_g. Therefore, as t_{ox} becomes small, tunneling current at on-state increases. In addition, just like standard MOSFET, SS is steeper at thinner t_{ox}. This indicates that strong gate control is effective to enhance band-to-band tunneling in vertical TFET. EOT = 0.5 nm is one of the thinnest EOT ever achieved on standard CMOS high-k/metal-gate technology [17]. Therefore, in the later subsection, reference TFET has t_{ox} = EOT = 0.5 nm as the best case, while NCTFET has t_{ox} = EOT = 0.5 nm interfacial layer with field plate on which ferroelectric gate insulator and top metal gate are formed. In this study, we look at how much gain we can get by adding ferroelectric stack on the thinnest EOT = 0.5 nm interfacial layer for NCTFET. This comparison will show us the benefit of ferroelectric stack in NCTFET, compared to TFET with just the thinnest EOT gate insulator.

B. Ferroelectric Gate Insulator Design

Based on the channel structure determined in the previous subsection, for ferroelectric gate insulator part, we determine the critical material parameters such as remanent polarization (P_r), coercive field (E_c) and thickness (t_{ins}) of a ferroelectric thin film. Both P_r and E_c values are tuned within the range which does not cause significant hysteretic behavior as discussed in [14]. As a reference design, we simply apply the nominal material parameters of $P_r = 10\,\mu$C/cm^2 and $E_c = 1$ MV/cm which are chosen from survey results of experiment data of ferroelectric HfO_2 thin film [14], [18]. Thickness of ferroelectric gate insulator is 6 nm which is close to the minimum thickness that shows ferroelectricity in HfO_2. Fig. 6(a) shows the charge density versus Ψ_s, V_{ox} and $V_g - V_{fb}$. Ψ_s is effectively amplified by negative V_{ox} due to negative capacitance effect. As a result, Fig. 6(b) shows the $I_d - V_g$ characteristics of this reference NCTFET and shows steeper SS than just TFET.

It should be noted that the SS becomes steep almost 4 decades of the current level even in deep subthreshold region, while NCFET mostly shows steep slope around and above threshold voltage. This can be explained by charge balance of polarization charge density of the ferroelectric gate insulator and the space charge density at the source junction of NCTFET. While polarization charge density can balance mostly with the inversion charge density in NCFET at high V_g to induce large negative oxide voltage, the space charge density at the overlapped source

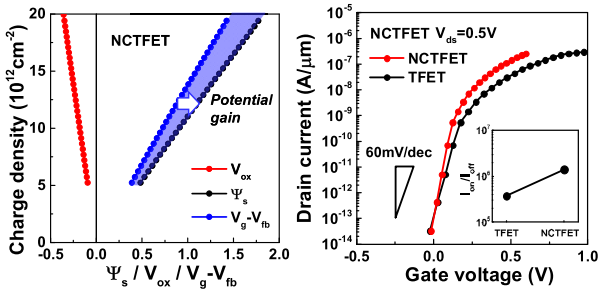

Fig. 6. (a) Charge density versus Ψ_s, V_{ox} and $V_g - V_{fb}$ for the reference NCTFET. (b) Simulated $I_d - V_g$ characteristics of the reference NCTFET. The inset shows the summary of dependence on each parameter. I_{on} and I_{off} are taken at $V_{gs} = 0.5$ V and $V_{gs} = 0$ V, respectively.

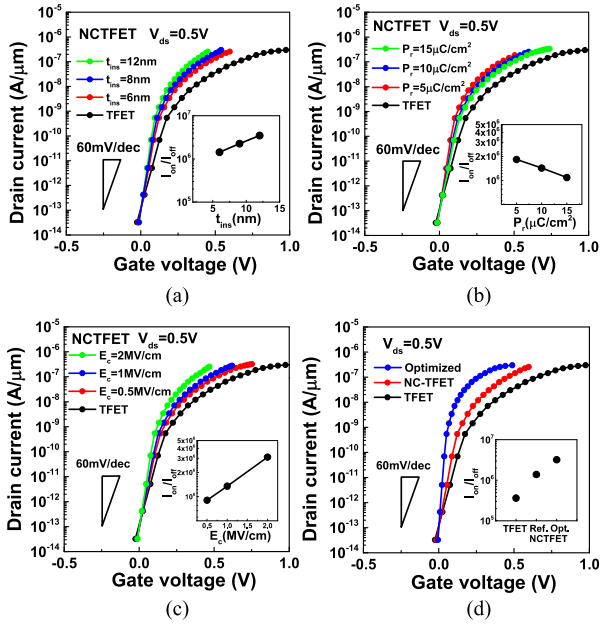

Fig. 7. Simulated $I_d - V_g$ characteristics of NCTFET varying (a) t_{ins}, (b) P_r, (c) E_c, and (d) optimizing the parameters. The inset shows the summary of dependence on each parameter. I_{on} and I_{off} are taken at $V_{gs} = 0.5$ V and $V_{gs} = 0$ V, respectively.

can respond to the polarization charge density at low V_g subthreshold region in NCTFET. This result is consistent with the ground-plane type NCFET device design [19]. Fig. 7 shows $I_d - V_g$ characteristics of NCTFET varying material parameters comparing to TFET.

Fig. 7(a) shows the t_{ins} dependence. Ferroelectric material has unique P-E characteristics and V_{ox} is determined by the product of the electric field in the ferroelectric insulator and t_{ins}. Thicker t_{ins} induces larger V_{ox} on ferroelectric gate insulator. Therefore Ψ_s is more amplified by thicker t_{ins} and NCTFET shows steeper slope.

Fig. 7(b) shows the P_r dependence at fixed E_c. When P_r becomes large, NC becomes large in P-E curve and negative V_{ox} available at given charge density becomes small. Therefore smaller P_r is preferable to access larger negative V_{ox} and thus obtain steeper slope.

TABLE I
KEY DEVICE PARAMETERS OF THE OPTIMIZED NCTFET

N_{source}	t_i	L_{ov}	t_{ox}	t_{ins}	P_r	E_c
1×10^{21}/cm^3	5 nm	50 nm	0.5 nm	6 nm	5 μC/cm^2	2 MV/cm

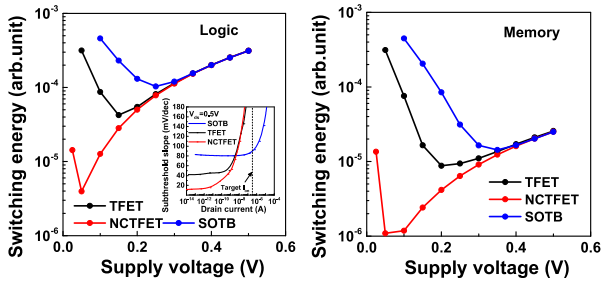

Fig. 8. Energy efficiency of optimized NCTFET, TFET and SOTB for (a) logic acitivty and (b) memory activity. The inset of (a) shows the SS of these three transistors as a function of drain current.

Fig. 7(c) shows the E_c dependence at fixed P_r. When E_c becomes large, NC becomes small in P-E curve and negative V_{ox} available at given charge density becomes large. Therefore larger E_c is preferable to access larger negative V_{ox} and thus obtain steeper slope.

In Fig. 7(b) and (c), we confirm that the strategy to obtain steeper slope by NC is consistent with the previous device design guideline of NCFET [14]. Now Fig. 7(d) shows $I_d - V_g$ characteristics of an optimized NCTFET as well as reference NCTFET and TFET. By choosing realistic material parameters of ferroelectric HfO_2 thin film; $P_r = 5\ \mu$C/cm^2 and $E_c = 2$ MV/cm, a super steep slope NCTFET was achieved with higher I_{on}/I_{off}.

To summarize this subsection, optimum device parameters are shown in Table I.

C. Benchmark of Energy Efficiency

In Fig. 7(d), the optimized NCTFET shows higher I_{on}/I_{off} ratio than reference NCTFET and TFET. Especially high I_{on}/I_{off} ratio is maintained even at supply voltage (V_{dd}) less than 0.5 V. This means that NCTFET can realize highly energy-efficient switching at ultralow V_{dd}.

Fig. 8(a) and (b) shows switching energy [20], which is referred as energy efficiency, of optimized NCTFET, TFET and conventional MOSFET that is Silicon-on-Thin-Box (SOTB) MOSFET for logic and memory activity. TCAD is calibrated for SOTB MOSFET using experimental data [21]. The switching energy is estimated by

$$E \propto V_{dd}^2 \left(\xi + \frac{I_{off}}{I_{on}} \right), \tag{2}$$

where ξ is active time ratio [16]. Standard ξ value is chosen 1/800 and 1/10000 for logic and memory activity, respectively. Drive currents of NCTFET, TFET and SOTB match at $V_{dd} = 0.5$ V for fair normalization and comparison. SS of these three devices is shown in the inset of Fig. 8(a) as a function of drain

current. For both logic and memory activity, it is demonstrated that NCTFET has lower energy minimum voltage and has a potential to significantly improve energy efficiency more than 10 times compared to TFET and SOTB at ultralow V_{dd} less than 0.2 V. This is an encouraging result that suggests NCTFET is a promising candidate for an ultralow power IoT technology.

Though we focus on Si TFET for benchmarking, it is known that compound semiconductor TFETs can outperform Si TFET [4]. NC effect is in principle additive performance booster to any type of channel material. Therefore, improvement of TFET performance by compound semiconductor can lead to further performance improvement of NCTFET as well.

IV. Summary

In this work, NCTFET was proposed as a hybrid device structure of vertical TFET and NCFET with ferroelectric HfO_2. Hybrid simulation method was also established to design TFET channel and ferroelectric gate insulator in combination. Based on the simulation, TFET channel structure and ferroelectric gate insulator are optimized to achieve the highest band-to-band tunneling and largest potential amplification, and thus maximum I_{on}/I_{off} ratio of NCTFET. It is demonstrated that NCTFET has a potential to achieve 10 times higher energy efficiency than TFET and conventional MOSFET. NCTFET is a promising candidate for IoT technology platform.

Acknowledgement

The authors appreciate the supports received from JST PRESTO and NEDO. The authors also acknowledge VDEC for TCAD support.

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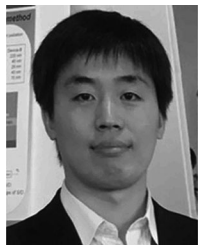

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