3-D Finite Element Monte Carlo Simulations of Scaled Si SOI FinFET With Different Cross Sections

Daniel Nagy, Muhammad A. Elmessary, Manuel Aldegunde, Raul Valin, Antonio Martinez, Jari Lindberg, Wulf G. Dettmer, Djordje Perić, Antonio J. García-Loureiro, and Karol Kalna

***Abstract*—Nanoscaled Si SOI FinFETs with gate lengths of 12.8 and 10.7 nm are simulated using 3-D finite element Monte Carlo (MC) simulations with 2-D Schrödinger-based quantum corrections. These nonplanar transistors are studied for two cross sections: rectangular-like and triangular-like, and for two channel orientations: ⟨100⟩ and ⟨110⟩. The 10.7-nm gate length rectangular-like FinFET is also simulated using the 3-D nonequilibrium Green's functions (NEGF) technique and the results are compared with MC simulations. The 12.8 and 10.7 nm gate length rectangular-like FinFETs give larger drive currents per perimeter by about 33–37% than the triangular-like shaped but are outperformed by the triangular-like ones when normalised by channel area. The devices with a ⟨100⟩ channel orientation deliver a larger drive current by about 11% more than their counterparts with a ⟨110⟩ channel when scaled to 12.8 nm and to 10.7 nm gate lengths. $I_D - V_G$ characteristics obtained from the 3-D NEGF simulations show a remarkable agreement with the MC results at low drain bias. At a high drain bias, the NEGF overestimates the on-current from about $V_G - V_T = 0.3$ V because the NEGF simulations do not include the scattering with interface roughness and ionized impurities.**

***Index Terms*—Cross-section shapes, FinFET, Monte Carlo simulations, nonequilibrium Green's functions (NEGF) simulations.**

I. Introduction

NONPLANAR multigate transistors like FinFETs [1] are the leading solutions for the sub-22 nm digital technology [2]. Further scaling of FinFETs requires a realistic assessment of device performance, which is strongly affected by the exact device geometry and architecture [3]. However, the 3-D geometry of all nonplanar transistors brings new challenges for physically based device modeling like ensemble Monte Carlo (MC)[4], since these nanoscale devices exhibit unique shapes created by fabrication processes [5]. These irregular geometries can be accurately described by the 3-D finite element (FE) method.

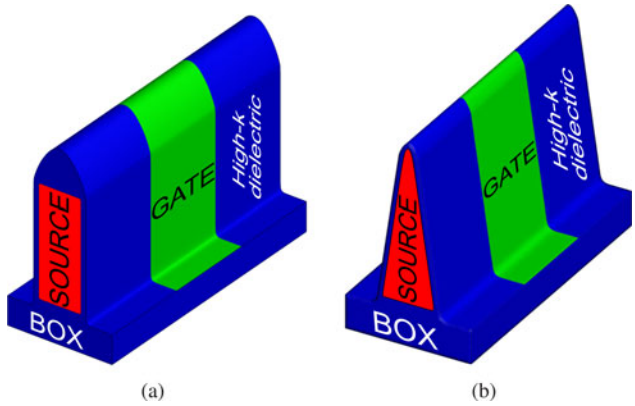

Fig. 1. Schematic of the 12.8/10.7 nm gate length. (a) Rectangular and (b) triangular shape n-channel SOI Si FinFET. Dimensions and parameters are summarized in Table I.

In this study, we report on the device performance of nanoscale n-channel Si SOI FinFETs scaled to gate lengths of 12.8 and 10.7 nm following the ITRS [6]. The investigation includes 1) two different shapes of the scaled transistors: rectangular-like [see Fig. 1(a)] and triangular-like [7] [see Fig. 1(b)] with rounded corners [8], and 2) two different channel orientations: ⟨100⟩ and ⟨110⟩. The devices are simulated using a novel 3-D FE MC toolbox with quantum corrections based on 2-D FE solutions of the Schrödinger equation [9] capable of an accurate prediction of the 3-D transistor performance. These simulations are accompanied with 3-D nonequilibrium Green's functions (NEGF) simulations [10], [11] which include dissipative processes (phonon scattering). The dissipative NEGF simulations are carried out for the rectangular cross section 10.7-nm gate length FinFET in order to study the effect of source-to-drain tunneling on its subthreshold characteristics and the on-set of on-current.

II. Monte Carlo Simulations With Schrödinger Equation-Based Quantum Corrections

The performance of nanoscale n-channel FinFETs is predicted using an in-house-developed 3-D FE self-consistent ensemble MC simulation toolbox described in details elsewhere [8], [9]. However, we briefly summarize core features of the

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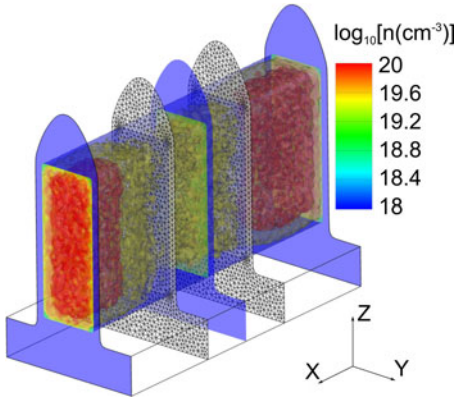

Fig. 2. Isosurface of the electron density from the 3-D MC at $V_G - V_T = 0.7$ V, $V_D = 0.7$ V and 2-D slices for the Schrödinger solver across the channel in the 10.7-nm gate length rectangular shape FinFET.

toolbox, especially those which are different to other 3-D MC simulation codes and relevant to the investigated devices. The simulation process starts with a solution of the 3-D self-consistent drift-diffusion (DD) transport model. The motivation for the initial DD presimulation is twofold: 1) accurate simulation of deep subthreshold and 2) obtaining an initial solution for the MC to speed up the simulation process. The FE MC simulation process then continues with transport process (free flights and scatterings), Poisson equation solution, and quantum corrections performed at every time step. The 3-D FE MC toolbox with FE density gradient (DG)-based quantum corrections [8] demonstrated an excellent agreement with experimental $I_D - V_G$ characteristics for the 25-nm gate length SOI FinFET [12], justifying its accuracy. The drawback of the DG is that it requires a calibration which can be impossible for complex transistor geometries. However, a new 3-D FE MC toolbox with Schrödinger-based quantum corrections [9] has no need for any parameter calibration [13]. A 3-D FE mesh of the device under investigation contains predefined 2-D planes perpendicular to the transport direction x, where the cross section is constrained to conform with a 2-D triangular mesh, as illustrated in Fig. 2. Those are used to extract a 2-D electrostatic potential, $V(y, z)$, from the 3-D electrostatic potential $V(\mathbf{r})$ where $\mathbf{r} \equiv \mathbf{r}(\mathbf{x}, \mathbf{y}, \mathbf{z})$. The 2-D potential is then used to solve a 2-D time-independent Schrödinger equation

$$-\frac{\hbar^2}{2}\nabla_\perp \cdot \left[(\mathbf{m}^*)^{-\mathbf{1}} \cdot \nabla_\perp \psi(\mathbf{y}, \mathbf{z})\right] + U(y, z)\psi(y, z) = E\psi(y, z) \quad (1)$$

where E is the energy, $(\mathbf{m}^*)^{-\mathbf{1}}$ is the inverse effective mass tensor, the subscript $\perp$ refers to the transverse coordinates y and z, $\psi(y, z)$ is the wave function penetrating into the surrounding oxide, and $U(y, z) = -[qV(y, z) + \chi(y, z)]$ is the potential energy with $\chi(y, z)$ being the electron affinity. The 2-D quantum density n_{q}, calculated from the eigenstates and energies of (1), is then interpolated onto the 3-D simulation domain to obtain the quantum correction potential as [9], [13]

$$V_{\mathrm{qc}}(r) = (k_B T/q) \log\left[n_{\mathrm{q}}(\mathbf{r})/n_{\mathrm{ien}}(\mathbf{r})\right] - V(\mathbf{r}) + \phi_n(\mathbf{r}) \quad (2)$$

TABLE I
DEVICE DIMENSIONS AND PARAMETERS: PHYSICAL GATE LENGTH (L_g), FINFET HEIGHT AND WIDTH, EQUIVALENT OXIDE THICKNESS (EOT), STANDARD DEVIATION FOR GAUSSIAN n-DOPING IN SOURCE/DRAIN (σ_x), CIRCUMFERENCE/PERIMETER OF THE SI n-CHANNEL UNDER THE GATE, AND AREA OF THE SI n-CHANNEL

Technology [nm]	Rectangular		Triangular	
	16	11	16	11
Lg [nm]	12.8	10.7	12.8	10.7
Height [nm]	18	15	21.21	17.67
Width [nm]	7	5.8	7	5.8
EOT [nm]	0.67	0.62	0.67	0.62
σ_x [nm]	4.13	3.45	4.13	3.45
Perimeter [nm]	43	35.8	43	35.8
Area [nm^2]	126	87	74	51

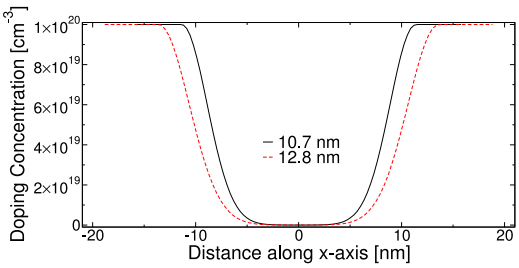

Fig. 3. Cross sections of doping profiles along the transport x-direction for the 12.8 and 10.7 nm gate length FinFETs.

where $n_{\mathrm{ien}}(\mathbf{r})$ is the effective intrinsic carrier concentration and $\phi_n(\mathbf{r})$ is the quasi-Fermi potential for electrons. The particles are moved in the quantum-corrected potential according to [13]

$$d\mathbf{k}/dt = (q/\hbar)\nabla\left[V(\mathbf{r}) + V_{\mathrm{qc}}(\mathbf{r})\right]. \quad (3)$$

Fig. 2 shows the isosurface of the density for the 10.7-nm device at $V_G - V_T = 0.7$ V and drain bias of 0.7 V. For the 2-D-Schrödinger solver, the rectangular-shaped devices had 21 slices distributed with more slices at the gate and the triangular shaped devices had 25 slices evenly distributed along the transport direction.

The MC engine in the 3-D FE simulation toolbox uses a nonparabolic anisotropic model [14], all Si-related electron scattering mechanisms are included: scattering with acoustic and nonpolar optical phonons (intravalley and intervalley) [4], [15], ionised impurity scattering using the third body exclusion by Ridley [16], [17], and interface roughness (IR) scattering using Ando's model [18]. More details on the 3-D FE MC device simulation tool can be found in [8], [9], [19].

The SOI FinFETs are scaled to gate lengths of 12.8 and 10.7 nm following the ITRS [6]. Table I lists the dimensions of the scaled FinFETs with both rectangular-like and triangular-like cross sections. Finally, Fig. 3 shows the Gaussian-like doping profile cut-lines along the transport direction of the two scaled transistors which were adapted from the 25-nm gate length Si SOI FinFET [8].

Source-to-drain tunneling might deteriorate subthreshold characteristics of multigate transistors with a gate length around 10 nm [20]. Therefore, we have employed a 3-D NEGF

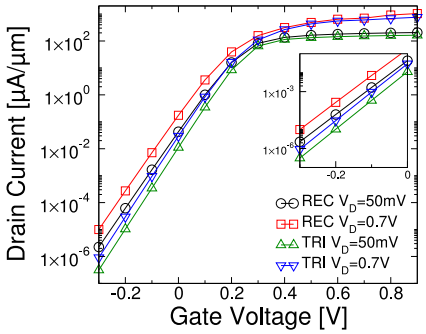

Fig. 4. Subthreshold $I_D - V_G$ characteristics for both shapes of the 12.8-nm gate length FinFETs. The inset magnifies the slope in a deep subthreshold region (3-D DD).

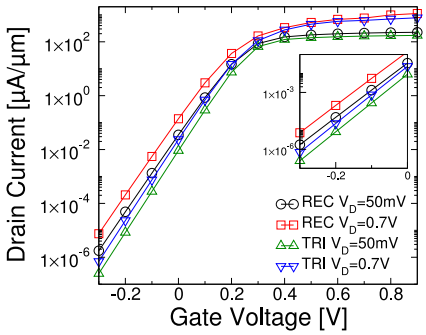

Fig. 5. Subthreshold $I_D - V_G$ characteristics for both shapes of the 10.7-nm gate length FinFETs. The inset magnifies the slope in a deep subthreshold region (3-D DD).

simulation toolbox [11] to investigate the *I–V* characteristics of the shortest gate length transistor, a 10.7-nm gate length FinFET, and compare them with the results from the MC simulations. This 3-D finite volume quantum transport simulator implements the mode-space approach of the NEGF formalism [21], [22] including dissipative energy processes like all relevant electron–phonon interactions. The 3-D nonlinear Poisson equation is solved self-consistently with the equations of the NEGF model as described in details elsewhere [11].

III. Scaled Si SOI FinFETs

The subthreshold regions of the two scaled FinFETs are initially investigated using a 3-D FE DD transport approach without quantum corrections. The initial DD simulations are employed to investigate electrostatic integrity of the nonplanar transistors because the ensemble MC is too noisy in the subthreshold region to accurately calculate very small currents. The FE DD simulations can predict well the subthreshold slopes (SS) of devices with various cross-section shapes but cannot take into account a channel orientation as well as any source-to-drain tunneling which will be investigated with a quantum transport technique, the NEGF method.

Figs. 4 and 5 show $I_D - V_G$ characteristics on logarithmic scale at low (0.05 V) and high (0.7 V) drain biases comparing rectangular-like and triangular-like cross sections for the 12.8 and the 10.7 nm gate length devices, respectively, obtained from

TABLE II
Threshold Voltage (V_T) and Subthreshold Slope (SS) for Drain Biases of 0.05 V (LOW) and 0.7 V (HIGH) From the DD {from the NEGF}, DIBL From DD and From MC, and Drive Currents ($I_{MC}^{\langle channel\ orientation\rangle}$) for Triangular and Rectangular FinFETs

Technology [nm]	Rectangular		Triangular	
	16	11	16	11
V_T [V]	0.2	0.2 {0.26}	0.2	0.2
SS_{LOW} [mV/dec]	71	70 {72}	66	66
SS_{HIGH} [mV/dec]	72	71 {78}	67	66
DIBL [mV/V]	58	56 {77}	34	34
$DIBL_{MC}^{\langle 100\rangle}$ [mV/V]	66	65	61	60
$DIBL_{MC}^{\langle 110\rangle}$ [mV/V]	71	65	64	64
$I_{MC}^{\langle 100\rangle}$ [μA/μm]	1853	1930	1393	1436
$I_{MC}^{\langle 110\rangle}$ [μA/μm]	1660	1749	1243	1290

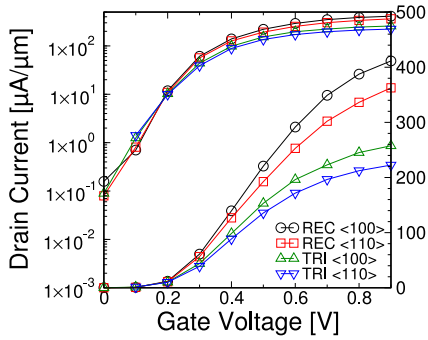

Fig. 6. $I_D - V_G$ characteristics at $V_D = 50$ mV with a gate length of 12.8 nm for the triangular (TRI) and rectangular (REC) shape FinFETs with $\langle 100\rangle$ and $\langle 110\rangle$ channel orientations (3-D MC).

these DD simulations. The inset in both figures magnifies the deep subthreshold region. The SS values are listed in Table II. The SS values for the rectangular-like devices are about 70–72 mV/dec and, for the triangular-like ones, the SS is nearly ideal, ~66 mV/dec, for both gate lengths. The better SS in the triangular-like transistors is due to the accumulation of carriers at the top of the device channel where the gate has a better control over the charge. Note that the differences between high and low drain bias for both cross sections are negligible. In addition, Table II compares the threshold voltage, the DIBL from 3-D DD, 3-D NEGF [11] and 3-D FE ensemble MC simulations and lists the drive currents from the 3-D MC for scaled triangular and rectangular devices with two channel orientations.

The 3-D FE MC with 2-D Schrödinger-based quantum corrections was employed to obtain the current in the operational region. Figs. 6 and 7 show the $I_D - V_G$ characteristics on logarithmic and linear scales at a low drain bias of 0.05 V for the 12.8 and 10.7 nm gate lengths, respectively. The figures also compare the different cross sections with $\langle 100\rangle$ and $\langle 110\rangle$ channel orientations. The drain current is normalized to the gate perimeter (see Table I). Note that the value of a very small current obtained from monitoring in MC simulations at $V_G = 0$ V becomes visibly affected by statistical errors inherent to the MC technique [23]. In the case of $\langle 100\rangle$ channel orientation, the drain current is always larger compared to the $\langle 110\rangle$ orientation

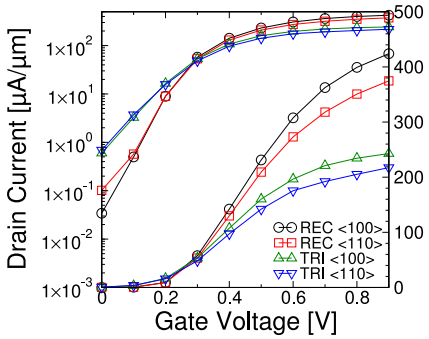

Fig. 7. $I_D - V_G$ characteristics at $V_D = 50$ mV with a gate length of 10.7 nm for the triangular (TRI) and rectangular (REC) shape FinFETs with $\langle 100 \rangle$ and $\langle 110 \rangle$ channel orientations (3-D MC).

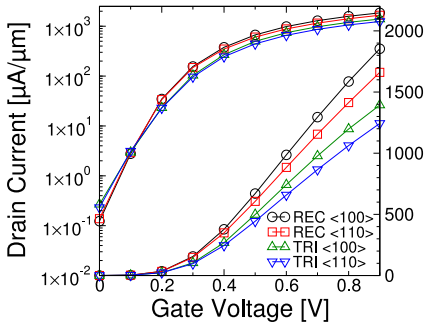

Fig. 8. $I_D - V_G$ characteristics at $V_D = 0.7$ V with gate length 12.8 nm for the triangular (TRI) and rectangular (REC) shape FinFETs with $\langle 100 \rangle$ and $\langle 110 \rangle$ channel orientations (3-D MC).

for both gate lengths and cross sections as expected due to a higher mobility of electrons in the $\langle 100 \rangle$ crystallographic orientation. At a gate voltage overdrive of 0.7 V, the drain current is $\sim 14\%$ larger in the $\langle 100 \rangle$ channel device than in that with the $\langle 110 \rangle$ channel orientation. The scaling from a gate length of 12.8 to 10.7 nm will increase the drive current about 3% for the rectangular and 1% for the triangular cross sections. The 12.8 and the 10.7 nm gate length rectangular-like devices with both channel orientations have 61% and 65% more drain current than the triangular-like cross-section devices with the respective gate lengths. The subthreshold region simulations using the 3-D FE MC with quantum corrections also suggest that the different quantum confinement could lead to a deterioration of the subthreshold slope with the scaling of the transistors.

The $I_D - V_G$ characteristics at a high drain bias of 0.7 V for the 12.8 and 10.7 nm gate length devices are shown in Figs. 8 and 9, respectively, again for both orientations and both cross sections. The difference between the drain current for $\langle 100 \rangle$ and $\langle 110 \rangle$ channel orientations are slightly reduced (10%) compared to the difference at the low drain bias. The difference for the drive currents between the 12.8 and 10.7 nm device is increased to 5% and 2% for the rectangular and triangular cross-sections, respectively, when compared to low drain bias. The rectangular-like cross-section devices have a 33–37% more current (normalized per perimeter) than the triangular-like ones for both scaled gate lengths of 12.8 and 10.7 nm despite the

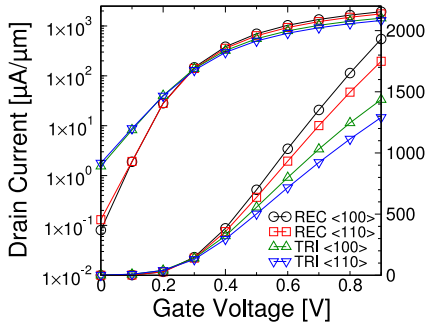

Fig. 9. $I_D - V_G$ characteristics at $V_D = 0.7$ V with gate length 10.7 nm for the triangular (TRI) and rectangular (REC) shape FinFETs with $\langle 100 \rangle$ and $\langle 110 \rangle$ channel orientations (3-D MC).

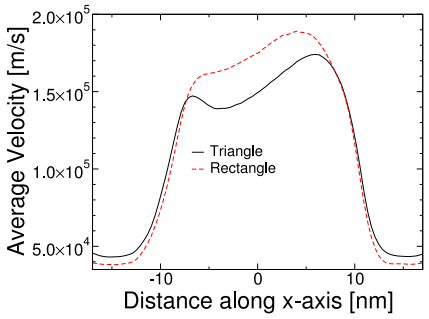

Fig. 10. Average electron velocity along the $\langle 100 \rangle$ channel at $V_G - V_T = 0.7$ V, $V_D = 0.7$ V for the 12.8-nm gate length rectangular-like and triangular-like FinFETs (3-D MC). The zero is set in the middle of the gate.

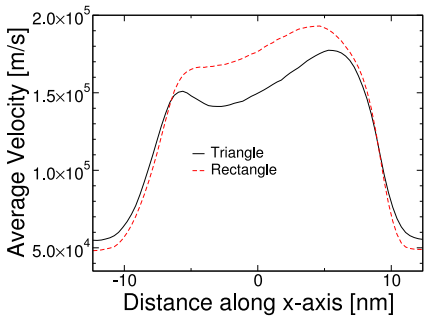

Fig. 11. Average electron velocity along the $\langle 100 \rangle$ channel at $V_G - V_T = 0.7$ V, $V_D = 0.7$ V for the 10.7-nm gate length rectangular-like and triangular-like FinFETs (3-D MC). The zero is again set in the middle of the gate.

devices having the same perimeter. The larger drain current is due to a larger area of the rectangular-like cross-section channels compared to the triangular-like cross-sections which can be understood from Figs. 12 and 13 showing current normalised per area and discussed later.

Figs. 10 and 11 compare the average electron velocity along the $\langle 100 \rangle$ channel of the 12.8 and 10.7 nm gate length FinFETs, respectively. The electron velocity in the triangular-like cross-section transistor, in the region controlled by the gate (the effective channel), is consistently lower due to an enhanced IR and phonon scattering (despite a better confinement indicated by a higher velocity in the source/drain regions) when compared to

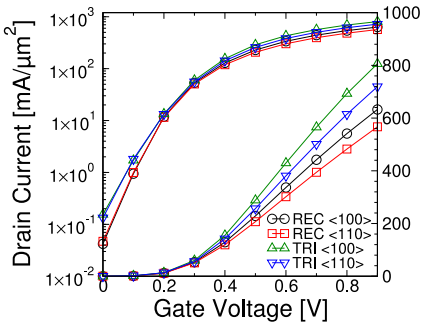

Fig. 12. $I_D - V_G$ at $V_D = 0.7$ V using a normalised-to-area current for the triangular-like and rectangular-like 12.8-nm FinFETs with $\langle 100 \rangle$ and $\langle 110 \rangle$ channel orientations.

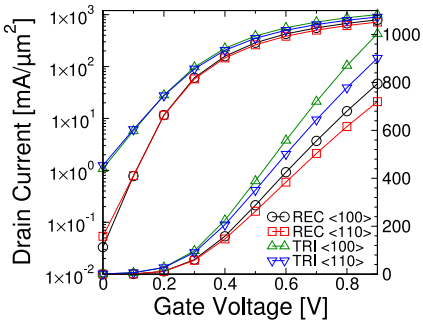

Fig. 13. $I_D - V_G$ at $V_D = 0.7$ V using a normalised-to-area current for the triangular-like and rectangular-like 10.7-nm FinFETs with $\langle 100 \rangle$ and $\langle 110 \rangle$ channel orientations.

the rectangular-like cross-section device. The enhanced IR and phonon scattering redistribute mainly the electron momentum in the transport direction resulting in the decline of the velocity at the beginning of the gate. The velocity starts to increase again as electrons are accelerated by a large electric fringing field at the end of the gate and, finally, declines at the heavily doped drain due to a strong ionised impurity scattering.

Figs. 12 and 13 show the $I_D - V_G$ characteristics normalized for the cross-section area (see Table I). When the drain current is normalised by the area of the cross section, the nonplanar triangular-like cross-section transistor delivers a larger on-current than the rectangular-like one. This opposite trend, when compared to the current normalisation per perimeter, occurs because the area difference of the two cross sections is larger than the effects of the decline in average electron velocity and the increase in electron sheet density. The average electron density along the channel is larger for the triangular-shaped devices (see Figs. 14 and 15), so that the sheet density does not increase proportionally to the change in cross-section area. The rectangular-like transistor has 1.7 times larger area than the triangular-like one for both gate lengths and gives up to a 24% and 27% larger on-current for the 12.8 and the 10.7 nm gate lengths, respectively, for both channel orientations at high drain bias. Finally, the 10.7 nm gate length devices have, in general, a 27% and 23% more drain current than the 12.8-nm gate length for the rectangular-like and triangular-like ones, respectively, justifying the scaling.

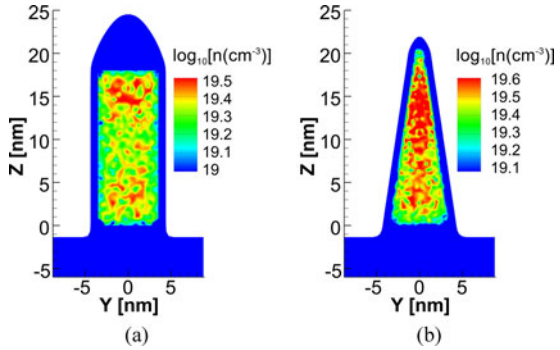

Fig. 14. Electron density cross section in the middle of the gate of the (a) rectangular-like and (b) triangular-like, $\langle 100 \rangle$ channel, 12.8-nm FinFET at $V_G - V_T = 0.7$ V, $V_D = 0.7$ V (3-D MC).

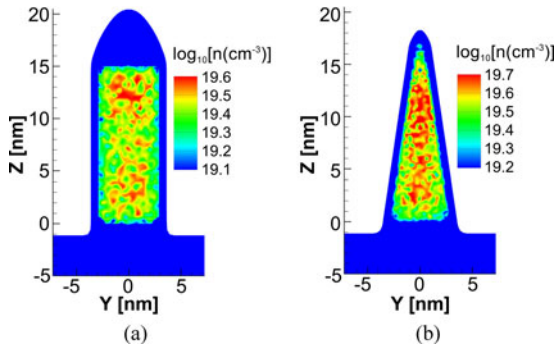

Fig. 15. Electron density cross section in the middle of the gate of the (a) rectangular-like and (b) triangular-like, $\langle 100 \rangle$ channel, 10.7-nm FinFET at $V_G - V_T = 0.7$ V, $V_D = 0.7$ V (3-D MC).

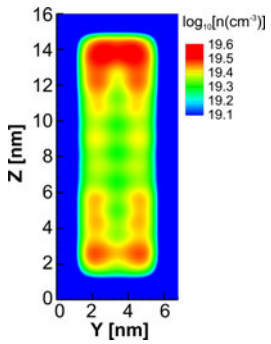

Fig. 16. Electron density cross section in the middle of the gate in 10.7-nm gate length, the rectangular FinFET at $V_G - V_T = 0.7$ V, $V_D = 0.7$ V (3-D NEGF).

Figs. 14 and 15 show the average electron density cross sections in the middle of the gate ($x = 0$ nm) for both cross sections of the 12.8 and 10.7 nm devices with the $\langle 100 \rangle$ channel, respectively, at $V_G - V_T = 0.7$ V and $V_D = 0.7$ V. Note here that the scale for the different shapes and devices are different in order to show the contrast between high and low areas of density. In the rectangular device, the electron density is distributed mostly at the top and bottom [see Figs. 14(a) and 15(a)] as also confirmed by the density distribution from the NEGF simulations in Fig. 16. A more scattered average density is observed from

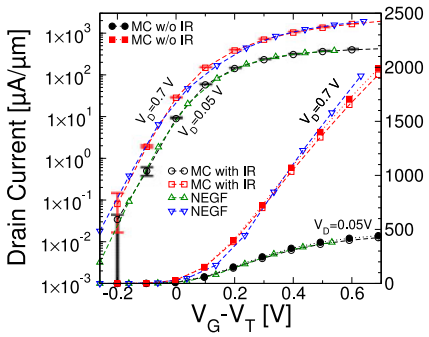

Fig. 17. I_D–$(V_G - V_T)$ at $V_D = 0.7$ V and $V_D = 50$ mV for the 10.7-nm gate length rectangular-like FinFETs with a $\langle 100 \rangle$ channel orientation comparing the MC and NEGF simulations. The MC simulations are shown without the IR (MC w/o IR) and with IR (MC with IR). Error bar included for the 3-D MC.

the 3-D MC because it is a particle-based simulation while the results from the 3-D NEGF are smoother since it is a wave-type quantum transport simulation technique. The density in the triangular-like device [see Figs. 14(a) and 15(b)] is larger and is distributed toward the narrow top explaining a larger on-current in Figs. 12 and 13. For the rectangular-like devices [see Figs. 14(a) and 15(a)], the density is slightly larger at the top due to the effect of the gate. Also, note that the thickness of the dielectric at the top of the triangular-like cross-section devices are smaller which helps to maintain a higher electron density there.

Finally, Fig. 17 compares the I_D–$(V_G - V_T)$ characteristics at 0.05 and 0.7 V drain biases normalized per cross-section perimeter, on both logarithmic and linear scales, obtained from the 3-D NEGF and 3-D MC simulations for the 10.7-nm gate length FinFET with a channel orientation of $\langle 100 \rangle$. The figure also contains error bars showing a statistical error from MC simulations in the deep subthreshold region. The error is relatively large at a gate bias of -0.2 V because of a very small current in the subthreshold region, but reduces dramatically at larger gate biases when the drain current increases at and above threshold. Note the 60 mV shift in the V_T between the MC and the NEGF simulations. The shift is because the MC simulation uses an approximation of the density of states (DoS), which is 3-D with nonparabolic dispersion law and a shift in the conduction band energy given by the quantum corrections, whereas the NEGF simulation has a 1-D-like DoS using a parabolic dispersion approximation which is self-consistently calculated including the effects of the scattering in the broadening of the energy levels [10]. The agreement between the two types of simulations is remarkably close in the subthreshold region. At the drain current on-set (just above the threshold), the agreement between the currents is still exceptionally good. For the high drain bias at $V_G - V_T = 0.3$ V the NEGF results start to overestimate the MC. The higher current in the NEGF is caused by the fact that these quantum transport simulations do not include the IR or ionized impurity scatterings [10]. The relevance of the surface roughness scattering on realistic *I–V* characteristics of 10-nm gate length FinFETs using the NEGF formalism has also been pointed out in [24]. The difference in the SS between MC and NEGF simulations is negligible and can be explained by a very small effect of the source-to-drain tunneling that is expected in devices with gate lengths of around 10 nm [25], [26]. Note the difference in the DIBL between the results from the NEGF and the MC in Table II where the NEGF predicts a larger DIBL by about 10 mV/V because it models accurately multisubband transport processes. Part of these multisubband processes could be taken into account with the multisubband ensemble MC technique [26], [27], but for a substantial price of computational burden when applied to the studied 12.8 and 10.7 nm gate length transistors. When scaled further to transistors with sub-10-nm gate lengths and sub-5-nm cross sections, the multisubband MC might achieve a better agreement with the NEGF technique. However, the agreement will be always limited because the source-to-drain tunneling starts to play a role in the total current not only in the subthreshold but also in the on-current region [20]. Furthermore, as the cross section is reduced, the difference in 1-D-like DoS between the multisubband MC, using a Fermi golden rule-based scattering, and the NEGF, using self-energies, will increase.

IV. Conclusion

We have successfully simulated rectangular-like and triangular-like shaped cross-section FinFETs scaled to gate lengths of 12.8 and 10.7 nm using a 3-D FE MC with quantum corrections based on solutions of the 2-D Schrödinger equation. The $I_D - V_G$ characteristics normalized to the perimeter showed that at low drain bias the on-current is higher for the rectangular shaped device by 61% and 65% for the 12.8 and 10.7 nm devices, respectively. For high drain bias, these differences are reduced to a $33 - 37\%$ higher on-current of the rectangular shaped FinFETs for both gate lengths. However, using normalization to the cross-sectional area shows that the triangle has higher on-current by 23–27% for both devices at high drain bias since the rectangular cross sections are 1.7 times larger than the triangular cross sections and the increase in sheet density and electron velocity is not enough to compensate this difference. The density for the rectangle spreads out more evenly while in case of the triangle it concentrates at the top due to the thinner silicon body and oxide thickness and therefore better control from the gate.

The NEGF simulations of the rectangular-shaped 10.7-nm gate FinFET show a very small deterioration of the SS with respect to classical DD simulations at $V_D = 0.05$ V and slightly larger SS for $V_D = 0.7$ V, indicating an increasing source-drain tunneling for higher drain bias. DD simulations show a better SS for the triangular cross-section FinFET and a negligible degradation with the scaling from 12.8 to 10.7 nm gate lengths. Finally, MC simulations show that during the scaling there is an increase of the perimeter-normalized drive current up to 5% when the devices are scaled from 12.8 to 10.7 nm. While the scaled SOI FinFETs deliver a small increase in the performance when assessed by the perimeter-normalized drive current, the performance increases by about 25% when the drive currents are evaluated using the normalization by the area of channel cross section.

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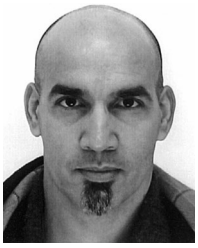

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