Comments and Corrections

Corrections to "Low-Cost Packaging of 300 GHz Integrated Circuits With an On-Chip Patch Antenna"

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In [1], an incorrect version of Table II was published. The correct version is presented here.

TABLE II
SIMULATED AND MEASURED (WITH AND WITHOUT PACKAGING) PERFORMANCE OF 300 GHz SIGNAL GENERATORS

Process Technology	65-nm CMOS					
Harmonic	2					
	Simulation				Measurements	
Encapsulation Material	None		QFN (ε_r=3.55)[b]		None	QFN
			Loss Tangent			
			0.01	0.02		
f_0 (GHz)	300	276	274	274	276	274
Pwr. Delivered to Ant. (dBm)	−13.2	−18.5	−16.4	−16.5		
Radiation Efficiency (%)	35	25	40	34		
Peak Gain at $\phi = 0°$(dB)	2.1	0	3.2	2.4		
[a] *EIRP* (dBm) (With bonding wires)	−11.1	−18.5	−13.2	−14.1	−18.9	−12.8
P_{DC} (mW)	24	24	24	24	26	26.3

[a]Effective isotropic radiated power.
[b]Simulated results with a 400 μm thick material with $\varepsilon_r = 3.55$ and loss tangents of 0.01 and 0.02 with bonding wires.

REFERENCE

[1] H. S. Bakshi *et al.*, "Low-cost packaging of 300 GHz integrated circuits with an on-chip patch antenna," *IEEE Antennas Wireless Propag. Lett.,* vol. 18, no. 11, pp. 2444–2448, Nov. 2019.

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