A Compact Ka-Band Active Integrated Antenna With a GaAs Amplifier in a Ceramic Package

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***Abstract*—This letter presents the design of a Ka-band active integrated antenna in package (AIAiP). A monolithic microwave integrated circuit amplifier based on the GaAs process and a compact patch antenna based on the printed circuit board process are implemented, respectively. Then, the amplifier and antenna are assembled together in a specified package using the wire-bond process. Thus, compared to the traditional solutions, the transmission loss and the size of the proposed AIAiP are significantly reduced. Furthermore, the influence of the bonding wire and the package is taken into account in the design of the amplifier and the antenna, respectively. A good agreement between the simulation and measurement results can be observed. The proposed AIAiP occupies a compact size of 7×7 mm^2. Meanwhile, it achieves -10-dB impedance bandwidth from 33.4 to 37.2 GHz and a peak gain of 18.9 dBi at 35 GHz. Additionally, the impact of the package size on the antenna performance has been demonstrated for future AIA designers.**

***Index Terms*—Active integrated antenna (AIA), antenna in package, GaAs amplifier.**

I. Introduction

ACTIVE integrated antenna (AIA) refers to the antenna integrated with one or more active solid-state devices. The AIA has received considerable interest due to its advantages in low loss and compact size, and is much more suitable for the phased-array antenna systems [1], [2]. Several kinds of AIAs have been investigated and reported. In [3] and [4], antenna is integrated with an amplifier on a single chip. However, this on-chip AIA is difficult to achieve high gain due to the process limitation. To improve the antenna gain, an additional off-chip reflector [3] and an additional off-chip lens [4] are introduced at the cost of increasing the size of the AIA. In [5], a Ka-band patch antenna array is integrated with packaged monolithic microwave integrated circuit (MMIC) phase shifters as an AIA using the low-temperature cofired ceramic (LTCC) technology. While in [6], a low noise amplifier (LNA) is also packaged with antenna arrays using the LTCC process, and a peak gain of 35 dBi is obtained by this AIA. Compared to the LTCC technology, the printed circuit board (PCB) process has an advantage of cost. As reported in [7], a packaged W-band LNA is integrated with a Yagi–Uda antenna based on the PCB technology and a 21.2-dBi peak gain is observed at 93 GHz.

However, these AIAs are entirely exposed to the air, which may seriously degrade their reliability and stability in harsh environments, especially when a bare die is used to form the AIA. Additional protective structures or protective materials can be used to solve this problem. However, these structures or materials could seriously degrade the performance of the antenna if their influences are not taken into account in the antenna design.

Actually, in recent years, the system-in-package (SiP) technology has been proposed to achieve a compact, integrated, and reliable system. Using this technology, a transceiver chip can be integrated with an antenna in a sealed package [8]. However, most of the reported SiP designs focus on the V-band or above the V-band, due to the limitation of antenna size. As we know, Ka-band is widely used in satellite communications and the military radar and communication systems. However, few of the AIAs in Ka-band are designed based on the concept of package. This limits the miniaturization potential of the Ka-band systems.

In this letter, a Ka-band packaged AIA is presented. To achieve a compact and reliable AIA, the proposed AIA is assembled in a sealed ceramic quad flat no-lead (QFN) package. The package influence is taken into account in the design of the antenna. The ceramic QFN package is applied in this work because it not only has better sealing characteristics than the plastic QFN package, but also has better heat dissipation performance than the embedded wafer-level ball grid array package. Two patch antennas are designed for comparison in the limited space with the specified package. Simulated results show that the half-wave patch antenna on the high dielectric constant substrate has a higher gain compared to the quarter-wave patch antenna on the low dielectric constant substrate. Therefore, only the former antenna is fabricated and tested in this work. Additionally, a Ka-band amplifier is designed and fabricated using

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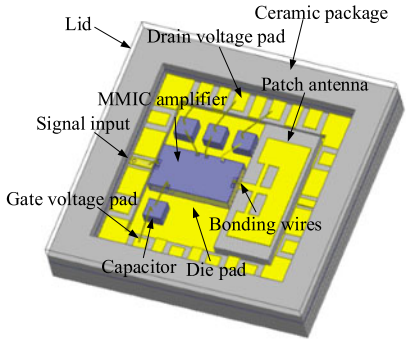

Fig. 1. Structure of the proposed AIA in package.

the GaAs process. Then, it is integrated with the antenna in the package using the wire-bond process. To achieve the impedance matching between the chip and the antenna, the influence of the bonding wire has been taken into account in the design of amplifier. Meanwhile, this letter investigates the impact of the package size on the performance of the antenna. It is useful to guide the AIAiP and SiP design in the future work. As will be shown, the measured −10-dB bandwidth of the amplifier and the AIAiP is 4.1 GHz (from 33.0 to 37.1 GHz) and 3.8 GHz (from 33.4 to 37.2 GHz), respectively, while the measured peak gain of them is 13.6 and 18.9 dBi, correspondingly. The proposed AIAiP is a promising solution to build a miniaturized system for the Ka-band communication and radar applications.

II. AIA Design

The proposed AIA is composed of an amplifier chip and a microstrip patch antenna and is assembled in a ceramic package based on wire-bond technology, as Fig. 1 illustrated. The amplifier chip is implemented by the standard 0.15-μm GaAs pseudomorphic high electron mobility transistor process provided by WIN Foundry. A microstrip antenna is adopted in this design due to its small profile, low cost, and easy fabrication. In addition, the ceramic package is provided by the KYOCERA Corporation with a size of $7 \times 7 \times 1.24$ mm^3. The ceramic material of the package is Kyocera A473, with the dielectric properties of $\varepsilon_r = 8.5$ and $\tan\sigma = 0.0021$.

A. Amplifier Design

The schematic diagram of the implemented MMIC amplifier is shown in Fig. 2. It is seen that the common source configuration is used in this design to obtain the best tradeoff between gain and output power, while three stages are adopted to achieve the desired gain [9], [10]. To reduce the power consumption, the transistor width of both the first and the second stage is selected to be 4×50 μm. Meanwhile, to achieve a high output power, the final stage contains two paralleled transistors with the width of 6×50 μm. Additionally, the influence of the bonding wire must be taken into account in the design of the amplifier because the amplifier is connected with the antenna and the package pad using wire-bonds in this AIAiP. The simulated *S*-parameter of a typical bonding wire (diameter is 25 μm, length is 400 μm) is first extracted and then added into the simulation model of the amplifier, as Fig. 2(a) illustrated. Therefore, the bonding wire is treated as a part of the matching network to achieve a good impedance matching for the amplifier. The impedances of the amplifier at 35 GHz with and without a bonding wire are

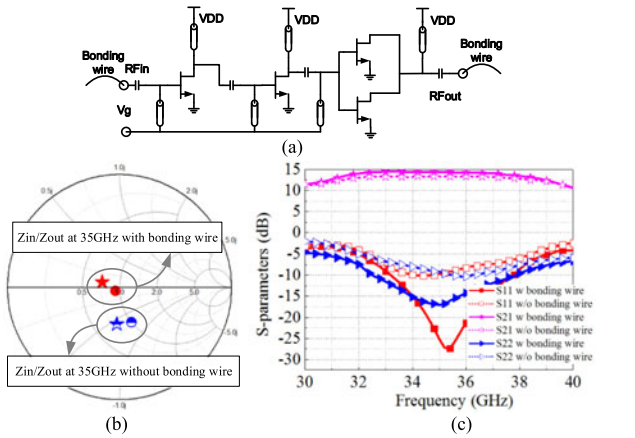

Fig. 2. (a) Schematic diagram of the MMIC amplifier used in the AIAiP. (b) Impedances of the amplifier with and without a bonding wire at 35 GHz. (c) *S*-parameters of the amplifier with and without a bonding wire.

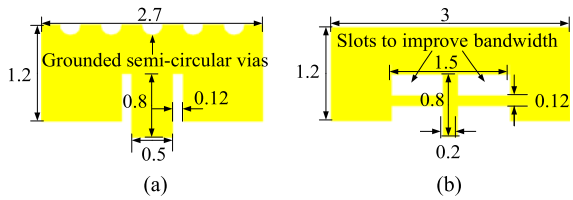

Fig. 3. Two kinds of patch antenna are simulated for comparison (unit: mm). However, only the antenna with a higher gain and a lower cost is fabricated and measured in this work. (a) Quarter-wave patch antenna with a low-permittivity substrate. (b) Half-wave patch antenna with a high-permittivity substrate (two slots are designed to improve the antenna bandwidth).

presented in Fig. 2(b). It shows that the amplifier input/output impedances change from 49.3 – j34.5 Ω/38.65 – j28.2 Ω to 46.3 – j2.7 Ω/36.5 – j3.7 Ω by adding the bonding wire. In addition, a peak gain of 14.5 dBi can be obtained by the amplifier with the bonding wire, which is about 1 dB higher than that without a bonding wire, as shown in Fig. 3(c).

B. Antenna Design

For the AIA packaged in a ceramic package, the size of the antenna needs to be designed to meet the requirements of this application. As shown in Fig. 1, the cavity in the package is $4 \times 4 \times 0.74$ mm^3 for amplifier and antenna assembling. The amplifier IC has occupied the size of 1.2×2.2 mm^2. Thus, the length of the antenna should be limited less than 1.5 mm (an installation margin of 0.3 mm should be required). Two types of patch antenna are simulated to meet this size requirement. As Fig. 3 depicted, one is a quarter-wave patch antenna with semicircular grounded vias at the edge of the antenna, on a low-permittivity substrate Ro4350B ($\varepsilon_r = 3.66$, $\tan\sigma = 0.0037$, $h =$ 0.338 mm). Another one is a half-wave patch antenna on a high-permittivity substrate RT6010LM ($\varepsilon_r = 10.2$, $\tan\sigma = 0.0023$, $h = 0.254$ mm). Two slots are designed in this antenna to increase the antenna capacitance, so as to improve the impedance matching of the antenna and increase the antenna bandwidth. The optimized size parameters of these two antennas are also shown in Fig. 3. Simulation results of reflection coefficient and gain are presented and compared between these two antennas, as Fig. 4 illustrated. It is seen that the −10-dB bandwidth of the half-wave patch antenna is 2% less than that of the quarter-wave patch antenna, but the maximum gain is 2.1 dB higher than the

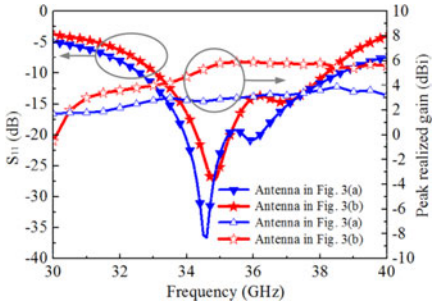

Fig. 4. Simulated reflection coefficient and peak realized gain of these two antennas.

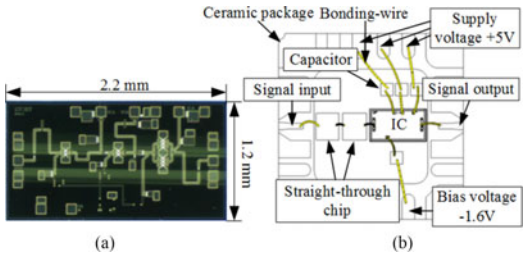

Fig. 5. Die photograph and the measurement setup of the designed GaAs amplifier. (a) Die photograph with the size of 1.2×2.2 mm^2. (b) Amplifier is measured in the package with two straight-through chips.

other. Moreover, it should be noted that the cost of making such semicircular grounded vias is relatively high. Hence, in this work, only the half-wave patch antenna presented in Fig. 3(b) is manufactured for a higher gain and a lower cost.

It should be noted that all of the simulation results are based on the model presented in Fig. 1. Accordingly, the influences of the MMIC and the package on the antenna performance have been taken into account in the antenna simulation.

III. Measurement

Fig. 5(a) illustrates the chip photograph of designed GaAs amplifier. For the first step, this MMIC amplifier is tested in the ceramic package before assembled with the antenna. A wire-bond process is used to realize the chip-to-package connection, as shown in Fig. 5(b). The bias voltage and the supply voltage of the amplifier are -1.6 and $+5$ V respectively. It should be mentioned that an additional straight-through chip is needed to fix and connect in series with the amplifier in the package. Thus, the length of the bonding wire between the amplifier pad and package pad can be limited to around 400 μm, as assumed in the matching design of the amplifier. Then, the *S*-parameters of this packaged amplifier are tested using an Agilent vector network analyzer (VNA) with short–open–load–through calibration. The measured results are shown in the letter. It is seen that the designed amplifier achieves good input and output matching in the package. The measured -10-dB bandwidth of the amplifier is from 33.0 to 37.1 GHz, which is in good agreement with the simulation results. Meanwhile, the measured gain is changed from 12.3 to 13.6 dB in the whole operating bandwidth. A deviation of about 1.1 dB is observed when compared to the simulation results. This is due to the loss of the PCB-to-package transition, the loss of the additional straight-through chip, and the GaAs process deviation.

For the second step, the amplifier chip and the patch antenna are assembled together in the ceramic package, which

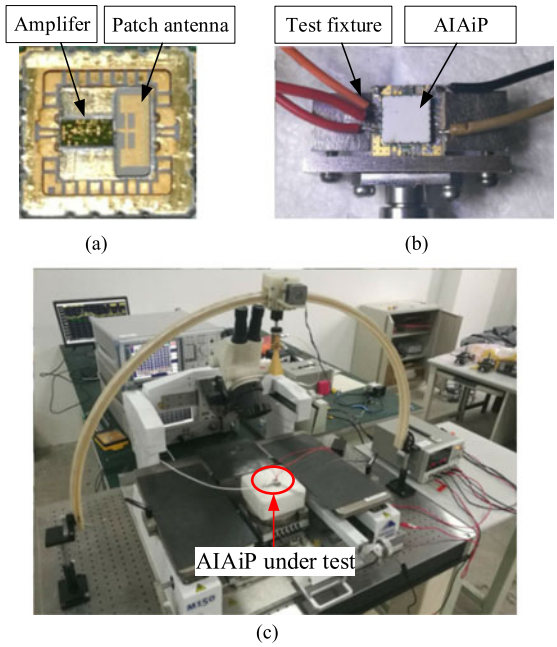

Fig. 6. Photograph and the measurement setup of the proposed AIAiP. (a) Photograph of the AIAiP (without package lid). (b) AIAiP is assembled on a PCB and then fixed on a test fixture for the measurement. (c) Measurement setup of the AIAiP radiation patterns.

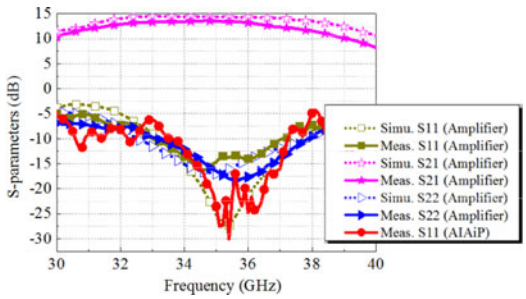

Fig. 7. *S*-parameters of the amplifier and the AIAiP.

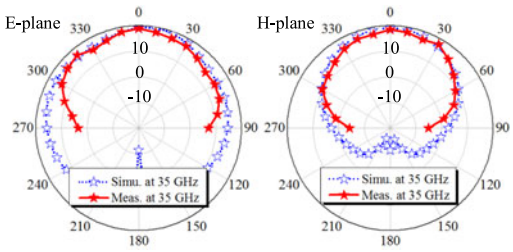

Fig. 8. Radiation patterns of the AIAiP at 35 GHz.

forms the proposed AIAiP. Fig. 6(a) and (b) shows the photographs of the AIAiP. As Fig. 6(b) presented, a test fixture is used to fix the AIA for the flowing test. The VNA is also used to test the reflection coefficient of the AIA, and the measurement result is also presented in Fig. 7. It is seen that the AIAiP has a -10-dB bandwidth of 3.8 GHz, from 33.4 to 37.2 GHz. The antenna radiation patterns are measured based on the setup reported in our previous work [11], as Fig. 6(c) depicted. The gain of the AIAiP is then calculated using the Friis transmission formula [12]. Fig. 8 presents the measured and simulated patterns at 35 GHz, respectively. As is shown, the proposed AIA has a

TABLE I
COMPARISON TO THE STATE OF THE ART

Ref.	Approach	Freq. (GHz)	Gain (dBi)	Size (mm^2)	Package
This work	Antenna* with amplifier#	35	18.9	7×7	Sealed QFN package
[3]	Antenna# with LNA#	60	12	3×2.8	Die, not packaged
[4]	Antenna# with amplifier# and lens	78	18	12×12	Die, not packaged
[6]	Antenna$ with LNA#	60	35	13×20	LTCC package but not sealed
[7]	Antenna$ with LNA#	90	21.2	3×1.9	PCB package but not sealed

* is implemented with the PCB process.
# is implemented with the semiconductor process.
$ is implemented with the LTCC process.

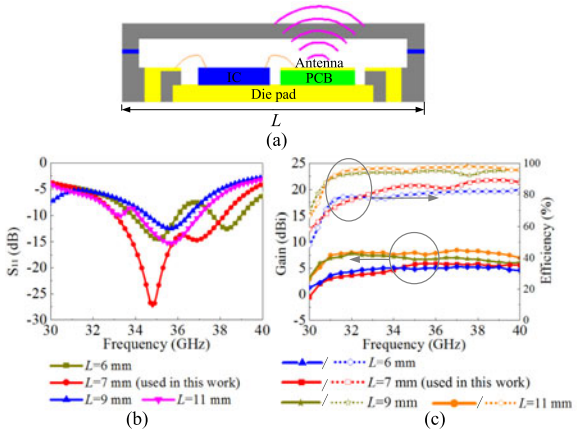

Fig. 9. Investigate the influence of package size on the performance of the antenna for the future work. (a) Proposed AIA in a package with a size of $L \times L$ mm^2. (b) Antenna reflection coefficient with different L. (c) Antenna gain and efficiency with different L (the gain of the amplifier is not included in the antenna gain in this figure).

peak gain of 18.9 dBi at 35 GHz, and the 3-dB beamwidths are about 100° and 70° in the *E*-plane and *H*-plane, respectively. A reasonably good agreement between the simulated and measured results can be observed except when $\theta < -60°$ in the E-plane. This discrepancy is mostly due to the existence of the metal test fixture of the AIAiP. It is worthwhile mentioning that the simulated gain of the AIAiP is the sum of the simulated gain of the patch antenna and the measured gain of the amplifier.

The performance of the proposed AIAiP is summarized and compared to the state of art in Table I. As is shown, with a sealed package, a good performance is achieved by our antenna. In addition, compared to other AIAs, the proposed AIA is much more suitable for working in harsh environments especially when a die is used to form the AIA.

IV. INVESTIGATION OF THE PACKAGE SIZE INFLUENCE FOR THE FUTURE WORK

As discussed in the preceding sections, the package used in this work is a specified one. However, in the future work, we are planning to integrate many more chips (like the switch, phase shifter, and oscillator) with the antenna in a package to implement an SiP in Ka-band. Then, the size of the package needs to be increased to accommodate these chips and antenna. thus, in this letter, the influences of the package size ($L \times L$ mm^2) on the performance of the antenna are investigated. It is seen from Fig. 9(b) that the package size has a significant effect on the reflection coefficient of the antenna. This may be due to the edge effect of the package. Therefore, changing the package size, the impedance matching of the antenna needs to be redesigned. Additionally, according to Fig. 9(c), increasing the package size will improve the antenna gain and efficiency obviously. This may be because the metal die pad of the package could be regarded as a reflector of the antenna. Increasing the package size means raising the reflector size, and then the antenna gain and efficiency will be improved.

V. CONCLUSION

This letter presents an AIAiP for the Ka-band applications. A GaAs amplifier and a microstrip patch antenna have been designed, respectively, and then are assembled together in a package for test. The measured operating frequency of the proposed AIAiP is from 33.4 to 37.2 GHz, while a peak gain of 18.9 dBi is obtained at 35 GHz. Additionally, the influence of the package size on the antenna performance has been studied. It is helpful for the future AIAiP and SiP design.

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