Directional Correction of Over-Current Relay Using Voltage Slope in Multi Terminal DC System With SFCL

Sang-Jae Choi and Sung-Hun Lim

***Abstract*—In the DC system, a larger fault current flows due to capacitor discharging than in an AC system. In the event of a fault in the MTDC (multi-terminal DC), although the magnitude of the current flowing through each DCCB (DC circuit breaker) varies depending on the fault location, all capacitors in MTDC may discharge and all DCCB may interrupt. In this paper, the trigger type SFCL (superconducting fault current limiter) were constructed to limit large fault current, and DC OCR (overcurrent relay) was designed to prevent interrupting malfunction according to the impact of SFCL. When the fault current was small by operation of SFCL, the DCCB did not interrupt or trip time is delayed. These problems cause malfunction even when DC OCR is applied. Therefore, DC OCR requires an additional correction method. In this paper, a new correction method was proposed in consideration of the current direction and voltage slope. The simulation was conducted according to four cases, and the proposed OCR correction was verified to eliminate malfunctions through case studies.**

***Index Terms*—MTDC (multi-terminal DC), SFCL (superconducting fault current limiter), DC OCR (overcurrent relay), directional correction.**

I. Introduction

THE need for a multi-terminal DC system is emerging due to the increase in DC distributed power sources such as PV and the increase in the consumption of DC load. The MTDC (multi-terminal DC) system has the advantage of excellent system stability using a converter, but protection equipment and regulation to cope with a DC fault accident have not been specifically established. In a MTDC system, a very large overcurrent flows due to a capacitor discharge in the case of a fault. Overcurrent is also very fast at the rate at which it increases, which can destroy many facilities in the DC system. Therefore, research to reduce the operating time of the DCCB (DC circuit breaker) is ongoing. DCCBs are largely divided into four types: passive, active, solid, and hybrid, and passive and active circuit breakers are relatively inexpensive, but are difficult to apply because the interruption time is relatively long. Currently, hybrid DCCB was developed to be able to block within 2 ms [1]. However, hybrid DCCB has a very high cost to capacity. Therefore, measures to reduce the circuit breaker current capacity have been studied, and a representative solution is to use a FCL (fault current limiter) [2].

However, the resistive FCL has a long limiting response time, so it is difficult to apply it to a DC system where the fault current rapidly increases within 1 ms [3]. Due to this, the SFCL (superconducting fault current limiter) using the superconducting characteristics of the superconductor not only effectively limit the fault current in a short time, but also there is no need to use a large-capacity DCCB. Various studies have been conducted on the types of superconducting fault current limiters [4], [5]. Among them, the trigger type SFCL used in this document have a switching element connected, unlike the resistive type SFCL. In general, the resistive type SFCL cannot protect the superconducting element from a large fault current, and thus the superconducting element often loses its superconductivity. In order to prevent this, a trigger type SFCL, in which the voltage across the superconducting element is measured to operate the switch, and the fault current limit is limited by the CLR, not the superconducting element, was studied [6]–[8]. This method has a great advantage in terms of economy by reducing the amount of superconducting elements used. For example, the SFCL applied in the 154 kV class transmission system in south Korea also applied the trigger type SFCL, not the resistive type SFCL.

On the other hand, an appropriate protection method is required to operate DCCB. Established protection schemes for DC system include traveling wave, overcurrent, voltage level and current differential protection [9]–[12]. According to a collaborative research conducted in the TEWNTIES project in 2010, the best method for DC system protection is the current differential method using backup by overcurrent protection [13]. However, this method is practically possible only when a fast and reliable communication system base between each point is established. As an alternative to this, there is a method through correction for OCR (overcurrent relay) commonly used in AC systems [14]–[16].

In general, when SFCL is applied in the AC power system, the trip time of the OCR is delayed [16], [17]. Since the delay

Manuscript received November 30, 2020; revised February 25, 2021 and March 18, 2021; accepted March 18, 2021. Date of publication March 26, 2021; date of current version May 24, 2021. This work was supported by Korea Electric Power Corporation under Grant R19XO01-19 and in part by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MOE) under Grant 2020R1F1A1077206. *(Corresponding author: Sung-Hun Lim.)*

The authors are with the Department of Electrical Engineering, Soongsil University, Seoul 156-743, South Korea (e-mail: choisj203@gmail.com; superlsh73@ssu.ac.kr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TASC.2021.3068612.

Digital Object Identifier 10.1109/TASC.2021.3068612

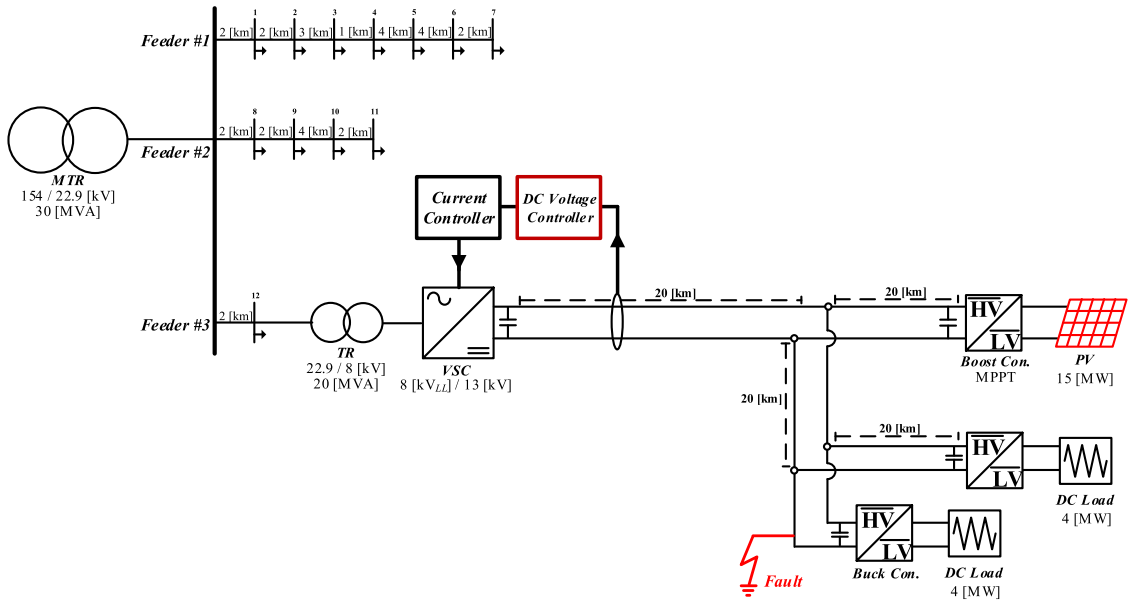

Fig. 1. Configuration of Multi-Terminal DC System with SFCL connected with AC Distribution System.

of the trip time causes the circuit breaker to malfunction or non-tripping, a correction method of OCR is absolutely necessary. On the other hand, since the fault current of the DC system flows out of all capacitors connected to the fault location, the probability of malfunction and non-tripping is higher if a conventional OCR correction algorithm is used. Therefore, OCR correction combined with DC fault protection algorithm was proposed. In this paper, along with SFCL, it is modeled a DCCB and a DC OCR, which are essential for multi-terminal DC system protection. In consideration of the fault current characteristics and the DC voltage characteristics in the multi-terminal DC system, new algorithm for the DC OCR was proposed. Modeling for the mathematical characteristic equation of each component comprising the DC OCR and SFCL, proposed directional correction method of DC OCR was simulated with the PSCAD/EMTDC (power system computer aided design/electromagnetic transient including direct current analysis program). And the application of DC OCR using the proposed algorithm was confirmed to be contributed to preventing malfunction of DCCB.

II. Fault Current in Multi-Terminal DC System with SFCL

A. Multi-Terminal DC System Configuration

In the current study, a multi-terminal DC system connected to the AC distribution system was constructed through VSC (voltage-sourced converter) and coupling transformer, as show in Fig. 1. The MTDC (multi-terminal DC) system consists of two load, VSC and PV terminal. The VSC is constructed in the form of a 3-Level converter. The PV capacity is 15 [MW], assuming maximum power, and each load consumes 4 [MW]. Therefore, VSC transmits 7 [MW] of power to the AC system. The power in VSC can be changed according to PV output and load consumption. To connect the PV to the MTDC system, a boost converter was modeled and it was controlled according to the MPPT (maximum power point tracking) algorithm [18], [19]. Each DC load is connected to the MTDC system through a buck converter, and the consumption power of the load is kept constant. The SFCL (superconducting fault current limiter) was applied at the front feeder to BUS1 where the largest fault current flows in the DC system.

The cable that composes the MTDC system is modeled by aluminum sheath segment stranded XLPE (Cross linked polyethylene insulated cable), and the maximum conductor resistance at 20° is 0.0176 Ω/km, and the capacitance is 0.33 uF/km. The ACSR 170/40 is used as the overhead line, and the maximum conductor resistance at 20° is 0.1682 Ω/km.

B. Fault Current Flow in Multi-Terminal DC Systems

From Fig. 2, the fault location is assumed to be at load1, but the fault may occur in PV or load2, and more feeders can be connected to BUS2. Also, since the capacitor of VSC is generally the largest in MTDC system, the point where the fault current is greatest is also BUS1. For this reason, it was decided that the most effective location to applying SFCL was at front feeder of BUS1.

The fault occurred at load 1, as can be seen in Fig. 2. The fault type is pole to pole. In a DC system, the initial fault current is the capacitor discharge current [20], [22]. Since the capacitors of the modeled multi-terminal DC system, are connected to two loads, VSC and PV, the fault current flowing at this time can be plotted as shown in Fig. 3.

The fault current flows through a total of three paths. The red color is the path through which the fault current flows from the VSC capacitor. Blue is the path of fault current flowing from the boost converter capacitor of PV, and green is the path of fault current flowing from the buck converter capacitor of load2.

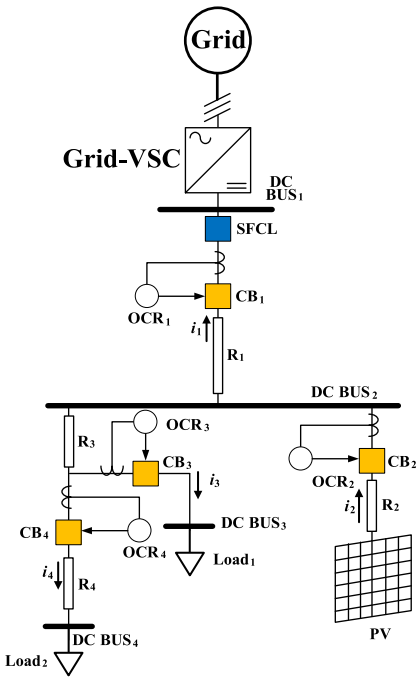

Fig. 2. Normal State Current Flow in Multi-Terminal DC System with SFCL .

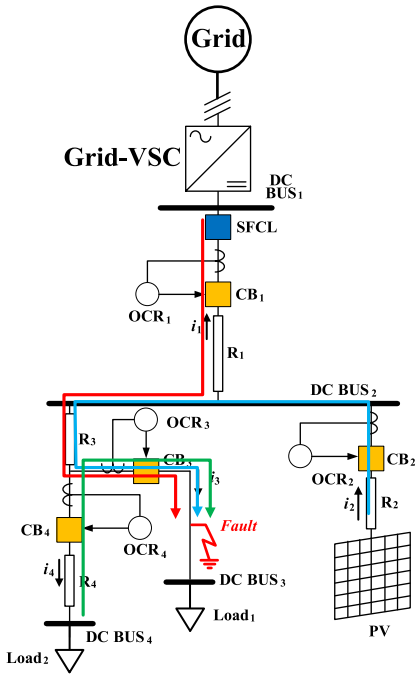

Fig. 3. Fault Transient State Current Flow in Multi-Terminal DC System with SFCL .

Equation (1) below is an equation representing the magnitude of the fault current. The fault current can be mathematically analyzed by the parallel capacitor connected to each terminal and the line impedance. τ_1, τ_2, and τ_4 can be obtained by the line impedance of the fault current path and each parallel capacitor. Since the τ value is proportional to the capacitor capacity, it can

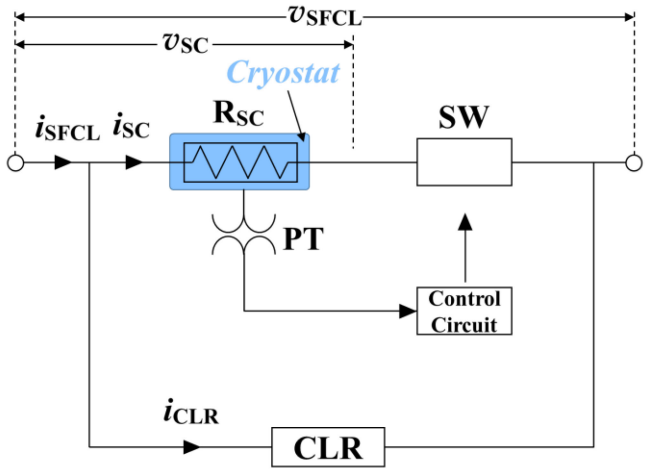

Fig. 4. Equivalent Circuit of Trigger Type SFCL(Superconducting Fault Current Limiter).

be inferred that the larger the parallel capacitor, the larger the initial fault current. When modeling a DC cable, the size of the capacitance is much larger compared to the serial inductance. Therefore, it was calculated ignoring the inductance and could be assumed as a first-order circuit.

$$\begin{cases} i_{fault1} = \frac{v_{c1}(0)}{R_1+R_3}\, e^{-t/\tau_1} \\ i_{fault2} = \frac{v_{c2}(0)}{R_2+R_3}\, e^{-t/\tau_2} \\ i_{fault4} = \frac{v_{c4}(0)}{R_4+R_3}\, e^{-t/\tau_4} \\ i_{fault} = i_{fault1} + i_{fault2} + i_{fault4} \end{cases} \tag{1}$$

The practical fault current is different from equation (1) because it considers even the arc current of the fault contacts. However, the initial fault current is more affected by the capacitor discharge current than the arc component, so the initial fault current is similar to equation (1).

C. Modeling of SFCL

The trigger type SFCL can effectively limit the fault current through the CLR (current limiting reactor/resistor) while protecting HTSC (high-temperature superconductor) from being damaged by fault current. Fig. 4 below shows the equivalent circuit of trigger type SFCL [4]–[6]. Trigger type SFCL connects SW in series with HTSC and CLR in parallel. SW is normally closed, but when HTSC is quenched, open it to commutate the fault current toward CLR. R_{SC}, the resistance of HTSC, used a model that is affected by the fault current only when quenched, and increases with time after quench. Equation (2) below shows the model used for HTSC resistance [23].

$$R_{SC}(t) = \begin{cases} 0 \ (t < t_{fault}) \\ R_n\left[1 - exp\left(-\frac{t-t_{fault}}{\tau}\right)\right]^{\frac{1}{2}} \\ (t_{fault} < t < t_{SWopen}) \end{cases} \tag{2}$$

In normal state, i_{CLR} is 0 because superconducting resistance R_{SC} is 0. After a fault occurs, fault current flows through the

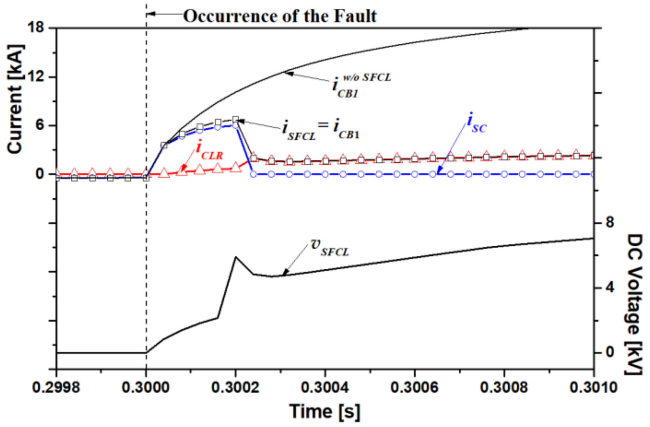

Fig. 5. Operating Current and Voltage Waveform of Tigger type SFCL .

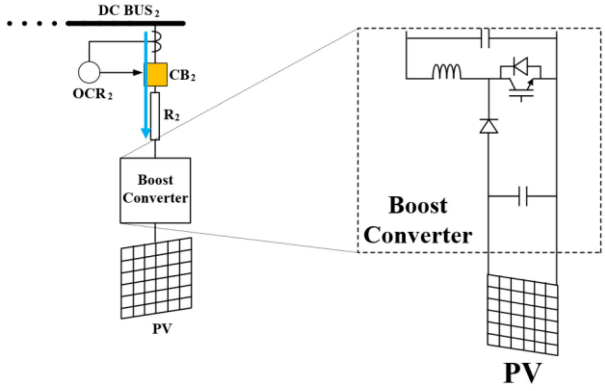

Fig. 6. Fault Current Reversal by Capacitor Recharging on PV Generating Terminal .

CLR and the voltage of HTSC v_{SC} is induced. At this time, a signal is generated to open SW in the control circuit based on the v_{SC}. After the SW opens, the fault current flows through the CLR and is limited.

Fig. 5 shows the voltage and current waveforms when trigger type SFCL is operated. When SFCL is not applied, it can be seen that the current flowing through CB1 increases significantly. When SFCL is applied, i_{SC} rises first due to fault current. At this time, when the i_{SC} becomes larger than the threshold current, the HTSC is quenched and the current flows to the i_{CLR}. After that, when v_{SC} rises above the threshold voltage, SW opens and fault current commutates toward CLR.

D. Impact of SFCL

As can be seen from Fig. 3, only the current through the red path is affected by the SFCL. This is simply proved through Equation (1). When the SFCL operates, resistance in series with R_1 increases in Equation (1). So i_{fault1} gets smaller. At this time, the blue path current, which is the path of fault current from PV, is not limited. Due to this, the trip time of CB3 is delayed, whereas the trip time of CB2 is not. There are various correction methods to solve this problem, but in DC [12], [13], unlike AC, there are many sources of fault current, so it is not appropriate to apply these conventional methods.

Therefore, an algorithm that can determine the direction according to the sign of the current has been developed. This makes it possible to prevent tripping in all cases except when a failure occurs on the PV side. However, in this study, it was not considered that the reverse current flows after the fault elimination. This will be confirmed again in Section III.

III. Over Current Relay Directional Correction With Voltage Slope

A. Conventional OCR Operating Characteristic Equation

Equation (3) is the standard formula for OCR used in Korean distribution systems

$$T_{trip} = TD\left(\frac{A}{M^p - 1} + B\right) \tag{3}$$

A, B, and p mean relay constants. TD is a time dial and is a changeable parameter proportional to the trip time. Likewise, I_{pickup} is a threshold value at which the system operator starts generating trip signals.

B. Directional Correction

In DC, it is easier to determine the direction of fault current compared to AC. When the current changes from positive to negative or from negative to positive, it can be seen that the current direction is reversed. By using this, the malfunction of the relay can be prevented. This can be set simply by making a difference between the load terminal relay and the generator terminal relay. For instance, if a fault occurs at the load end, the current direction is the same as in the normal state and fault state. However, when a fault occurs in the generator terminal, the direction of the current changes between the normal state and fault state.

- Method 1) The load terminal relay trips on when the direction does not change and the fault current becomes larger than the threshold value.
- Method 2) The generator terminal relay trips on when the direction changes and the fault current becomes larger than the threshold value.

However, the method of correction through the current direction has a big problem. In general, when the fault is removed, the discharged capacitor is recharged with an overcurrent in the reverse direction. Fig. 6 shows the direction of current flow when the capacitor is recharged after the fault is removed.

In the existing direction correction method 2), the direction of the current at the generator terminal does not change and it is set to trip when overcurrent flows. Therefore, the direction of the current is reversed again due to recharging, and OCR2 trips due to the flow of overcurrent. In other words, the CB2 operates even though the fault is removed. To solve this problem, in this paper, we consider charging and discharging of capacitors through voltage slope. That is, if the cause of the current flowing in the forward direction is due to charging, no trip. Conversely, if overcurrent occurs due to discharge, it is judged as a fault, OCR2 trips, and CB2 is open.

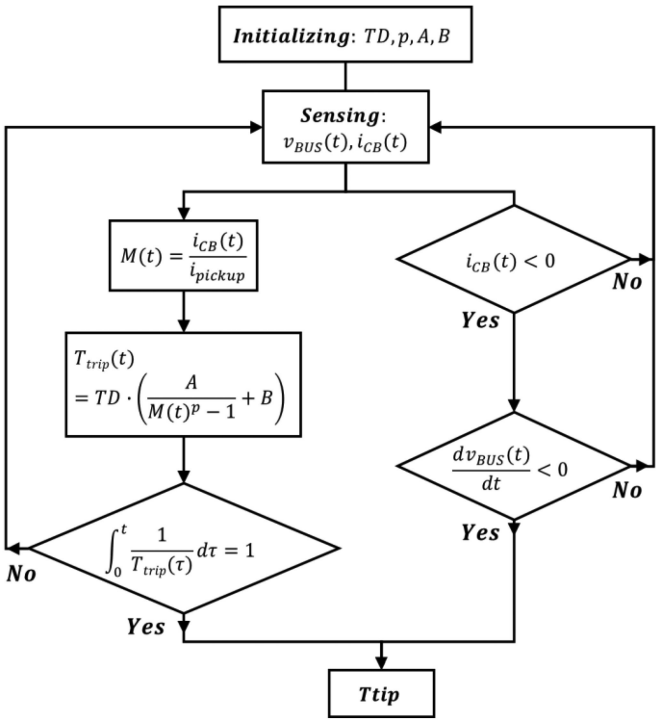

Fig. 7. Proposed Algorithm of DC OCR (Overcurrent Relay) Directional Correction with Voltage Slope.

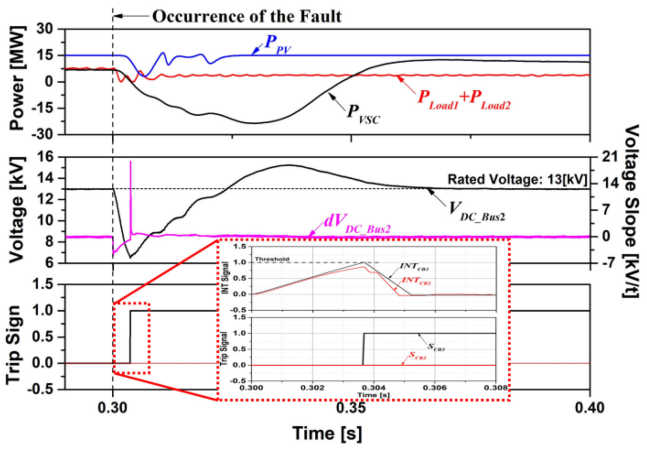

Fig. 8. Power Flow and Voltage of DC Bus2, Trip Signal waveform in case1 (fault only).

C. Voltage Slope Correction

In case of fault, the voltage of the capacitor can be obtained through the differential equation as shown in equation (4) & (5).

$$v_{BUS2} = v_{c2}\ (t) - R_2 C \frac{dv_{c2}\,(t)}{dt} \tag{4}$$

$$v_{BUS2} = \ 13u\,(t)\,,\ v_{c2}\ (0) = \ 0 \tag{5}$$

$$v_{c2}\ (t) = v_{BUS2}\ \left(1 - e^{-t/\tau}\right),\ \tau\ = R_2\ C \tag{6}$$

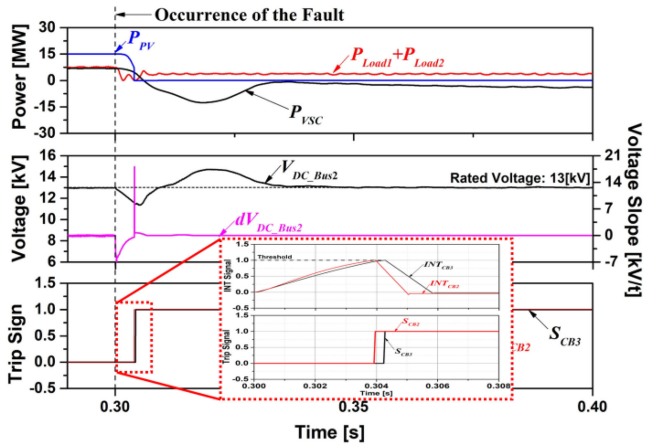

Fig. 9. Power Flow and Voltage of DC Bus2, Trip Signal waveform in case2 (fault with SFCL).

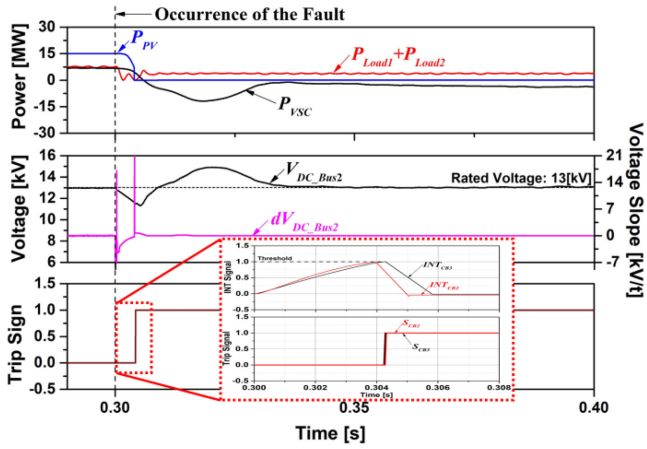

Fig. 10. Power Flow and Voltage of DC Bus2, Trip Signal waveform in case3 (fault with SFCL and DC OCR correction method using current direction).

Equation (5) is the solution to Equation 4, and through this, the slope of the capacitor voltage can be obtained. At this time, the voltage slope is positive during charging and the voltage slope is negative during discharge.

Therefore, the algorithm can be designed to prevent trips during charging. The proposed algorithm is shown in Fig. 7. The bus voltage and the current flowing through the CB are sensed and the T_{trip} value is calculated based on this. When its reciprocal integral value reaches 1, a trip signal is generated. Meanwhile, the sign of the differential value between the current and the voltage on the bus side is determined.

IV. Simulation and Results

A. Simulation Setup

The model used in the simulation was composed of the A system in Section II above. The DC system is composed of PV, DC Load, and VSC terminals. The fault location is assumed on the DC Load1 side. At this time, the location of SFCL is located in front of the CB on the VSC side. The PV irradiation amount

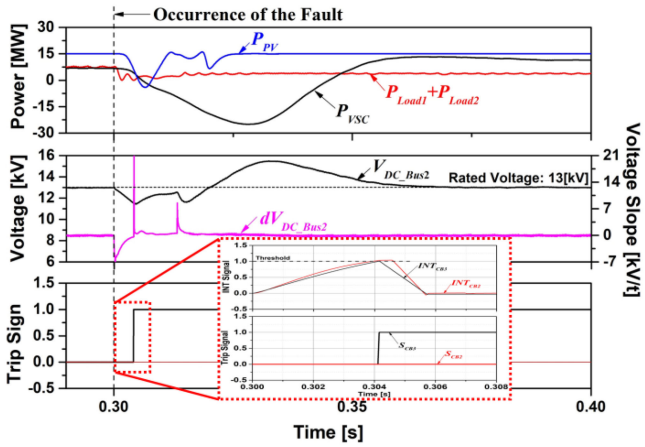

Fig. 11. Power Flow and Voltage of DC Bus2, Trip Signal waveform in case4 (fault with SFCL and DC OCR correction method using current direction and voltage slope).

TABLE I
PARAMETERS FOR SIMULATION

Classification	Description	Value & Unit
PV (Photovoltaic)	Irradiation	1200 [W/m^2]
	Temperature	28 [℃]
	Capacitor Size	5000 [uF]
	Rating Voltage	10.7 [kV]
DC Load	Load Size	4 [MW]
	Capacitor Size	200 [uF]
	Rating Voltage	10 [kV]
VSC(Voltage Sourced Converter)	Voltage Con.	13 [kV]
	Reactive Power Con.	0 [Mvar]
	Capacitor Size	8000 [uF]

and temperature, and the mode of each converter are shown in the Table I below. In addition, the size of each converter's ripple adjustment capacitor is also listed in Table I.

B. Case Study

The system used in this paper is shown in Fig. 1. At this time, four cases were reviewed according to the application of SFCL and the OCR correction method

- *Case 1:* W/O SFCL, No OCR Correction
- *Case 2:* with SFCL, No OCR Correction
- *Case 3:* with SFCL, Directional Correction with only Current Direction
- *Case 4:* with SFCL, Directional Correction with Current Direction and Voltage Slope

In the normal state, PV outputs 15 MW. Each load consumes 4 MW, so a total of 8 MW is consumed. Therefore, 7 MW is converted to the AC distribution system side through VSC. After a fault occurs, CB2 is not tripped, but only CB3. The trip time of CB3 is 3.7 ms.

Since load1 is dropped after the CB3 trip, the total load consumption is 4 MW and PV is not dropped, so it outputs 15 MW again. No delay due to SFCL effect. In VSC, overcurrent flows as the discharged capacitor is recharged, and power flows in the DC side direction. After charging is completed, 11 MW is converted to the AC side.

In Case 2, the current was greatly reduced due to SFCL, and the trip time of CB3 was significantly delayed from 3.7 ms to 4.25 ms. However, CB2 trips before CB3 because there is no delay due to SFCL effect. That is CB2 malfunctions. Due to this, PV output becomes 0 after fault removal.

In Case 3, when a fault occurs, it does not trip because the current direction in CB2 is in the reverse direction. However, after the fault is removed, a positive overcurrent occurs due to the recharging of the capacitor, so it trips again. Eventually, CB2 malfunctions.

In the last case, the proposed directional correction was applied. Since the voltage slope is positive as the voltage rises after the fault, the trip signal of CB2 does not occur by the proposed algorithm. Therefore, it can be seen that CB2 does not malfunction before and after fault. However, the trip delay of CB3 still exists due to the influence of SFCL.

V. CONCLUSION

In this paper, the protection relay method of DC circuit breaker in multi-terminal DC system was reviewed. Each CB (circuit breaker) trips through OCR (over-current relay), and the trip time is inversely proportional to the magnitude of the fault current.

Therefore, due to the use of SFCL (superconducting fault current limiter), the size of the fault current could be effectively reduced, but the trip time was delayed. Due to this, the PV side relay malfunctioned. If the directional correction considering the current direction is used, CB malfunction due to a failure can be prevented, but after the fault is removed, the malfunction occurs due to overcurrent due to capacitor recharging.

Finally, an algorithm that considers the charging and discharging of capacitors was proposed using the current direction and voltage slope. By applying the proposed algorithm to the modeled system, the malfunction of CB2 could be effectively prevented. In order to minimize the fault section when configuring the MTDC system, the proposed method in this paper is effective. Therefore, this study can contribute when designing future MTDC system or connecting additional terminals.

REFERENCES

[1] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid HVDC breaker," ABB Grid Systems, Technical Paper, Nov' 2012.
[2] S.-H. Lim, S. Ko, and T.-H. Han, "Analysis on current limiting characteristics of a transformer type SFCL with two triggering current levels," *Physica C: Supercond.*, vol. 484, pp. 253–257, 2013.
[3] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-Circuit and ground fault analyses and location in VSC-Based DC network cables," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3827–3837, Oct. 2012.
[4] J. Kozak, M. Majka, S. Kozak, and T. Janowski, "Comparison of inductive and resistive SFCL," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, Jun. 2013, Art. no. 5600604.
[5] S. Lim, "Operational characteristics of flux-lock type SFCL with series connection of two coils," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 1895–1898, Jun. 2007.
[6] S. Lim, and S. Lim, "Current limiting and recovery characteristics of a trigger-type SFCL using double quench," *IEEE Trans. Appl. Supercond.*, vol. 28, no. 3, Apr. 2018, Art. no. 5601305.
[7] O. Hyun, K. Park, J. Sim, H. Kim, S. Yim, and I. Oh, "Introduction of a hybrid SFCL in KEPCO grid and local points at issue," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 1946–1949, Jun. 2009.

[8] W. Kim *et al.*, "Dynamic characteristics of a vol. 22.9 kV hybrid SFCL for short-circuit test considering a simple coordination of protection system in distribution networks," *IEEE Trans. Appl. Supercond.*, vol. 22, no. 3, Jun. 2012, Art. no. 5601404.

[9] S. Le Blond, R. Bertho, D. V. Coury, and J. C. M. Vieira, "Design of protection schemes for multi-terminal HVDC systems," *Renewable Sustain. Energy Rev.*, vol. 56, pp. 965–974, 2016.

[10] Y. Zhang, N. Tai, and B. Xu, "Fault analysis and traveling-wave protection scheme for bipolar HVDC lines," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1583–1591, Jul. 2012.

[11] S. Liang *et al.*, "Parameter matching and optimization of a hybrid type DC SFCL considering the transient characteristics of VSC-Based DC systems," *Energies*, vol. 12, 2019, Art. no. 3522.

[12] Y. Zhang, Y. Li, J. Song, B. Li, and X. Chen, "A new protection scheme for HVDC transmission lines based on the specific frequency current of DC filter," *IEEE Trans. Power Del.*, vol. 34, no. 2, pp. 420–429, Apr. 2019.

[13] D. Jovcic, D. van Hertem, K. Linden, J. Taisne, and W. Grieshaber, "Feasibility of DC transmission networks," in *Proc. 2nd IEEE PES Int. Conf. Exhib. Innov. Smart Grid Technol.*, Manchester, 2011, pp. 1–8, doi: 10.1109/ISGTEurope.2011.6162829.

[14] S. Lim, and S. Lim, "Analysis on coordination of over-current relay using voltage component in a power distribution system with a SFCL," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, Aug. 2019, Art. no. 5603605.

[15] S. Lim, and S. Lim, "Analysis on operational improvement of OCR using voltage component in a power distribution system for application of SFCL," *J. Electr. Eng. Technol.*, vol. 14, pp. 1027–1033, 2019.

[16] S. Lim, and S. Lim, "Analysis on coordination of over-current relay using voltage component in a power distribution system with a SFCL," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, Aug. 2019, Art. no. 5603605.

[17] S. Lim, and S. Lim, "Analysis on protective coordination between over-current relays with voltage component in a power distribution system with SFCL," *IEEE Trans. Appl. Supercond.*, vol. 30, no. 4, Jun. 2020, Art. no. 5601706.

[18] K. H. Hussein, I. Muta, T. Hoshino, and M. Osakada, "Maximum photovoltaic power tracking: An algorithm for rapidly changing atmospheric conditions, generation, transmission and distribution," *IEE Proc.*, vol. 142, no. 1, pp. 59–64, 1995.

[19] O. Wasynczuk, "Dynamic behavior of a class of photovoltaic power systems," *IEEE Trans. Power App. Syst.*, vol. 102, no. 9, pp. 3031–3037, Sep. 1983.

[20] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-Circuit and ground fault analyses and location in VSC-Based DC network cables," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3827–3837, Oct. 2012.

[21] A. Berizzi, A. Silvestri, D. Zaninelli, and S. Massucco, "Short-circuit current calculations for DC systems," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 990–997, Sep.-Oct. 1996.

[22] C. Li, C. Zhao, J. Xu, Y. Ji, F. Zhang, and T. An, "A Pole-to-Pole short-circuit fault current calculation method for DC grids," *IEEE Trans. Power Syst.*, vol. 32, no. 6, pp. 4943–4953, Nov. 2017.

[23] J.-S. Kim, S.-H. Lim, and J.-C. Kim, "Comparative analysis on current limiting characteristics of hybrid superconducting fault current limiters (SFCLs) with first half cycle limiting and non-limiting operations," *J. Elect. Eng. Technol.*, vol. 7, no. 5, pp. 659–663, 2012.