Stacked Josephson Junction Arrays for the Pulse-Driven AC Josephson Voltage Standard

Oliver Kieler, Ruediger Wendisch, Rolf-Werner Gerdau, Thomas Weimann, Johannes Kohlmann, and Ralf Behr

***Abstract*—We developed a fabrication process to establish large arrays of up to 5-stacked Josephson junctions for the Josephson Arbitrary Waveform Synthesizer (JAWS). SNS-type Josephson junctions with Nb_xSi_{1-x} barriers are used for this application. By modifying our standard window process, e.g. to add a CMP (chemical mechanical polishing) and an ALD (atomic layer deposition) step, the yield of this process was increased. An output voltage of 1 V RMS could be achieved by using 4 JAWS arrays in series with a total number of 60,000 5-stacked junctions. The investigation of the current-voltage characteristics (IVC) showed an interesting and potentially useful feature. The required pulse amplitude per junction for getting the maximum Shapiro step width reduces for higher junction stacks. We found that the pulse power linearly reduces with the square of the junction number in the array. The origin of this effect might be a strong neighbour-neighbour interaction of the junctions, which are closely arranged within the stacked configuration. This might generate a strong self-synchronization of the junctions.**

***Index Terms*—AC Josephson voltage standard, Josephson arbitrary waveform synthesizer, SNS Josephson junction, stacked Josephson junctions, self-synchronization.**

I. Introduction

THE pulse-driven AC Josephson Voltage Standard [1], which is also called "Josephson Arbitrary Waveform Synthesizer" (JAWS) has already demonstrated its enormous potential for many applications in the voltage metrology community in the last couple of years. The JAWS is characterized by unique characteristic features: quantum-based precision voltages, spectral purity, large frequency bandwidth from DC to MHz range, arbitrary waveforms, low noise and no drift. Output voltages of > 2 V RMS [2] or even 4 V RMS [3] have already been demonstrated. The challenging tasks of further increasing the output voltage, reducing the complexity and overall costs of JAWS systems are the motivation for various efforts. As the number of junctions in a single array is limited shown for example in [4], [5], the common idea is to operate more junctions in a parallel configuration. For example, the implementation of different types of on-chip power dividers was successfully realized already [6], [7]. Another approach of implementing an optical pulse-drive with on-chip photodiodes (operated at 4 K) showed already first promising results [8], but parallelization of many photodiodes is still a challenging task.

Both methods are already combined with the technological approach of implementing vertically stacked Josephson junctions in the series arrays. For this task a sophisticated fabrication technology with low parameter spread and high yield is required, as for the programmable Josephson voltage standard too. Recently it was shown by PTB [9] and NIST [10] that 3-stacked junction arrays show high-quality properties and are established for the use in voltage standard circuits already.

This paper describes the effort to extend the stacks up to five junctions while providing a sufficient yield and simultaneously low parameter spread (section II). We also present the results of the Shapiro step generation for different array geometries, i.e. the influence of the number of junctions per array and number of junctions per stack on the required pulse amplitude per junction (i.e. peak pulse power) at different operation frequencies (section III).

II. Fabrication

SNS-type Josephson junctions (JJ) with non-hysteretic current-voltage characteristic (IVC) and Nb_xSi_{1-x} [11] as the normal-metal barrier material are used for the realization of JAWS systems at PTB (S…superconductor, N…normal conductor). The Josephson junctions of our circuits are embedded in the center line of a coplanar waveguide (CPW), which is terminated at the end of the array by 50 Ω on-chip resistors. The CPW impedance is tapered, as suggested in [12], from 50 Ω to 37 Ω. There is no difference in the layout for the JAWS circuits with different number of stacks. While keeping the junction stack distance constant, the total array length was changed from about 15 mm (2500 JJ per array) up to about 23 mm (4000 JJ per array).

The simplified schematics of the window fabrication process for the 5-stacked Josephson junction arrays (fabrication steps 1-4) is shown in Fig. 1. The process consists of 6 main fabrication steps. The last two steps are not shown. At step 5 AuPd on-chip resistors are integrated by a lift-off process. The opening of the

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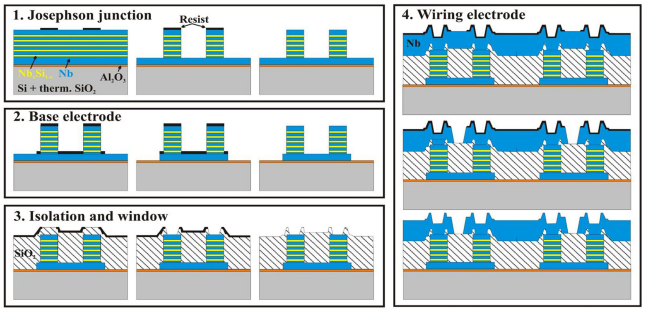

Fig. 1. Schematic of the fabrication process for 5-stacked Josephson junction arrays (first 4 steps).

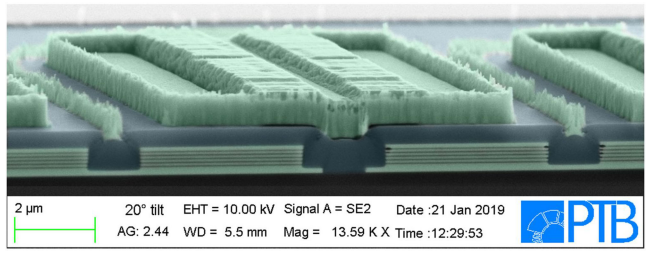

Fig. 2. SEM image of a cut into a JAWS array with 5-stacked Josephson junctions.

wire-bond contact pads (not shown, removing of the SiO_2) is done by RIE-ICP (reactive ion etching with inductive coupled plasma) in step 6. The junction multilayer itself is about 800 nm thick and 12 layers are deposited in-situ in our fully automated cluster sputter system. This system enables a high reproducibility of the Nb_xSi_{1-x} barrier composition and thickness to achieve a low spread in the junction characteristics. The complete JAWS circuit consists of 16 layer (plus 2 $\times$ SiO_2, Nb-Wiring, AuPd) and the overall thickness is more than 2 μm.

The detailed fabrication process needs about 40 fabrication steps and the clean-room cycle time for two wafers is about three weeks. In summary of the process: we have 5 $\times$ deposition, 6 $\times$ etching, 7 $\times$ electron beam lithography, 1 $\times$ lift-off and 1 $\times$ CMP. We describe in [9] more details of our standard window process for 3-stacked junctions, which is similar to the modified process presented in this paper.

The modifications required for these higher stacked junction arrays are the following. The thickness of the e-beam (electron beam lithography) resists was increased to match the different aspect ratios and to ensure the sustainability during the rather rough RIE-ICP process. As a consequence, the e-beam electron doses, the proximity correction and the development times were carefully adjusted as well. The RIE-ICP ensures the steep etch profile of nearly 90 degrees which is necessary to have the same active junction area for each junction floor in the stack. This guarantees that the whole stack has the same critical current. To ensure a good edge coverage the thicknesses of the SiO_2 (deposited by PECVD: plasma enhanced chemical vapor deposition) and the Nb-wiring were also increased. For 5 junctions per stack, thicknesses of SiO_2 and Nb-wiring are 900 nm and 1050 nm, respectively.

Two additional steps were included into our process to enable a high yield of these circuits. First, we performed a short CMP step of 10 s (polishing rate about 100 nm/min) right after the SiO_2 deposition to slightly flatten the surface topology for the following Nb-wiring layer. Second, another important modification was to introduce a 30 nm SiO_2 layer by ALD immediately before deposition of the thick SiO_2 layer by PECVD. Due to the extremely high conformity of ALD layers the complete junction stack pillar was perfectly covered to guarantee a reliable electrical isolation especially at the top edge of these pillars. Two 5-stacked junction wafers were fabricated, and 24 arrays were measured. For all these arrays no shorted stacks were observed. Only a minor number of 47 junctions were shorted (total number of junctions 375,000) by other reasons (e.g. impurities) corresponding to a junction yield of about 99.99 %. Before we implemented this ALD step we observed (5 wafers fabricated with 40 arrays each) that the upper most Nb_xSi_{1-x} layer was shorted almost always at the edges, i.e. the upper one junction stack was superconducting shorted and clearly missing in the current-voltage characteristic measured with pulses. The reason was an insufficient edge coverage of the PECVD SiO_2 at the top edge of the high pillar where notches occurred. Finally, we did the window etching of the SiO_2 in two lithographically steps, because the selectivity of the positive e-beam resist was too low to etch (by RIE-ICP with CHF_3) the relatively deep window in one single step.

Fig. 2 shows a colored SEM image of a cut into a JAWS array with 5-stacked Josephson junctions. On this picture we can clearly recognize the steep junction stacks as required. At some junctions a small under-etch into the stack can be seen. This might be the origin for slightly increasing the parameter spread of the critical current. Compared to the total junction area of 4.4 μm $\times$ 13.6 μm this effect is low enough to enable a high-quality IVC with a typical critical current spread of about 2 % to 3 % (for 20 arrays we determined a mean spread of 2.4 %). The intra wafer uniformity of the critical current density for one of the 5-stacked junction wafer (3 inch) was determined: (6.66 $\pm$ 0.07) kA/cm². Due to the comparable thick layers combined with long etching times and resist problems we observe large Nb fence structures mainly consisting of residues of the photo resist and nonvolatile etch products; fortunately, they do not disturb the operation of the JAWS circuits.

III. Measurements

The measurements presented here are performed at liquid helium temperature 4.2 K with the JAWS system described in [9], [13]. Within the scope of this paper arrays from 7 wafers were investigated with a mean critical current of 3.4 mA (range from 2.5–4.0 mA) and a mean normal state junction resistance of 3.2 mΩ (range from 2.9–3.3 mΩ). The characteristic frequency is in the range from 4–6 GHz. The number of junctions per stack or per array did not influence these basic junction parameters. The data shown for a certain array configuration (junctions per array or number of junctions per stack) are taken from at least two independent, nominally identical arrays located on

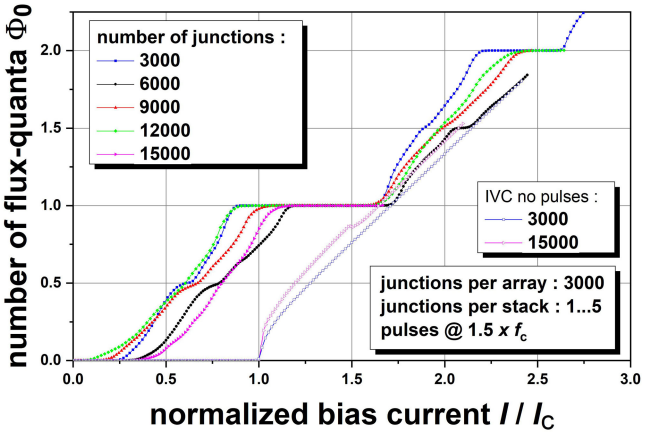

Fig. 3. Normalized current voltage characteristic without and with pulses for 1- to 5 stacks of junctions at 1.5 f_c.

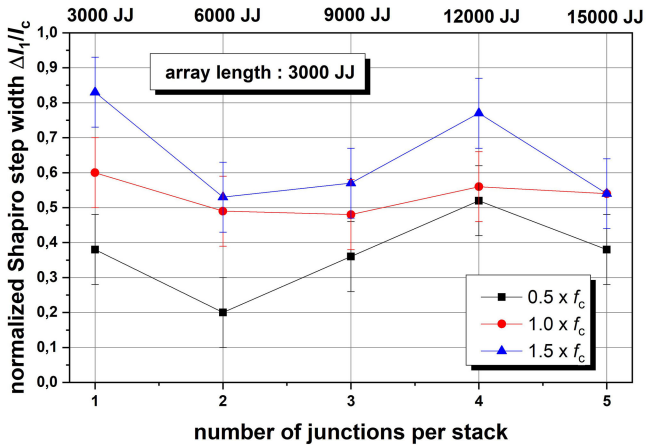

Fig. 4. Normalized Shapiro step width vs. number of junctions per stack for an array length of 3,000 junctions and three pulse frequencies.

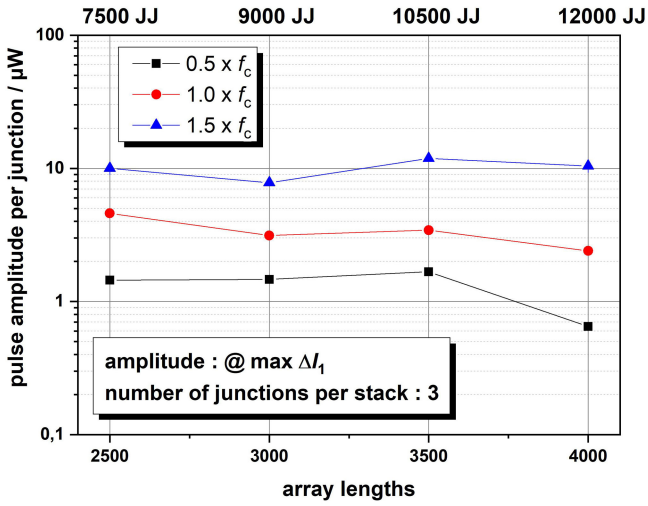

Fig. 5. Pulse amplitude per junction vs. array length for 3 junctions per stack and three frequencies. The pulse amplitude was adjusted to achieve a maximum first Shapiro step width.

one 10 mm × 10 mm JAWS chip. The error bars indicated in the figures correspond to type A uncertainty. Sometimes these uncertainty bars are not clearly visible, because they are smaller than the data point size. All measurements presented with microwave irradiation were performed with a fixed sequence of return-to-zero pulses (16 bits with all "+1") sent by a commercial pulse pattern generator (PPG) delivering ternary data signals consisting of bipolar pulses and zeros (−1, 0 and +1) with a maximum clock frequency of 15 GHz, i.e. a pulse width down to about 70 ps [13].

Fig. 3 shows the normalized IVC without pulses (for the smallest and largest arrays only) and with pulses at 1.5 × f_c (f_c: characteristic frequency, I: bias current, I_c: critical current, Φ_0: flux quanta) for 1- to 5 junctions per stacks with 3,000 junctions per array, i.e. the number of junctions increases from 3,000 to 15,000. We selected this pulse repetition frequency of 1.5 × f_c because it corresponds to our typical ratio of f_c to the clock frequency of the PPG for the JAWS application. The minimum Shapiro step width for all different stacks is about 400 μA and the step position is at (1.2–1.6) × I_c. The normalized Shapiro step width vs. number of junctions per stack from 1 to 5 (Fig. 4) indicates a good step formation even for 5-stacked junctions. At f_c the step width is about (0.48–0.60) × I_c for all stacks.

The pulse amplitude per junction required to get the maximum first Shapiro step as function of array length is shown in Fig. 5 for 3-stacked junctions at three frequencies: 0.5 × f_c, 1.0 × f_c and 1.5 × f_c. These frequencies cover the range of pulse repetition frequencies in the digital pulse codes, where the desired arbitrary waveforms are encoded. The pulse amplitude was estimated as follows. In our setup we used a PPG with a maximum peak output voltage of 500 mV. At the output of this PPG an additional broadband amplifier (picosecond 5882) with 16 dB gain was attached. The attenuation of our JAWS HF-setup (cables at 300 K, in the cryoprobe and on the chip carrier) is about 2 dB. Thus, the overall gain at the array is about 14 dB, which correspond to a voltage gain of 5.0. The impedance of our setup is matched to $R = 50\ \Omega$. The pulse amplitude power P per junction is calculated using this equation:

$$P = (5 \cdot U_{PPG})^2/(R \cdot N) \tag{1}$$

where U_{PPG} is the voltage output of the PPG, and N the number of junctions in the array. For pulse repetition frequencies $\geq f_c$ the pulse amplitude for different array lengths is roughly constant (Fig. 5), i.e. an equal power per junction is required for the Shapiro step generation. For example, this power is estimated to be 2.6 μW per junction at f_c and 12,000 junctions.

Fig. 6 shows the pulse amplitude per junction required to get the maximum first Shapiro step as a function of the number of junctions per stack for an array length of 3,000 junctions and again three frequencies. Here we can observe that the required power especially for higher stacks (4 and 5) is reduced, i.e. less power per junction is necessary. For example, this power is now 1 μW per junction at f_c and 12,000 junctions only. This is about 2.6 times less than presented in Fig. 5.

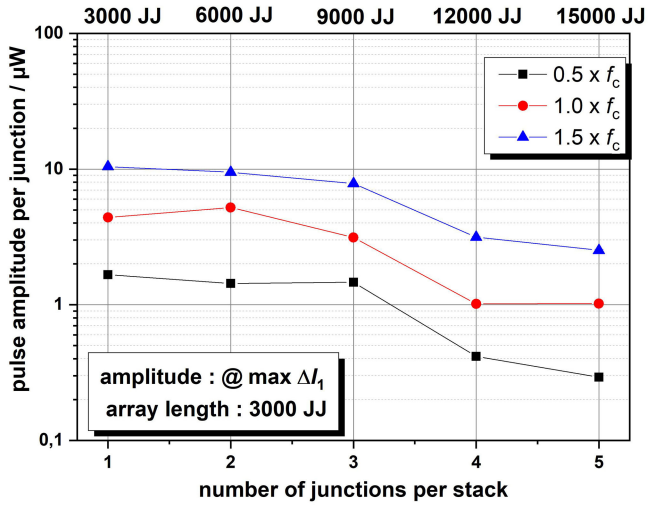

Fig. 6. Pulse amplitude per junction vs. number of junctions per stack for an array length of 3,000 junctions and three frequencies. The pulse amplitude was adjusted for maximum first Shapiro step width.

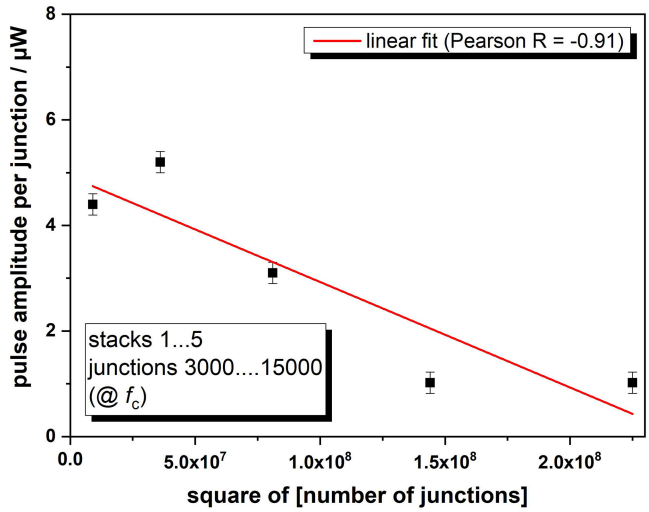

Fig. 7. Pulse amplitude per junction vs. square of number of junctions for 1- to 5-stacked junctions for an array length of 3,000 at f_c.

Therefore, we plotted the pulse amplitude per junction required to get the maximum first Shapiro step as a function of the square of the number N of junctions in Fig. 7 for 1- to 5-stacked junctions and an array length of 3,000 junctions at f_c. The required power is roughly linear in this plot (the linear regression delivered a Pearson factor of -0.91) decreasing with the square of N. Stacks with more junctions require less power per junction, and scales with $-N^2$.

This interesting feature is helping us to increase the number of junctions in our stacked arrays, which corresponds to our main goal to increase the overall output voltage of JAWS. If we need less microwave power to get a sufficient Shapiro step generation, we could further increase the number of junctions per chip.

This reduced power required could be an indication of strong self-synchronization, which is often observed in one-dimensional arrays of Josephson junctions (cf. [14], [15]). The microwave power uniformity along the length of the different arrays was not investigated. A slightly reduced Shapiro step width for the junctions at the array end is expected as investigated in previous measurements (not published). Additionally, the array design was not adapted to higher junction stacks, i.e. the impedance tapering of the CPW and the termination resistance was the same for all arrays. This should reduce the Shapiro step width due to increased attenuation and possible reflections for larger arrays and higher stacks. Such a reduction of operation margins was not observed, possibly obscured by the synchronization within the arrays. Other effects to reduce the operation margins, like e.g. self-heating, are possible too, but they are sufficiently small. A minor influence of the frequency dependent attenuation of the pulses within the setup is small enough too. This attenuation is constant for all investigated arrays, because the setup was not changed. We confirmed that no saturation effect of the broadband amplifier occurred. While the origin of the observed behavior in our stacked JAWS circuits is not clear yet, it helps us to operate larger arrays with more junctions. Increasing the output voltage is presently the major interest of our development of this technology.

IV. Conclusion

This paper describes the fabrication technology for up to 5-stacked Josephson arrays with a total number of 16 layers within the process for the application in JAWS. A low parameter spread, and good yield was achieved by modification of a window process at crucial points. Among others a CMP and ALD step were introduced to avoid superconducting shorts at the steep edges of the junction multilayers.

The Shapiro step generation of the JAWS circuits was investigated for different pulse repetition frequencies, number of junctions per array and number of junctions per stack. We showed that the pulse amplitude per junction required for the generation of the first Shapiro step decreases nearly linear with the square of the number of junctions for increasing the number of junctions per stack.

This feature is well suitable to easily increase the array size without the need of applying higher power into the circuits. Larger arrays enable larger output voltage which is the main goal in the further development of the JAWS circuits. The origin for this observed behavior might be a self-synchronization of the junctions in these one-dimensional arrays. There is no clear evidence in the data presently available.

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