Investigation of Broadband Wilkinson Power Dividers for Pulse-Driven Josephson Voltage Standards

Hao Tian, Oliver Kieler, Ralf Behr, Rolf-Werner Gerdau, Karsten Kuhlmann, and Johannes Kohlmann

***Abstract*—This paper describes recent developments for increasing the output voltage of the Josephson Arbitrary Waveform Synthesizer (JAWS) at PTB. For this purpose, we developed modified broadband Wilkinson power dividers, which enable the operation of two or four Josephson junction series arrays per RF channel of the pulse pattern generator and thus the generation of increased output voltages. In detail, we designed and investigated two different Wilkinson power dividers: the one-stage three-section Wilkinson power divider with extended bandwidth and the two-stage single-section Wilkinson divider with more outputs to combine four parallel series arrays. They were both integrated with triple-stacked Josephson junction series arrays. Additionally, a new modulator pulse amplifier was introduced into the JAWS set-up to provide sufficient power for all the junction arrays. Our measurement results show that spectrally pure sinusoidal waveforms were successfully generated with both types of power dividers. With the one-stage three-section Wilkinson power divider, we obtained RMS voltages of nearly 53 mV at a clock-frequency of 15 GHz combined with a test array of 3000 Josephson junctions. As for the two-stage single-section Wilkinson power divider combined with a test array of 6000 Josephson junctions, we synthesized RMS output voltages of about 105 mV. These test results show a promising prospect for quantum voltage standard applications.**

***Index Terms*—Broadband Wilkinson power divider, Josephson Arbitrary Waveform Synthesizer, triple-stacked SNS Josephson junctions, characteristic impedance.**

I. Introduction

THE pulse-driven Josephson Voltage Standard or Josephson Arbitrary Waveform Synthesizer (JAWS) enables the generation of quantized AC voltages with high accuracy. It is already widely used in different metrology applications, such as: AC calibrations [1], Josephson impedance bridges [2], [3] and Johnson noise thermometry [4], [5]. Series arrays of overdamped SNS Josephson junctions (JJs, S: superconductor, N: normal metal) are driven by a high-speed digital sequence of bipolar current pulses from a commercial pulse-pattern generator (PPG). The desired waveform is encoded by $\Sigma\Delta$ analog-to-digital conversion in the pulse sequence and stored in the memory of the PPG. Each digital pulse transfers n flux quanta $\Phi_0 = h/2e$ (h is Planck's constant and e is the elementary charge) through each junction of the series arrays operated at 4 K, which results in a quantized AC voltage. The JAWS makes the synthesis of spectrally pure AC voltages from DC up to MHz and above possible [6], [7]. A broadband behavior of all high-frequency components is required because of the pulse drive. According to the Josephson equation, the root-mean-square (RMS) AC output voltage and its frequency is generally given by:

$$V_{\mathrm{rms}} = \left(\frac{1}{\sqrt{2}}\right) A_{\Sigma\Delta} mn\Phi_0 f_{\mathrm{clock-PPG}} \tag{1}$$

$$f_{\mathrm{AC}} = T_{\Sigma\Delta}\, f_{\mathrm{clock-PPG}}/L_{\Sigma\Delta} \tag{2}$$

where m is the number of JJs, n is the order of the Shapiro-step (typically: $n = 1$), $f_{\text{clock-PPG}}$ is the clock frequency of the PPG (for return-to-zero pulses), and $A_{\Sigma\Delta}$ is the code amplitude factor ($0 < A_{\Sigma\Delta} < 1$, i.e., density of pulses in the code). The frequency of the AC output voltage is dependent on the code length $L_{\Sigma\Delta}$ and the number of periods of the code pattern $T_{\Sigma\Delta}$.

So far, the output voltage of the JAWS at PTB is still limited, as it is difficult for all the combined Josephson junction arrays to show common Shapiro steps with large code amplitudes at the high available pulse repetition frequencies. Previously, we connected 16 JJ arrays (arranged on eight 10 mm $\times$ 10 mm JAWS chips) with 162000 junctions in total to 16 high-speed PPG channels with RF cables, which transfer the short current pulses from the PPG at room temperature to the JAWS chip at 4 K. RMS output voltages of 2.25 V were generated with this complex measurement setup [8]. Recently, NIST has achieved a 4 V JAWS by adding a two-stage on-chip Wilkinson power divider using lumped elements into JAWS arrays [10], [11]. Applying such broadband on-chip power dividers to JAWS arrays has several advantages. Due to its compact on-chip structure, it can be integrated together with the Josephson junction series arrays on one chip and fabricated in a common process. In addition, the experimental setup is simplified and even the costs of the PPG are lowered by reducing the number of electrical pulse-channels at room temperature. Very recently, we have successfully developed and integrated a two-stage serial-parallel power divider and one-stage single-section Wilkinson power divider [12] into JAWS test circuits. To increase the operation of a larger number of JJs and thus increase the output voltage generated by a single channel of the PPG, we developed two modified designs of broadband Wilkinson power dividers. This paper describes the design of these dividers (Section II), their fabrication (Section III), and presents and discusses measurement results (Section IV).

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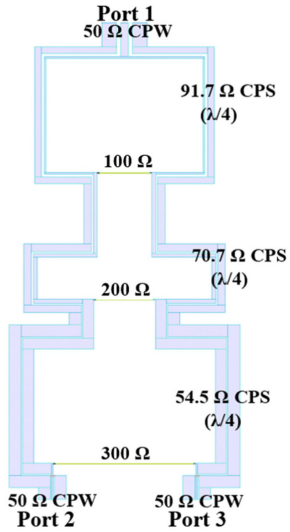

Fig. 1. Structure of a one-stage three-section Wilkinson power divider and its port definition.

II. Design and Simulation

As typical commercial PPGs with data rates around 30 Gbit/s offer pulse repetition frequencies up to 15 GHz, the pulse train of the JAWS contains frequency components from sub-GHz to more than 30 GHz so that the power dividers must be designed rather broadband. In the past, the NIST voltage standard group has designed a compact broadband one-stage Wilkinson power divider using lumped microwave elements [10]. This type of power divider was first successfully implemented in Programmable Josephson Voltage Standard (PJVS) circuits and later also in JAWS circuits [11]. Alternatively, we have developed two new improved broadband on-chip Wilkinson power dividers: one power divider with extended broad bandwidth and the other with more output ports. To increase the bandwidth of the power divider, a one-stage divider with three-sections based on a binomial transformer [13] was developed. To maintain its size and avoid changing its performance, coplanar striplines (CPS) and coplanar waveguides (CPW) with right-angle bending [14], [15] were used (see Fig. 1).

According to the theory and equations of [13], [16], each section has an equal electrical length (¼ λ). The characteristic impedances (Z) of each three sections were calculated to be $Z_1 = 91.7\ \Omega$, $Z_2 = 70.7\ \Omega$, and $Z_3 = 54.5\ \Omega$. A traditional Wilkinson power divider has an isolation resistor between the output ports to prevent that the reflected waves return towards the input port and degrade the performance. To improve the isolation between the two output ports, three resistors were calculated based on the equations from [16] and optimized in the simulation. The goal of increasing the bandwidth results in our design size of about 3900 μm × 1900 μm, which is considerably larger than our previous one-stage single-section Wilkinson divider in [12]. To provide additional chip space for JJs, we extended the JAWS chip length to 15 mm. Different models were numerically simulated in the commercial 3D electromagnetic simulation software CST Microwave Studio.[1]

The 3D structure was simulated using a time-domain solver over a frequency range from 0 to 30 GHz. Table I lists the materials and parameters defined in the simulation. Typically, we used the normal background and magnetic boundaries to model the power dividers, because the superconducting chip is mounted in a cryoperm shield during operation. The mesh cells should be defined correctly to avoid a short circuit between the Nb-base and Nb-wiring layers. Fine mesh cells could cause a long simulation time, but it would give more accurate results. In the excitation settings, waveguide ports of each input and output must be defined to calculate the S-parameter results in CST. Thus, the input port 1 and output ports 2 and 3 of this divider were created. By using the S-parameter sweep, the layout structure was simulated and optimized. From Fig. 2, we can observe that the transmission coefficients are close to the theoretical value of −3 dB and the reflection coefficient S_{11} is smaller than −15 dB from 8 GHz to 25 GHz.

TABLE I
Material Definition and Thickness of Each Layer of the Power Divider in the CST Simulation (PEC: Perfect Electric Conductor). These Parameters Are Very Close to the Fabrication and Measurement Condition At 4 K

Layer	Material	Thickness(μm)
Nb wiring	PEC	0.6
SiO_2 insulator (ε_r=4)	SiO_2	0.6
Nb vias	PEC	0.4
Nb base electrode	PEC	0.16
Si substrate (ε_r=11.9)	Silicon	380

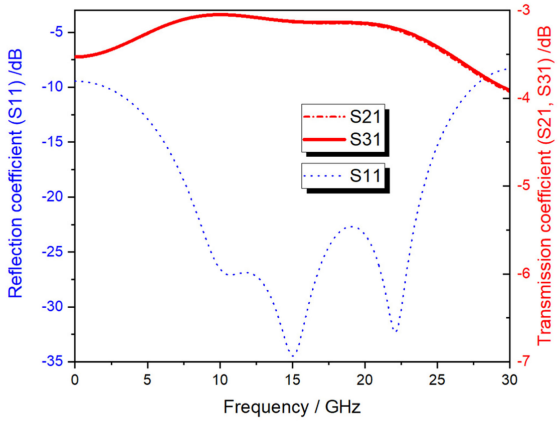

Fig. 2. Simulation results of a one-stage three-section Wilkinson power divider.

The second type of divider is based on our previous one-stage single-section Wilkinson power divider from [12]. We developed this structure further and designed a two-stage single-section Wilkinson power divider with CPS and CPW right-angle bending using ¼ λ resonators [13], [14], as shown in Fig. 3. This improvement enables one RF-channel of PPG to operate four parallel JJ series arrays instead of two. The size of this Wilkinson power divider is about 3000 μm × 3100 μm. In the simulation, most of the parameter settings remain the same as the one-stage three-section Wilkinson divider. In the waveguide set-up dialogue, the input port 1 and output ports 2–5 were defined. The simulation results in Fig. 4 show that the transmission coefficients are approximately to −6 dB with $S_{21} = S_{51}$ and

[1]Commercial equipment is identified in this paper to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by PTB.

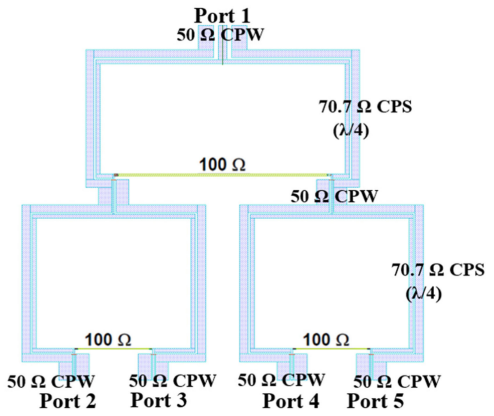

Fig. 3. Structure of a two-stage Wilkinson power divider and its port definition.

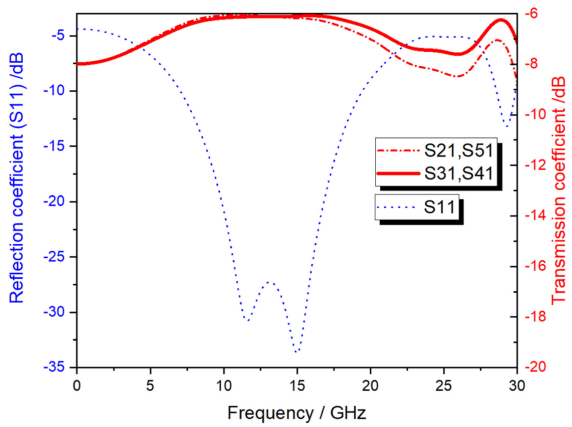

Fig. 4. Simulation results of a two-stage Wilkinson power divider.

$S_{31} = S_{41}$. By observing the simulated phase results of the transmission coefficients, the phase of these parameters at each output is zero and identical for all branches. This indicates that there is no phase shift in the outputs of both Wilkinson dividers. The JJ arrays connected to the outputs of the Wilkinson divider, are arranged in positive and negative polarities to obtain the sum voltage of these JJ arrays at the chip output. The reflection coefficient S_{11} is very small around the center frequency of 15 GHz. Its bandwidth is a bit narrower, because for each stage there is only one single ¼ λ resonator. However, it has a good matching over a wide frequency range from 9 GHz to 18 GHz.

For the on-chip integrated circuits connected to both types of dividers, we applied the bias tee circuit to the JJ arrays to separate the high-frequency signal and the low-frequency signal. A tapered on-chip DC-block parallel plate capacitor was placed on each output of the power dividers. Each series array (500 junction stacks for each parallel arm) was connected with low pass LR filters [19] and terminated by on-chip thin-film resistors. The Josephson stacks were embedded into the center conductor of the CPW. We use the Design Workshop Technology dw-2000 software[1] to draw the entire wafer layout.

III. Chip Fabrication and Experimental Set-Up

The circuits were fabricated in the clean room center of PTB on 3-in. Si wafers. In order to increase the output voltage of our JAWS chips, series arrays of triple-stacked self-shunted Josephson junctions (layer sequence: SNSNSNS) were integrated into the JAWS circuits. Nb_xSi_{1-x} is chosen as the junction barrier to achieve a high characteristic frequency f_c at a low critical current density j_c [17], [18]. The thickness of the Nb_xSi_{1-x} barrier is about 40 nm with a Nb content of about 20% (cf. [9]). By using a window process technology, adjusted for stacked junctions, the JAWS chips were fabricated. For more details of wafer fabrication, please refer to the second section of paper [9].

Just like our previous measurements at 4K [9], we used the PTB's 8-channel JAWS setup, which mainly includes a commercially 8-channel-ternary PPG (Sympuls BPG30G – TERx8[1]), arbitrary waveform generators (Agilent 33522B[1]), a self-made I/V box (to decouple the compensation signal from ground) and a fast digitizer (National Instruments PXI – 5922[1]). The PPG sends a high-speed digital sequence of bipolar return-to-zero pulses to the JAWS chip at 4 K through broadband RF cables at room temperature and semi-rigid RF cables (mounted in a 2-channel liquid-helium cryo-probe) at low temperature. For the JAWS chips with one-stage power divider, each output of the PPG is combined with a broadband pulse amplifier (Picosecond 5882[1]) with a maximum gain of +16 dB. It can provide sufficient power for both arrays. For the test chips with two-stage power divider, a new Optilab MD-50 modulator pulse amplifier[1] with variable gain (max. +30 dB) and fine-tuning function was installed in order to provide sufficient power for all four arrays. The wire-bonded JAWS chip was mounted on a specially made PCB carrier (RO 3006) and operated in a cryoperm shield.

The JJ arrays were operated using the AC-coupled bipolar bias technique [20]. Each JJ array was provided with a three-level digital high-speed signal (-1/0/+1) and a low-speed compensation bias current signal. The low-speed current compensation signals for each separate JJ array were delivered by the arbitrary waveform generators through coaxial low-frequency cables. In the case of the test chip with one-stage three-section Wilkinson power divider, two compensation signals were needed for two series arrays of JJs. Meanwhile, four compensation signals were required for the integrated chip with two-stage Wilkinson power divider connecting with four series arrays of JJs. To obtain the total output voltage, all the JJ arrays were connected in series with on-chip superconducting wires.

IV. Measurement Results

The current-voltage characteristics of the JAWS chips were measured under DC (at 4K) to determine the junction characteristic parameters. Its critical current I_c is around 2.3 mA with a R_n of 3 mΩ. Next, we tested the required broadband frequency behavior of the JAWS circuits under pulse irradiation. By feeding the return-to-zero pulses up to 15 GHz transferred from the PPG to the JJ arrays, the first order Shapiro steps were visible with sufficient step widths for each single array. Fig. 5 illustrates the measurement result of one of the JJ arrays integrated with the one-stage three-section Wilkinson power divider. The current-voltage characteristic was derived (dV/dI) to clearly show the first order Shapiro steps (where $dV/dI = 0$). During the measurements the pulse amplitude was adjusted to keep the zero-order Shapiro step constant at 0.7x I_c. In this figure, the first order Shapiro steps (the white area in the middle) were homogeneous and wide enough over a wide frequency range from 3 GHz to 15 GHz. All other divider layouts of this paper show a comparable performance. The results showed a quite large step width even at low frequencies, where the simulated reflection coefficient is a bit increased. Therefore, so far, the

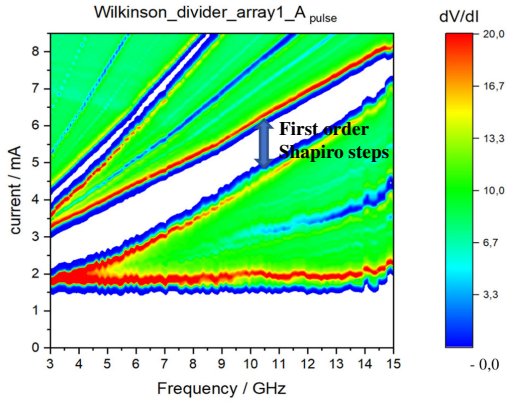

Fig. 5. Frequency dependence of the first-order Shapiro step versus pulse repetition frequency up to 15 GHz for one array containing 1500 JJs integrated with the one-stage three-section Wilkinson power divider. The width of the first-order Shapiro step is large over the wide frequency range at the selected pulse amplitudes.

less ideal reflection coefficient of the Wilkinson divider does not seem to affect the JAWS operation in a crucial way. At frequencies above 14.5 GHz the step size is reduced as a result of insufficient available pulse amplitude. This is indicated by the increased zero-order Shapiro step (above 0.7 x I_c), too.

For creating the codes for pulse operation (synthesizing sinusoidal waveforms), we used a second order $\Sigma\Delta$ modulator with feedback and optimized coefficients with CIFB topology and three digital levels digits (-1/0/1), cf. [21]. During measurements the phase of compensation signal to each parallel array segment should be the same, as there is no phase change in the outputs of Wilkinson power dividers; Otherwise, the synthesized output voltage from each parallel array cannot be observed. The frequency of the arbitrary waveform generator was set to the same as the synthesized signal frequency. The amplitudes of the different signals must be carefully adjusted to make sure that each input pulse transfers exactly one flux quantum through each JJ resulting in a pure frequency spectrum of the synthesized waveform. By adjusting the amplitudes of the pulses, the amplitudes of the compensation signals and even the gain of our new pulse amplifier, the correct operation of the JAWS can be identified by the complete suppression of harmonics shown from the fast digitizer. The digitizer PXI 5922 was operated from batteries. sampling rate was 500 kS/s at input range 10V and no averaging activated. A window function of 7 Term Blackman-Harris was used. Typically, the self-calibration was used, but not before every measurement.

By connecting to the Picosecond pulse amplifier, the JAWS chips with the one-stage three-section Wilkinson power dividers and 3000 JJs is operational up to a maximum clock frequency of 15 GHz (return-to-zero pulses) with a code amplitude of 80%. Fig. 6 shows the frequency spectrum of a synthesized bipolar sine wave with an RMS output voltage of about 53 mV. The current operation margins are 350 μA. the SFDR is about 106 dBc. Combining with the modulator pulse amplifier MD-50, the JAWS chips with the two-stage Wilkinson power divider and 6000 JJs is operated up to clock frequencies of 15 GHz (return-to-zero pulses) with 80% code amplitude. The RMS output voltage of the spectrally pure sinusoidal waveform has increased to ca. 105 mV with a SFDR better than 110 dBc, see Fig. 7. The operation margins determined by observing pure spectra of the synthesized waveform and aligned Shapiro steps shown in the oscilloscope exceed 300 μA in both cases,

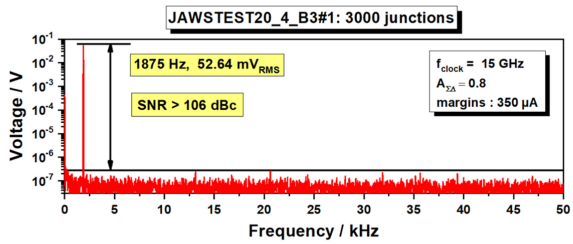

Fig. 6. Frequency spectrum of a synthesized sine wave using a JAWS chip with the one-stage three-section Wilkinson power divider and 3000 Josephson junctions (f AC = 1.875 kHz, Vrms = 53 mV, m = 3000, fclock-PPG = 15 GHz, $A\Sigma\Delta$ = 0.8). The operation margin is about 350 μA.

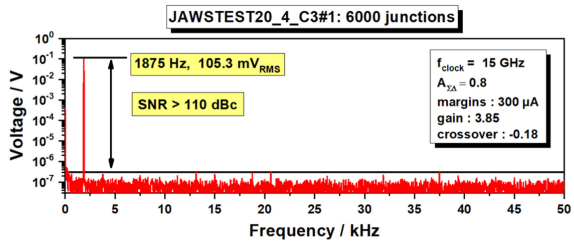

Fig. 7. Frequency spectrum of a synthesized sine wave using a JAWS chip with the two-stage Wilkinson power divider and 6000 Josephson junctions (fAC = 1.875 kHz, Vrms = 105 mV, m = 6000, fclock-PPG = 15 GHz, $A\Sigma\Delta$ = 0.8). The operation margin is about 300 μA.

which clearly demonstrates the operation the of JAWS chips in a quantum locked state. For the frequency spectra, we do not expect distortions up to the MHz range caused by the JAWS system, as research indicated [22].

V. Conclusion

Two types of improved on-chip Wilkinson power dividers with extended bandwidth and with more outputs were newly designed and successfully integrated in JAWS test circuits. JAWS chips with a one-stage three-section Wilkinson divider and 3000 JJs delivered RMS output voltages of 53 mV, while we achieved 105 mV using JAWS chips with a two-stage Wilkinson power divider and 6000 JJs. They can both be operated up to the maximum available clock frequency of 15 GHz with a high code amplitude of 80%. While the Picosecond pulse amplifier provides sufficient power for both arrays integrated with the one-stage Wilkinson power divider, it does not for four JJ arrays integrated with the two-stage Wilkinson power divider, especially at higher clock frequencies. A commercial modulator pulse amplifier (Optilab MD-50) has solved this problem of power deficiency. Both improved Wilkinson power dividers have shown very promising results. In the future, we plan to integrate these dividers with longer series arrays containing a larger number of JJs to further increase the output voltage of a single chip.

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REFERENCES

[1] S. P. Benz *et al.*, "An AC Josephson voltage standard for AC–DC transfer-standard measurements," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 2, pp. 239–243, Apr. 2007.

[2] S. Bauer *et al.*, "A novel two-terminal-pair pulse-driven Josephson impedance bridge linking a 10 nF capacitance standard to the quantized hall resistance," *Metrologia,* vol. 54, no. 2, pp. 152–160, Apr. 2017.

[3] F. Overney *et al.*, "Josephson-based full digital bridge for high-accuracy impedance comparisons," *Metrologia,* vol. 53, no. 4, pp. 1045–1053, Aug. 2016.

[4] N. E. Flowers-Jacobs *et al.*, "A Boltzmann constant determination based on johnson noise thermometry," *Metrologia*, vol. 54, no. 5, pp. 730–737, Oct. 2017.

[5] J. Qu *et al.*, "An improved electronic determination of the Boltzmann constant by johnson noise thermometry," *Metrologia*, vol. 54, no. 4, pp. 549–558, Aug. 2017.

[6] S. P. Benz and C. A. Hamilton, "A pulse-driven programmable Josephson voltage standard," *Appl. Phys. Lett.*, vol. 68, no. 22, pp. 3171–3173, May 1996.

[7] S. P. Benz, C. J. Burroughs, and P. D. Dresselhaus, "Low harmonics distortion in Josephson arbitrary waveform synthesizer," *Appl. Phys. Lett.*, vol. 77, no. 7, pp. 1014–1016, Aug. 2000.

[8] O. Kieler, R. Behr, R. Wendisch, and J. Kohlmann "Arrays of stacked SNS Josephson junctions for pulse-driven Josephson voltage standards," in *Proc. 13th Eur. Conf. Appl. Supercond.*, Sep. 17-21, 2017.

[9] O. Kieler, R. Behr, R. Wendisch, S. Bauer, L. Palafox, and J. Kohlmann, "Towards a 1 v Josephson arbitrary waveform synthesizer," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, Jun. 2015, Art. no. 1400305.

[10] M. M. Elsbury, P. D. Dresselhaus, N. F. Bergren, C. J. Burroughs, S. P. Benz, and Z. Popovic "Broadband lumped-element integrated-way power dividers for voltage standards," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no no. 8, pp. 2055–2063, Aug. 2009.

[11] N. Flowers-Jacobs *et al.*, "Development and applications of a four-volt Josephson arbitrary waveform synthesizer," ISEC 2019, Jul. 2019, USA.

[12] H. Tian *et al.*, "Development of RF-power dividers for the Josephson arbitrary waveform synthesizer," *IEEE Trans. Appl. Supercond.*, vol. 30, no. 5, Aug. 2020, Art. no. 1100105.

[13] D. M. Pozar, *Microwave Engineering*, 4th ed., Hoboken, NJ, Nov. 2011.

[14] K. Goverdhanam, R. N. Simons, and L. P. B. Katehi, " Coplanar stripline components for high-frequency applications," *IEEE Trans. Microw. Theory Techn.*, vol. 45, no. 10, pp. 1725–1729, Oct. 1997.

[15] H. Kim and R. Franklin-Drayton, "Wire-bond free technique for right-angle coplanar waveguide bend structures," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 2, pp. 442–448, Feb. 2009.

[16] U. T. Ahmed and A. M. Abbosh, "Extremely wideband in-phase power divider using modified Wilkinson design," *Microw. Opt. Technol. Lett.*, vol. 57, no. 8, pp. 1799–1802, Aug. 2015.

[17] B. Baek, P. D. Dresselhaus, and S. P. Benz, "Co-sputtered amorphous nb_xsi_{1-x} barriers for Josephson-junction circuits," *IEEE Trans. Appl. Supercond.*, vol. 16, no. 4, pp. 1966–1970, Dec. 2006.

[18] R. Behr, O. F. Kieler, J. Kohlmann, F. Mueller, and L. Palafox, "Development and metrological applications of Josephson arrays at PTB," *Meas. Sci. Technol.*, vol. 23, no. 12, Dec. 2012, Art. no. 124002.

[19] M. Watanabe, P. D. Dresselhaus, and S. P. Benz, "Resonance-free low-pass filters for the AC Josephson voltage standard," *IEEE Trans. Appl. Supercond.*, vol. 16, no. 1, pp. 49–53, Mar. 2006.

[20] S. P. Benz, C. J. Burroughs, and P. D. Dresselhaus, "AC coupling technique for Josephson waveform synthesis," *IEEE Trans. Appl. Supercond.*, vol. 11, no. 1, pp. 612–616, Mar. 2001.

[21] O. F. Kieler, R. Iuzzolino, and J. Kohlmann, "Sub-μm SNS Josephson junction arrays for the Josephson arbitrary waveform synthesizer," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 230–233, Jun. 2009.

[22] H. E. van den Brom, O. F. Kieler, S. Bauer, and E. Houtzager, "AC-DC calibrations with a pulse-driven AC Josephson voltage standard operated in a small cryostat," *IEEE Trans. Instrum. Meas.*, vol. 66, no. 6, pp. 1391–1396, Jun. 2017.