Reversible Fluxon Logic With Optimized CNOT Gate Components

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***Abstract*—Reversible logic gates were previously implemented in superconducting circuits as *adiabatic-reversible* gates, which are powered with a sufficiently slow clock. In contrast, we are studying *ballistic-reversible* gates, where fluxons serve to both encode the information and power the gates. No power is applied to the gate apart from the energy of the input fluxons, and the two possible flux polarities represent the bit states. Undamped long Josephson junctions (LJJs), where fluxons move at practically constant speed from inertia, form the input and output channels of the gates. LJJs are connected in the gates by circuit interfaces, which are designed to allow the ballistic scattering from input to output fluxon states, using the temporary excitation of a localized mode. The duration of the resonant scattering determines the operation time of the gate, approximately a few Josephson plasma periods. Due to the coherent conversions between fluxon and localized modes, the ballistic gates can be very efficient: In our simulations, only a few percent of the fluxon's energy are dissipated in the gate operation. Ballistic-reversible gates can be combined with other nonballistic gate circuits to extend the range of gate functionalities. Here, we describe how the CNOT can be built as a structure that includes the Identity-else-Same-gives-NOT (IDSN) and store-and-launch (SNL) gates. The IDSN is a 2-b ballistic gate, which we describe and analyze in terms of equivalent 1-b circuits. The SNL is a clocking gate, which allows the storage of a bit and the clocked launch of a fluxon on a bit-state-dependent output path. In the CNOT, the SNL gates provide the necessary routing and fluxon synchronization for the input to the IDSN gate.**

***Index Terms*—Ballistic signaling, fluxons, power efficient, reversible computing, superconducting logic circuits.**

I. Introduction

SEMICONDUCTING logic greatly benefits from the dramatic scaling down of transistor gate and interconnect dimensions. Nowadays, however, the benefits from further scaling are nearly exhausted. This has direct implications for the characteristics of logic gates such as a gate's energy cost: One of the bit states is stored as a voltage state on a capacitor, and the stored bit energy scales with the dimensions of the latter. In bit switching, which here amounts to discharging the capacitor, the entire energy of the stored bit state is dissipated. This energy cost is still much higher than the theoretical minimum energy cost, $\log(2)k_BT$, incurred for every bit erasure in irreversible logic gates. In reversible logic gates, on the other hand, no bit erasure takes place. The ensuing absence of a fundamental lower bound of the energy cost motivated Bennett to develop a mathematical model for a reversible computer [1]. Later, Likharev described how classical reversible computing could be achieved in a superconducting circuit, using an external (clock) drive that adiabatically modulates the circuit potential [2]. The energy for bit switching is here proportional to the inverse of the gate time and, thus, can theoretically be lowered indefinitely. More recently, such *adiabatic-reversible* gates have been realized with superconducting technology, in circuits named the quantum flux parametron [3] and the N-SQUID [4].

A physically different approach for energy-conservative computing is based on *ballistic-reversible* gates. In the classic model for these gates [5], logic operations are defined by the scattering of billiard balls. The gates are powered by the inertia of the input states (billiard balls) alone, in contrast to the external drive (clock) power used in the adiabatic model. Ballistic-reversible gates have been studied using optical solitons as information carriers [6], [7]; however, these optical "particles" have been more thoroughly investigated for high-speed and long-distance communication [8].

We have previously proposed reversible fluxon logic (RFL), which is designed to realize ballistic-reversible gates by the scattering of fluxons in special gate circuits [9]. The ballistic gates are unpowered other than the energy of the bit-representing fluxons. Also, the number of fluxons scattered in such a gate is conserved, and their energy is nearly conserved. However, the ballistic gates of RFL are not simply a realization of the billiard-ball model with fluxons, but have two main distinct features: 1) flux-polarity changes determine bit-switching in the gates instead of path changes, and 2) the scattering processes that define the gate operation are resonant. The latter feature makes the gates both energy-efficient and fast, with gate duration set by a few natural JJ oscillation cycles.

Table I compares different logic types in terms of their bit states, stored bit energy, energy cost, and power source. In CMOS (first column), the stored bit energy is given by the charging energy of a capacitance C held at a source voltage V. The capacitor is discharged during bit switching, and the entire

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TABLE I
COMPARISON OF DIFFERENT DIGITAL LOGIC TECHNOLOGIES

	CMOS	Irreversible SFQ	Adiabatic-rev. SFQ	Ballistic-rev. RFL
bit states 1 & 0	voltage state & null	flux state (SFQ) & null	equiv. circulating current states (e.g. CW & CCW)	fluxon polarity ± 1 (topological charge)
stored bit energy	$CV^2/2$ charging energy	$\sim I_c\Phi_0$ JJ-switching energy	$\lesssim I_c\Phi_0$ (time-dependent)	$E_{\rm fl} = 8E_0/\sqrt{1-v^2/c^2}$ fluxon energy
energy cost	$CV^2/2$ per bit switching	$I_c\Phi_0$ per switching JJ	$\ll I_c\Phi_0$	$\ll E_{\rm fl}$
power source	voltage bias V	current bias $I \lesssim I_c$	(multi-phase) current bias	excess bit energy (e.g. kinetic fl. energy)

Note: In contrast to irreversible types (CMOS, irreversible SFQ), in reversible logic types (Adiabatic-rev. and Ballistic rev. SFQ), the energy cost can be small relative to the stored bit energy.

charging energy is lost in the process. Similarly, in irreversible SFQ logic (e.g., RSFQ, ERSFQ, RQL) (second column), one bit state is represented by a single flux quantum (SFQ) stored at an energy $\sim I_c\Phi_0$. This is approximately equal to the energy cost of bit switching, which occurs under a 2π phase slip of a damped JJ with critical current I_c. For the bit states to be distinguishable, they must be separable by a potential barrier that is large compared to the energy of thermal fluctuations k_BT, thus requiring $I_c\Phi_0 \gg k_BT$.

In contrast, reversible logic gates preserve a significant part of the stored bit energy. One approach to this in superconducting circuits are adiabatic-reversible gates (third column), where the bit-defining potential is slowly modulated by a clock. The two bit states are usually represented by circuit states of equal energy. During the transition from one bit state to the other the energy dissipated in the circuit scales inversely with the clock period [2] and, thereby, can be made arbitrarily small.

With RFL (fourth column), we follow the alternative approach of ballistic-reversible gates, which is based on the undamped motion of fluxons in long Josephson junctions (LJJs). A fluxon in an LJJ contains the flux of one SFQ, $\pm\Phi_0$, and according to the sign (polarity), it is designated as either a fluxon or an antifluxon. The two flux polarities are used to represent the two bit states. Both bit states have the same stored bit energy, given here by the fluxon energy $E_{\rm fl}$, which is composed of the rest (potential) energy $8E_0 = 8I_c\Phi_0\lambda_J/(2\pi a)$ and kinetic energy. This stored bit energy can be adjusted for the application, similar to other superconducting SFQ technologies. Ballistic RFL gates make use of the scattering of fluxons at special circuit interfaces between LJJs. The fluxon's rest energy and the fluxon number is conserved in the scattering. Moreover, as our simulations of the classical equations of motion of the RFL gate circuits show, the total fluxon energy is also conserved to a large extent. The remainder is lost to small-amplitude plasma waves generated by the fluxon at the gate.

Ballistic RFL gates developed so far have no internal state memory, in contrast to proposed asynchronous reversible gates [11]–[13]. That is why, ballistic gates for two or more input bits, such as the 2-b NSWAP [9] and Identity-else-Same-gives-NOT (IDSN) gates [10], require a synchronous arrival of the input fluxons. In order to reliably use these gates as part of a larger circuit, we have, therefore, developed a gate for the purpose of clocking and synchronization. According to its operation, it is named a store-and-launch (SNL) gate [10]. The gate stores the bit state of the incoming data fluxon as a static circulating current. Later, upon arrival of a low-energy clock fluxon, the state is launched as a fluxon with the same polarity as the original. The clock fluxon is the sole power source of the launch and is annihilated in the process. Part of its energy goes to the launched data fluxon, which then may have larger energy than the (slowed-down) input data fluxon. The SNL can be designed with a clock fluxon, which has only a fraction of the data fluxon's energy, and is, therefore, energy efficient by irreversible logic standards. Moreover, with SNL-clock fluxons as the main energy cost, while ballistic gates and LJJs as transmission lines are unpowered, RFL can avoid problems associated with the dc-biasing of JJs in irreversible SFQ logic [14]–[16].

The launch direction of the SNL is bit-state dependent: bit state 0 (fluxon) and bit state 1 (antifluxon) each have their designated output LJJ. This bit-state dependent routing adds an important resource to RFL logic. It allows us to combine basic RFL components in a way that achieves a complex reversible gate operation, which for symmetry reasons cannot be achieved directly with a single ballistic RFL gate. As an example, we had proposed in [10] to implement a CNOT with a structure that is composed of several ballistic gates (including two IDSN gates) together with two SNL gates.

RFL was originally introduced in [9], where we studied fundamental ballistic gates of RFL through numerical simulation and also analytically with a collective coordinate model. In [10], we had extended the scope of RFL, by introducing concepts of the clocking gate SNL, the ballistic IDSN and the composite CNOT. These gates were, however, not studied in great detail and had not been optimized. Here, we provide the missing details and extend the original study: For the IDSN, we provide optimized parameters and margins, and also introduce an analytic model from which we derive parameter equivalences with 1-b gates. We now introduce and study an SNL with two-input LJJs, as is required in the CNOT application while initially only a one-input SNL version had been described [10].

This article is organized as follows: First, we summarize, in Section II, the operation of ballistic RFL gates and explain the resonant scattering dynamics in detail using the example of the simulated 1-b NOT gate, see Section II-A. The optimized 2-b IDSN gate is described in Section III, where we show the simulated dynamics and analytically map the gate to equivalent 1-b gates. Section IV presents the two-input SNL gate with details of the dynamics and a comparison to an earlier one-input SNL [10]. In Section V, we describe the CNOT gate, which is composed of the gates from the preceding sections.

II. SHORT SUMMARY OF BALLISTIC RFL GATES

LJJs are key structures in RFL. We design RFL circuits with discrete forms of LJJs, where an array of identical Josephson junctions (JJs) is connected by two inductor "rails." In Fig. 1(a), two such discrete LJJs form the left and right parts of the circuit. The JJs have capacitance and critical current of (C_J, I_c), and each unit cell of length a has the inductance

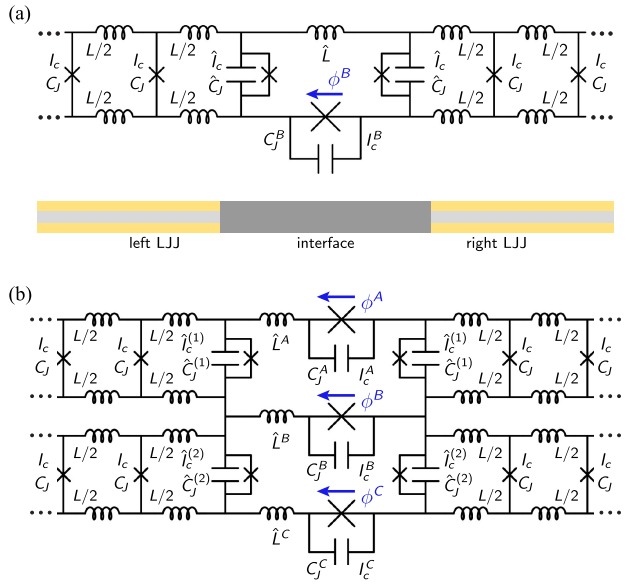


Fig. 1. RFL gate structures: (a) Schematic for a ballistic 1-b gate, consisting of two LJJs connected by an interface cell with three capacitance-shunted JJs: the left and right 'termination JJs' with $(\hat{C}_J, \hat{I}_c)$, and the 'rail JJ' with (C_J^B, I_c^B). For a ballistic RFL gate, parameters have to be set such that an incident free fluxon undergoes the desired type of forward-scattering from one LJJ to the other. These resonant dynamics are enabled by specific large values of the shunt capacitances $C_J^B, \hat{C}_J$. The sketch under the schematic illustrates the essential structure of the gates; dynamics in the discrete LJJs is similar to the continuous limit. (b) Schematic for ballistic 2-b gates consisting of two-input and two-output LJJs, and a circuit interface with 7 JJs. These allow forward-scattering of fluxons similar to 1-b ballistic gates, but now also with input-dependent (conditional) polarity changes. In efficient ballistic gates the interface's rail inductance(s) are small, $\hat{L} \ll L$, and this prevents the interface cell(s) from storing a flux quantum.

L. The circuit parameters set the Josephson plasma frequency $\omega_J = 2\pi\nu_J = \sqrt{2\pi I_c/(\Phi_0 C_J)}$, and the Josephson penetration depth, $\lambda_J = a\sqrt{\Phi_0/(2\pi L I_c)}$. The latter determines the length scale of phase gradients in the (discrete) LJJ, such as the width of a fluxon or edge states at the LJJ boundaries.

A fluxon in an LJJ is described by the soliton solution $\phi(x,t) = 4\arctan(\exp(\mp(x-vt)/\sqrt{1-v^2/c^2}))$ of the sine-Gordon equation $\partial_{tt}\phi - c^2\partial_{xx}\phi + \omega_J^2 \sin\phi = 0$ for the superconducting phase field $\phi(x)$. According to that solution, the fluxon behaves like a relativistic particle, moving with constant speed $v \le c$ below the upper velocity bound $c = \omega_J \lambda_J$. The energy of the moving fluxon is increased by a factor

$$E_{\mathrm{fl}}(v)/E_{\mathrm{fl}}(0) = \left(1 - (v/c)^2\right)^{-1/2} \tag{1}$$

relative to its rest energy $E_{\mathrm{fl}}(v=0) = 8E_0$, where $E_0 = I_c\Phi_0\lambda_J/(2\pi a)$.

In a discrete LJJ, the discreteness introduces a damping of the fluxon motion, compared to its motion at constant speed in a continuous LJJ. The strength of this perturbation is determined by the relative discreteness a/λ_J. In our circuit simulations, we choose $a/\lambda_J \simeq 1/3$ to be sufficiently small, such that the loss in speed (and energy) is negligible even when the fluxon moves over hundreds of unit cells.

The bit-switching mechanism of the logic requires a method to invert the fluxon polarity. The 1-b NOT gate, as the fundamental realization for bit-switching, is implemented in a circuit as shown in Fig. 1(a), where input and output LJJs are connected by a circuit interface. The designation as input and output LJJs can, in principle, be reversed since the circuit has left–right symmetry. The interface consists of at least three capacitively shunted JJs (CSJJs). Each LJJ is terminated by a CSJJ with parameters $(\hat{C}_J, \hat{I}_c)$ between its inductor rails, and we call these the left and right "termination-JJs" of the interface. The two rails of one LJJ are connected to those of the other, where one connection (shown between the lower rails) is formed by a CSJJ with parameters (C_J^B, I_c^B), and we call it the "rail-JJ" of the interface. The other connection (shown between the upper rails) is made with an inductor $\hat{L}$ that is typically small ($\hat{L} \ll L$) and the interface cell, thus, cannot store a flux quantum.

Depending on the interface parameters, such a circuit interface has been found to enable forward-scattering of an incoming fluxon from one LJJ to the other [9]. In these processes, the incident fluxon breaks at the interface into two parts, where its characteristic phase and current distributions become discontinuous. Its energy is transferred to excitations of the interface JJs and evanescent fields in the LJJs close to the interface. These localized excitations undergo a short coherent oscillation before a new fluxon forms in the other LJJ. Importantly, for certain interface parameters, the polarity of the newly created fluxon is opposite to that of the original fluxon and, thus, realizes a NOT gate. We note that polarity inversion is not possible for a fluxon within the bulk of a planar LJJ due to its topological nature (other than by a wiring crossover for a half-twist in an LJJ, not used here). In contrast, in the NOT gate, the polarity inversion is possible due to the interface's rail-JJ, which opens the otherwise flux-impermeable LJJ rails and allows for a large difference of 4π building up between the left and right termination-JJ phases. This phase change is dissipationless, unlike phase switching in the resistively shunted JJs of SFQ logic gates or in overdriven unshunted JJs. In Section II-A, we describe the NOT gate operation in more detail.

For the purpose of ballistic gates, the parameters of the interface cell are set such that the fluxon scattering is resonant. By resonance, we mean that the energy transfer from the moving fluxon to the localized excitation and again to a moving fluxon happens coherently. Considering the highly nonlinear nature of the fluxons and other involved modes, no obvious and unambiguous resonance criterion in the sense of matching frequencies exists. At resonance, the gate is particularly efficient since energy loss through plasma waves generated at the interface is minimized. Correspondingly, the energy-efficiency of the gate (ratio of fluxon energy before and after the scattering) assumes a local maximum with respect to most interface parameters, cf. [9, Fig. 9]. For example, a resonant NOT gate requires relatively large shunt capacitances of the three interface JJs [9], [17].

Different types of scattering resonances can be observed at different points in parameter space, each within a finite (but wide) range around an efficiency maximum. They can be classified according to characteristics such as 1) the number and duration of the interface oscillation cycles (comparable to the "bounces" in LJJs with point defects [18]). Furthermore, 2) a resonance may preserve or invert the polarity of the incoming

fluxon, and 3) the new fluxon may be created in the output LJJ (forward-scattering) or in the input LJJ (backward-scattering). For a given set of interface parameters, the resonant scattering typically is observed within a range of fluxon input velocities v. In the adiabatic limit, i.e., for very small input velocity, $v \ll c$, the flux quantum will be lost in the gate. In contrast, in adiabatic-reversible logic, the clock can be slowed in principle to an arbitrarily small frequency.

Similar to the 1-b NOT gate, a ballistic 1-b Identity (ID) gate can be implemented with the structure in Fig. 1(a), using a specific set of interface parameters. The fluxon induces at the ID gate interface a different resonance compared to the NOT gate resonance, and from it, a new fluxon is created in the output LJJ, which has the same polarity as the input fluxon. This resonant ID gate can, in principle, be parametrically tuned into a NOT gate, since both fundamental 1-b gates are based on the same circuit-interface structure. This is an advantage over a trivial ID operation in form of nonresonant transmission, e.g., through a regular LJJ cell, and informs the construction of more complex gates from the fundamental 1-b gates. We have, for example, designed ballistic 2-b gates based on the circuit structure shown in Fig. 1(b). It has two-input and two-output LJJs connected by a circuit interface with seven CSJJs. Interface parameters are set such that a fluxon coming in on the upper (lower) input LJJ is scattered forward to the upper (lower) output LJJ. In these 2-b gates, the polarity inversion is conditional: Depending on the interface parameters and on the presence and polarity of a synchronized input fluxon on the other LJJ, the action on the bit is polarity-preserving or polarity-inverting. So far, ballistic RFL designs exist for a 2-b NSWAP=NOT(SWAP) logic gate [9], and for an IDSN logic gate [10]. An updated version of the latter is discussed in detail in Section III.

The dynamics of the JJ phases in a given circuit is obtained through numerical integration of the classical circuit equations of motion, with fluxon(s) moving in the input LJJ(s) taken as initial conditions. For a desired gate operation, we identify suitable interface parameters by optimization of the gate efficiency. Parameter variations around these optimized values generally show relatively robust parameter margins [9], suggesting the feasibility of the gates in fabrication and operation. If the interface parameters are chosen far away from the parameter range set by these margins, the resulting dynamics, in general, are not useful as an RFL gate, such as fluxon annihilation or reflection. In certain limits far away from our gate margins, the fluxon dynamics at the interface is comparable to other well-studied fluxon phenomena, e.g., scattering of a fluxon at an LJJ end with specific boundary condition [19], [20], or scattering within the LJJ at a perturbation potential. The latter, which includes the resonant chaotic scattering at point defects [18], [21] and fluxon scattering at a qubit-induced potential [22], do not allow polarity change. The interface scattering used in RFL gates is nonperturbative, since the fluxon breaks up and loses its identity at the interface.

A. Dynamics in the 1-b NOT Gate

Fig. 2 shows the dynamics of a ballistic NOT gate in the circuit of Fig. 1(a). We obtain the evolution of the JJ phases from the simulation of the circuit equations of motion. The simulation starts from an initial phase distribution corresponding to a fluxon that moves in the left LJJ ($x < 0$) with velocity $\dot{x} = v$ toward the interface at $x = 0$. (Note that other simulations include also a circuit structure for launching fluxons [9].) The JJ phases ϕ_n in the left and right LJJ, including those of the left and right termination JJs of the interface, are shown in the panels of Fig. 2(a), each taken at a particular time of the dynamics. Fig. 2(b) shows the evolution of $\phi_n(t)$ as a continuous function of time; the colormap emphasizes phases close to the values $2(k+1)\pi$ ($k \in \mathbb{Z}$) of largest Josephson energy. Fig. 2(c) shows the evolution of the interface's rail-JJ phase ϕ^B.

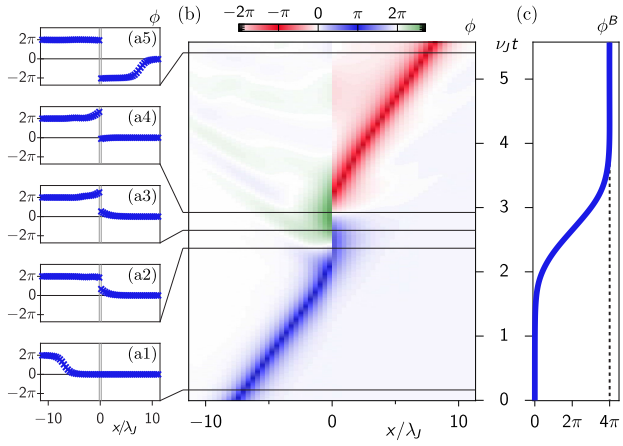


Fig. 2. RFL NOT gate dynamics. (a1)–(a5) JJ-phases ϕ_n left and right of the interface versus position, at fixed times of the dynamics, reproduced with parameters from [9]: (a1) Input fluxon moving in left LJJ toward interface; (a2)–(a4) intermediate excitation of left and right interface JJs and evanescent phase fields left and right of the interface; (a5) antifluxon emitted from the interface into the right LJJ. (b) Dynamics of JJ phases ϕ_n versus time. The colormap, which emphasizes phases of high Josephson energy around values $2(k+1)\pi$ ($k \in \mathbb{Z}$), shows the center of the free fluxon (antifluxon) moving toward (away from) the interface at constant velocity before (after) the scattering, and the localized oscillation of the evanescent fields that are resonantly excited by the fluxon. (c) Evolution of phase $\phi^B(t)$ of the interface's rail-JJ, showing an adiabatic 4π-change.

In panel (a1), one sees, in the left LJJ, the still undisturbed fluxon, with characteristic phase profile varying in position from 2π to 0 (for fluxon with positive polarity). Panels (a2)–(a4) illustrate the situation after the fluxon has broken up at the interface and induced an excitation of the interface JJs and adjacent JJs. This excitation has the form of exponentially localized edge states in the two LJJs. When the fluxon breaks up [at a time just before that shown in panel (a2)], the phase profiles left and right of the interface have negative, fluxonlike slopes: From 2π in the fluxon's wake in the left LJJ at $x \ll -\lambda_J$ to $\phi(x \lesssim 0) \approx \pi$ near the interface, and from $\phi(x \gtrsim 0) \approx \pi$ near the interface to 0 in the right LJJ at $x \gg \lambda_J$. These phase distributions then undergo coherent amplitude swings, stills of which are shown in panels (a2)–(a4). The oscillations left and right of the interface occur around 2π and 0, respectively, with maximum amplitudes of $\approx \pi$, and with evolving phase difference between the two. During the oscillations, the LJJ phase distributions close to the interface change their character from fluxonlike (negative slope) to antifluxonlike (positive slope). When the slope to the right of the interface turns from negative in panel (a3) to positive in panel (a4), this may be seen as the starting point for the formation of

TABLE II
LOGIC TABLE FOR THE IDSN GATE, WHOSE ALLOWED INPUT STATES ARE NULL INPUT (–), A SINGLE FLUXON (0), OR ANTIFLUXON (1) ON EITHER OF THE TWO-INPUT LJJS (S_1 OR S_2), OR TWO SYNCHRONIZED FLUXONS OF THE SAME POLARITY COMING IN ON BOTH LJJS (S_1 AND S_2)

Input		Output	
LJJ S_1	LJJ S_2	LJJ S_1'	LJJ S_2'
–	–	–	–
0	–	0	–
–	0	–	0
1	–	1	–
–	1	–	1
0	0	1	1
1	1	0	0

The IDSN gate circuit is shown in Fig. 3(a). An incoming fluxon on input LJJ S_1 (S_2) will be scattered to output LJJ S_1' (S_2'), assuming the fluxon input velocity and synchronization lie in the acceptable range.

an antifluxon. The phase distribution in the right LJJ develops into that of an antifluxon, varying from -2π at the interface to 0 in the bulk of the right LJJ. All along, the growing phase gap between right and left LJJ is compensated by the likewise growing phase of the interface's rail-JJ, $\phi^B \approx \phi(x \gtrsim 0) - \phi(x \lesssim 0)$, cf. Fig. 2(c), while the small inductance $\hat{L} \ll L$ in the interface cell stores negligible flux. By the time when ϕ^B has grown close to 4π, the antifluxon is released from the interface into the right LJJ where it moves freely, as shown in panel (a5). The 4π-phase change is adiabatic, happening on the time scale of the Josephson period, $1/\nu_J$, in contrast to the rapid (and dissipative) 2π-phase slips in RSFQ logic.

In Fig. 2(b), one can see the evanescent phase fields excited around the interface during the resonant process. The coherent oscillation of these edge states is characteristic for the resonant fluxon scattering used in RFL. A related "bounce"-resonance can be observed in an LJJ when a fluxon is scattered at a point defect such as a locally modified critical current [18]. Fig. 2(b) also shows that small plasma waves are emitted into the LJJs during and after the scattering process. They carry away a fraction of the initial fluxon energy. However, as indicated by the indistinguishable trajectory slopes of the incoming fluxon and outgoing antifluxon, this is only a minor loss: From fluxon fits before and after the scattering, we see that 97% of the fluxon energy is conserved.

III. IDSN GATE

We had recently introduced a type of ballistic 2-b gate, which is named IDSN after the operations it performs: A single input fluxon undergoes an ID operation, and two synchronized fluxons of the same polarity each undergo a NOT operation [10]. Table II summarizes the logic action of the IDSN gate. Note that the IDSN is a conditionally reversible gate [23], [24], where only certain 2-b inputs are allowed, whereas all 1-b inputs are allowed. Like the previously introduced NSWAP gate, the IDSN gate is implemented by the resonant fluxon scattering at a gate interface of the type shown in Fig. 1(b). The circuit has left–right symmetry across the interface, as well as vertical symmetry about the B-rail, i.e., $\hat{L}^C = \hat{L}^A$, $C_J^C = C_J^A$, $I_c^C = I_c^A$, and $C_J^{(2)} = C_J^{(1)}$, $I_c^{(2)} = I_c^{(1)}$, see also Fig. 3(a). Within certain ranges of the interface parameters, this structure supports an IDSN gate. Similar to other ballistic gates that make use of the resonant forward-scattering, it requires specific, large (shunt) capacitances $\gg C_J$ for the interface JJs. Unlike the NOT, ID, and NSWAP ballistic gates, the IDSN uses interface JJs that also have relatively large critical currents $> I_c$. For example, the particular IDSN gate in [10] has parameter values $(C_J^A, I_c^A) = (9C_J, 2.4I_c)$, $(C_J^B, I_c^B) = (21.3C_J, 4.9I_c)$, and $(\hat{C}_J, \hat{I}_c) = (6.0C_J, 1.2I_c)$, whereas the geometric inductances in the interface are negligible, $\hat{L}^A = \hat{L}^B \ll L$. Here, we present a new IDSN gate with nonnegligible interface inductance $\hat{L}^B$. The parameters are given in the caption of Fig. 3. The new IDSN differs in the details of the resonance dynamics from the one discussed in [10]; moreover, it has improved margins compared with the latter.

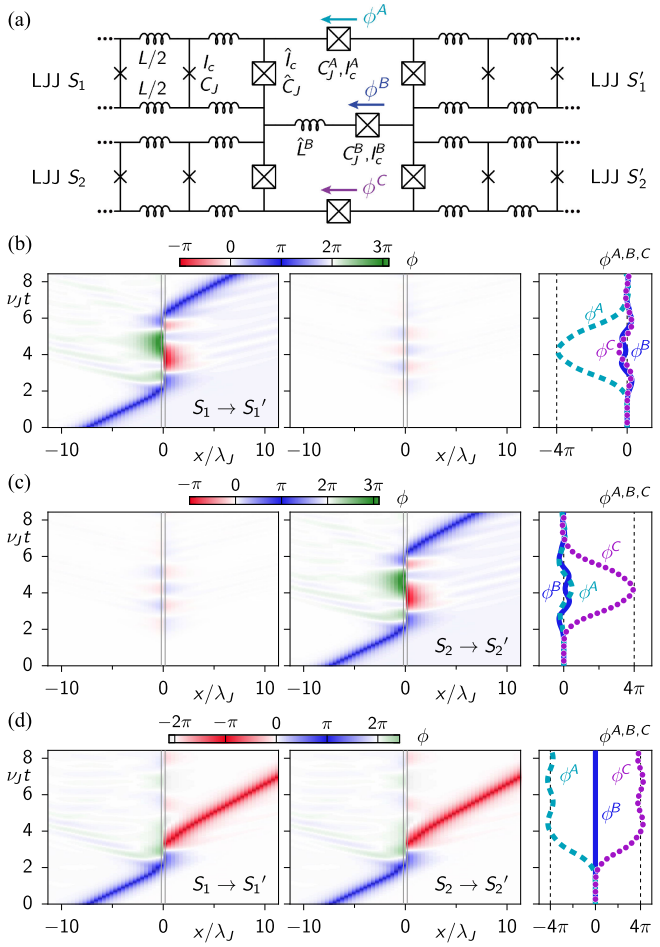


Fig. 3. IDSN gate circuit and dynamics. (a) Circuit for ballistic IDSN gate. The circuit has both left–right symmetry and bottom–top symmetry (symmetry-related circuit elements are not labeled). The interface JJs are shown with large symbols, which include large shunt-capacitances. (b)–(d) IDSN dynamics for different fluxon inputs. The first two panels of each row show the JJ-phases ϕ_n as colormaps, one for the upper LJJs, $S_1(x<0)$ and $S_1'(x>0)$, and one for the lower LJJs, LJJ $S_2(x<0)$ and $S_2'(x>0)$. The third panel in each row shows phases ϕ^A, ϕ^B, ϕ^C of interface rail-JJs. (b) and (c) Single-input fluxon, which enters on (b) LJJ S_1 and (c) LJJ S_2, respectively, and scatters forward with preserved polarity. (d) Two synchronized fluxons of the same polarity, each entering on one of LJJs S_1 and S_2, each scatter forward to opposite polarity state. The interface parameters are $C_J^A/C_J = 15.0$, $I_c^A/I_c = 1.5$, $C_J^B/C_J = 16.7$, $I_c^B/I_c = 6.9$, $\hat{C}_J/C_J = 5.8$, $\hat{I}_c/I_c = 1.5$, and $\hat{L}^B/L = 0.5$.

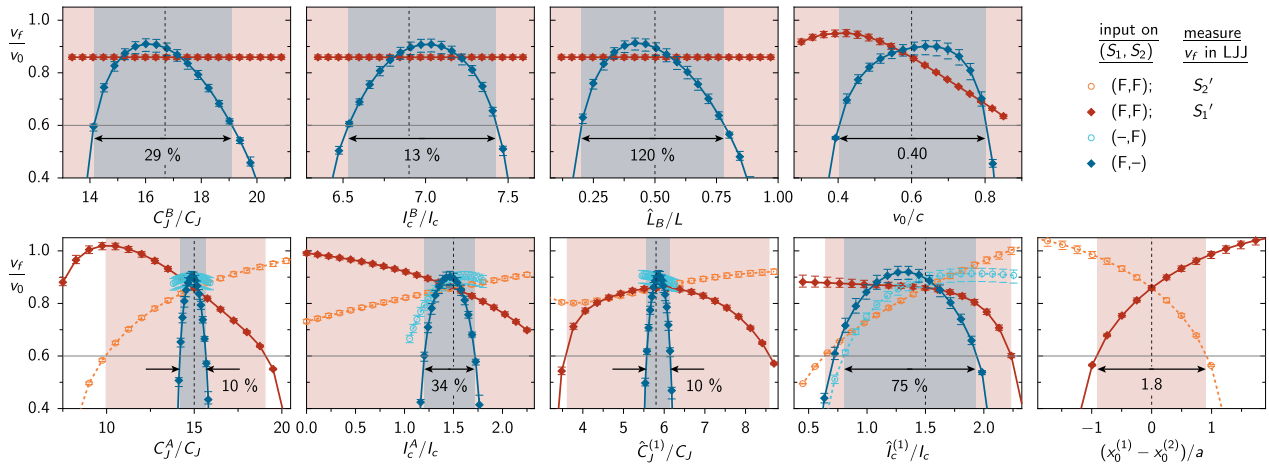


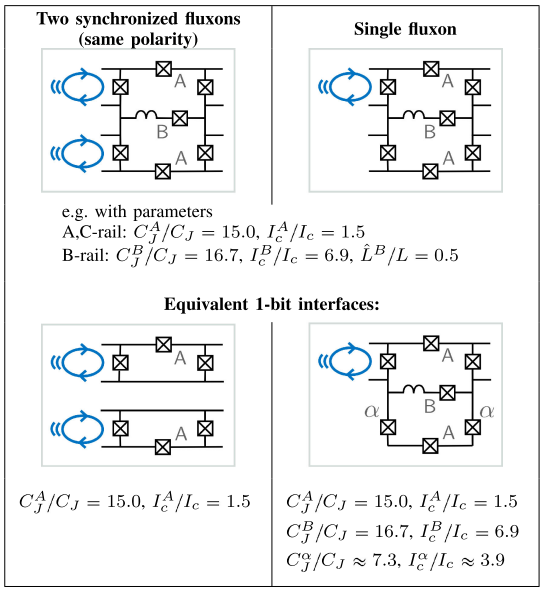
Fig. 4. IDSN gate robustness and margins: Ratio of gate output to input velocity v_f/v_0 as function of interface parameters $C_J^A, C_J^B, \hat{C}_J^{(1)}, I_c^A, I_c^B, \hat{I}_c^{(1)}, \hat{L}^B$ [cf. Fig. 1(b)], initial velocity $v_0 = v_0^{(1)} = v_0^{(2)}$, and fluxon separation $\Delta x = x_0^{(1)} - x_0^{(2)}$. In each panel, only a single parameter (interface parameter or initial state parameter v_0 or Δx) is varied, whereas all others are kept constant at the value indicated by the vertical dashed lines (cf. caption of Fig. 3). The output velocity v_f may depend on the input type: (F,–) and (–,F) for single-fluxon input on LJJ S_1 (◆) and S_2 (○), respectively, and (F,F) for two-fluxon input, where v_f refers to either the output fluxon on LJJ S_1' (◆) or on LJJ S_2' (○). In the first row of panels, the variation of parameters $C_J^B, I_c^B, \hat{L}^B$ preserves the vertical symmetry of the structure, as does the simultaneous variation of input velocities of both fluxons v_0. Thus, after the input of two fluxons (F,F), the output fluxons on both LJJs S_1' and S_2' have identical output velocity v_f. Also, forward-scattering of a single fluxon on either of S_1 or S_2 leads to identical v_f. In contrast, in the second row of panels, the variation of interface parameters $C_J^A, I_c^A, \hat{C}_J^{(1)}, \hat{I}_c^{(1)}$ breaks vertical symmetry, and thus, the final velocities v_f of the two forward-scattered fluxons differ. Similarly, a finite separation $\Delta x \neq 0$ of the two-input fluxons in input type (F,F) breaks the symmetry of the initial state, and thus, v_f of the two scattered fluxons differ. Error bars indicate the amplitudes of velocity oscillations after scattering. Shaded regions illustrate the ranges where $v_f/v_0 > 0.6$ is fulfilled for two-fluxon input (red) or single-fluxon input (blue), corresponding to fluxon energy conservation $E_{\mathrm{fl},f}/E_{\mathrm{fl},0} > 86\%$. Arrows indicate the effective margins resulting from this criterion. The admissible range for initial velocities is $0.4c \leq v_0 \leq 0.8c$, and the two fluxons in the (F,F)-type may be initially separated by up to ± 0.9 cell, i.e., the fluxons need to be synchronized with a delay time less than $0.09/\nu_J$.

The fluxon dynamics for this new IDSN is shown in Fig. 3(b)–(d). Fig. 3(b) and (c) illustrates the dynamics for a single fluxon, which is coming in on input LJJ S_1 and input LJJ S_2, respectively. The dynamics for these two initial conditions is of course equivalent, owing to the vertical symmetry of the structure. In either case, the incoming fluxon creates a short resonant excitation centered at the interface from which a new fluxon is created in the corresponding output LJJ, S_1' and S_2', respectively. The output fluxon has the same polarity as the input fluxon, similar to the 1-b ID gate. However, the resonance here consists of a longer oscillation cycle at the interface than in the optimized 1-b ID gate, cf. [9, Fig. 2]. The different dynamics in the IDSN can be attributed to the additional excitation of interface rail-JJs and evanescent field excitation in the nonfluxon carrying LJJs, see analysis in Section III-A.

Fig. 3(d) shows the scattering dynamics for two synchronized fluxons, each coming in on its own input LJJ. Here, the dynamics in the upper and lower parts of the structure is dynamically decoupled, because the current across the rail-JJ with phase ϕ^B cancels due to symmetry reasons. This is similar to the NSWAP gate with input fluxons of equal polarity, and as in that case, the fluxons here also undergo NOT dynamics, i.e., they are forward-scattered to the output LJJs with inverted polarity. Owing to the decoupled dynamics in upper half and lower half, the resonance here is essentially identical to that of the 1-b NOT gate, with, however, slightly different gate duration and efficiency. These differences are due to the deviation from the optimized parameters of the 1-b NOT, required here (as in 2-b gates in general) for a compromise with the other IDSN operations.

Fig. 4 summarizes the robustness characteristics of the IDSN gate with respect to variations of the interface parameters and the initial state. The individual panels of Fig. 4 show the ratio v_f/v_0 of output-to-input velocity of the forward-scattered fluxon(s) versus the varied parameter, both for the single-fluxon processes (blue and light blue) and the two-fluxon processes (red and orange). Each panel shows the effect of one parameter variation around the optimized value (given in the caption of Fig. 3 and indicated here by vertical dashed lines), whereas all other parameters of the system are held fixed. The parameter variations shown in the first row of panels preserve the top–bottom symmetry of the interface (variation of $C_J^B, I_c^B, \hat{L}^B$) or of the initial condition in the LJJs (equal variation of the fluxon input velocities in both LJJs, $v_0 = v_0^{(1)} = v_0^{(2)}$). Accordingly, the fluxon output velocity v_f is here independent of whether the fluxon is sent in on input LJJ S_1 or S_2 in the single-fluxon process. Similarly, v_f is equal in both output LJJs S_1' and S_2' in the two-fluxon process. That is why only two data lines are seen in the first row of panels. In contrast, the parameter variations shown in the second row of panels break either the top–bottom symmetry of the interface (variation of $C_J^A \neq C_J^C, I_c^A \neq I_c^C, \hat{C}_J^{(1)} \neq \hat{C}_J^{(2)}, \hat{I}_c^{(1)} \neq \hat{I}_c^{(2)}$) or the top–bottom symmetry of the initial condition in the LJJs (variation of relative initial fluxon position $x_0^{(1)} - x_0^{(2)} \neq 0$ for double-fluxon process). In these cases, it, therefore, makes a difference whether a single fluxon is sent in on LJJ S_1 and measured in S_1' (dark blue diamonds) or sent in on LJJ S_2 and measured in

TABLE III
EQUIVALENT CIRCUITS OF IDSN GATE FOR THE TWO FLUXON INPUT CASES



Note: For two synchronized input fluxons (left column), the current on the B-rail of the interface cancels, such that the upper and lower part each are equivalent to a 1-b (ID) gate. For single fluxon coming, e.g., on upper input LJJ (right column), excitations in the lower left and right LJJs together with their parallel interface JJs can be treated perturbatively, allowing to map to JJs α. IDSN parameters are those of Fig. 3. The left and right termination JJs are identical in all interfaces, $\hat{C}_J/C_J = 5.8$ and $\hat{I}_c/I_c = 1.5$.

S_2' (light blue circles). Similarly, in the two-fluxon process the output velocities measured on S_1' (dark red diamonds) and S_2' (orange circles) differ.

The shaded regions in Fig. 4 show the ranges where $v_f/v_0 > 0.6$ is fulfilled, for either two-fluxon input (red shaded) or single-fluxon input (blue shaded), corresponding to an energy efficiency of $E_{\rm fl}(v_f)/E_{\rm fl}(v_0) > 86\%$, cf. (1). The margins resulting from this efficiency criterion are indicated by the arrows. Given current fabrication uncertainties, these margins are sufficiently wide to allow fabrication and testing. The interface parameters that need to be defined most precisely, within 10%, are the capacitances C_J^A, C_J^C of the upper and lower rail-JJs of the interface, and the capacitances $\hat{C}_J^{(1)}, \hat{C}_J^{(2)}$ of the left and right interface JJs. In the two-fluxon process also the input fluxons need to be relatively well synchronized, with a delay time less than $0.09/\nu_J$ at velocity $v_0 = 0.6c$, corresponding to an admissible separation $x_0^{(1)} - x_0^{(2)}$ less than 0.9 cells between the two fluxons. The range of acceptable input velocities, $0.4c \le v_0 \le 0.8c$, is conveniently wide, despite the resonant character of the underlying dynamics. This is different from the chaotic character of resonant scattering at point defects in LJJs [21].

A. Equivalent 1-b Gate Circuits

We now briefly discuss how the IDSN gate operations are dynamically equivalent to certain 1-b interfaces, depending on the input type. The resulting mappings to approximately equivalent 1-b interfaces are summarized in Table III for the IDSN gate of Fig. 3. Similar reductions of the 2-b gate dynamics have been discussed for the input cases of the NSWAP gate [9].

Case (i): When two fluxons of the same polarity approach the *vertically symmetric* 2-b interface at the same time, the currents excited in the rails of the interface form a vertically antisymmetric distribution, and the current through the center rail cancels. The dynamics in the upper and lower part of the interface is then effectively decoupled, and in each of them is equivalent to the dynamics of a 1-b interface as shown in the left column of Table III. The 1-b interface has only a single rail-JJ, which is identical to one of the outer-rail JJs of the 2-b interface, with parameters (C_J^A, I_c^A).

Case (ii): Consider a single fluxon coming in on the upper input LJJ S_1. It dominantly excites the upper part of the IDSN structure, where the upper rail JJ starts winding by more than $\phi^A > \pi/2$. Due to the current conservation on the interface rails, current also flows in the lower part of the interface. The resulting phase fields in the lower LJJs, S_2 and S_2', have the form of exponentially localized edge states, and their amplitude remains small, $|\phi_n| \ll 1$. This allows us to approximately map the gate dynamics to that of a fluxon scattering in the 1-b circuit shown in the right column of Table III. In this mapping each of the lower LJJs S_2, S_2' of the IDSN, including its termination JJ with parameters $(\hat{C}_J, \hat{I}_c)$, is replaced by a single effective JJ, with characteristics

$$C_J^\alpha = \hat{C}_J + \frac{C_J}{e^{2\mu a} - 1}$$
$$I_c^\alpha = \hat{I}_c + \frac{I_c}{e^{2\mu a} - 1} + \frac{\Phi_0}{2\pi} \frac{(e^{\mu a} - 1)^2}{L(e^{2\mu a} - 1)} \qquad (2)$$

where μ is the inverse decay length ($\mu \lesssim 1/\lambda_J$) of the edge states. These quantities are derived in the Appendix, where we parameterize the LJJ fields by exponentially localized edge states, $\phi_n \propto e^{-\mu a|n|}$ and, thus, reduce the many degrees of freedom of each LJJ together with its termination JJ to the amplitude of the edge state. Furthermore, by comparing the plasma frequency of the effective JJ, $\omega_J^\alpha(\mu) = \sqrt{2\pi I_c^\alpha/(\Phi_0 C_J^\alpha)}$, with the frequency $\omega_{\rm bulk}(\mu)$ with which the edge states oscillate in the LJJ bulk, we can estimate $\mu = 0.68/\lambda_J$. The resulting values from (2) are given in the right column of Table III.

We have simulated the fluxon scattering dynamics of the equivalent 1-b interfaces in Table III. In case (i) (left column of Table III), where the reduction is exact due to symmetry, there is of course full agreement with Fig. 3(d). In case (ii) (right column of table III), although the reduction is only approximate, it nevertheless leads to excellent agreement between the 2-b gate dynamics, as is seen in the comparison between Figs. 3(b) and 8.

IV. SNL GATE

The IDSN gate is an example of a ballistic 2-b gate, with an energy efficiency close to unity ($\ge 86\%$ for the IDSN gate with margins defined in Fig. 4). In the case of its two-fluxon operation, the high energy efficiency, however, relies on the input of two well-synchronized input fluxons, cf. last panel in Fig. 4. Moreover, fluxon velocity of course needs to be restored after a sequence of ballistic gates. Therefore, in addition to the *ballistic*

logic gates, *clocking* gates are required for fluxon synchronization and for restoring fluxons to a velocity within the velocity range of the ballistic gates. We have developed such SNL gates, which store the bit state of an incoming (slowed-down) *data* fluxon. Later, triggered by the interaction with a timed *clock* fluxon, the SNL launches the stored bit as a *data* fluxon carrying the original bit state on an output LJJ (at a certain higher speed). The clock fluxon, which is annihilated in the process, serves as the power source of this thermodynamically irreversible gate.

Earlier, we had introduced a one-input SNL gate, which has a single-input LJJ for data [10]. Here, we report on a related two-input SNL, where a data fluxon can come in on one of two input LJJs. The schematic of the two-input SNL is shown in Fig. 5(a). As an additional feature, our SNL gates have two-output LJJs. The output fluxon is launched into one of them, depending on the stored bit state. Both, the bit-dependent routing and the existence of more than one-input port, are not general properties of clocking gates, but are required in the particular application for which we have developed the SNL gate, namely as a component of a CNOT gate. The application is discussed below in Section V, including Fig. 6.

The gate circuits of the *ballistic* RFL gates have left–right symmetry as a necessary condition for logic reversibility: Running the gate "backward," by reverting the momentum of the output fluxons, will restore the gate's input state. In a ballistic gate, the sets of input and output LJJs are, therefore, interchangeable. In contrast, the irreversible SNL gates do not have left–right symmetry, and the role of each LJJ is fixed as either input or output channel. The SNL gates, however, have top–bottom symmetry, such as in the two-input SNL of Fig. 5(a), where the center capacitor $\hat{C}^y$ together with the clock LJJ (coming out of the article) define the symmetry plane of the circuit.

The two-input SNL circuit, in Fig. 5(a), consists of a central storage cell, comprised of inductors of small values $\hat{L}^A, \hat{L}^B, \hat{L}^y$, and the JJs J1–J4, with critical currents $\hat{I}_c^L, \hat{I}_c^R$, which terminate the input and output LJJs. On the input side, these JJs (J1 and J4) are also resistively shunted with resistance $\hat{R}^L$. All other JJs in Fig. 5(a) are undamped, and all JJs have the same plasma frequency as the JJs in the LJJs, $\omega_J = \sqrt{2\pi I_c/(\Phi_0 C_J)}$. Additional circuit elements are either directly in parallel to the clock LJJ, such as capacitance $\hat{C}^y$, or in parallel with other parts of the storage cell, such as capacitance $\hat{C}^x$ and resistance $\hat{R}^x$.

All input and output LJJs have equal properties, with the JJ characteristics (C_J, I_c), cell inductance L, and cell length a. The parameters of the clock LJJ are scaled relative to these data LJJs according to $(C_J^{\rm clk}, I_c^{\rm clk}, L^{\rm clk}, a^{\rm clk}) = (C_J/s, I_c/s, sL, a)$, here with a factor $s = 2$. This scaling implies that the clock LJJ has the same Josephson penetration depth λ_J, and the same upper velocity bound $c = \omega_J \lambda_J$ as the data LJJs. However, compared with the latter ones, the characteristic impedance in the clock LJJ is a factor of s larger, $\sqrt{L^{\rm clk}/C_J^{\rm clk}} = s\sqrt{L/C_J}$, and the rest energy of a clock fluxon is reduced by a factor of s^{-1}, $E_{\rm fl}^{\rm clk}(0) = E_{\rm fl}(0)/s$. As will be discussed in more detail later, this is done in order to minimize the energy cost of the launching process, in which the clock fluxon is annihilated. Its energy should, therefore, be as small as possible (while still properly launching the data fluxon) to make the SNL energy-efficient.

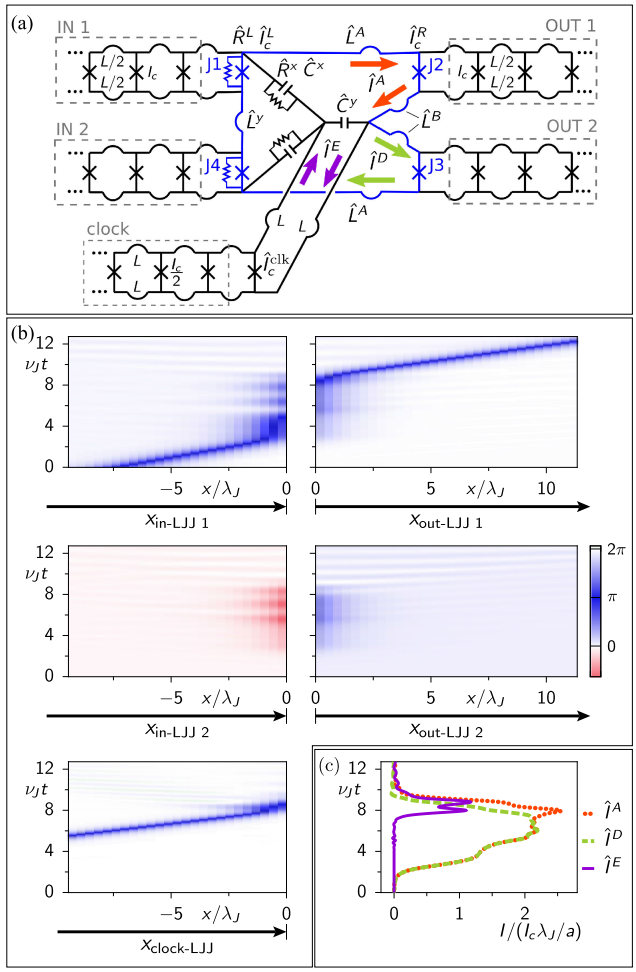
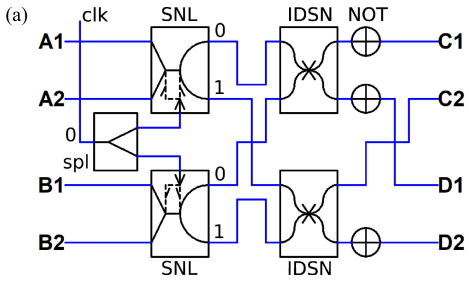


Fig. 5. Two-input SNL gate receives one-input data fluxon from one of two possible input LJJs. (a) SNL gate circuit. After the data fluxon enters through input LJJ 1 or 2, the bit is stored as a circulating current in a center storage cell, which contains JJs J1-J4 (connected to the input and output LJJs) and inductors $\hat{L}^A, \hat{L}^B$, etc. The storage cell (marked in blue) has bottom–top symmetry, where the symmetry line is defined by the center capacitor $\hat{C}^y$ and connected clock LJJ. (For clarity, some circuit elements are left unlabeled, such as $\hat{I}_c^L[\text{J4}] = \hat{I}_c^L[\text{J1}]$, because they are determined by top–bottom symmetry.) A low-energy clock fluxon is sent in on the clock LJJ and will cause a stored bit state 0 (1) to be launched as a fluxon (an antifluxon) on the upper (lower) output LJJ. (b) LJJ phases $\phi_n(t)$ versus positions x and time t: A data fluxon (bit state 0) comes in on input LJJ 1 with velocity $v_{\rm in} = 0.4c$ and settles into the storage cell of the SNL. The stored data bit later gets launched into output LJJ 1 by a low-energy clock fluxon arriving from the clock LJJ at $\nu_J t_{\rm clk} \approx 8$. (c) Storage-cell currents $\hat{I}(t)$, as defined in (a): The current generated by the stored data fluxon is equal in upper and lower parts of the storage cell, $\hat{I}^D \approx \hat{I}^A$ for $t < t_{\rm clk}$. Later, the superposition of this storage current with that of the clock fluxon (with same polarity as the data fluxon, $\hat{I}^E \cdot \hat{I}^A > 0$) leads to a current imbalance $\hat{I}^A > \hat{I}^D$, and eventually to the launch of the stored bit as a new fluxon into output LJJ 1. In contrast, a stored antifluxon (bit state 1) would get launched into output LJJ 2. The parameters of the simulation for (b) and (c) are given in the text.

Fig. 5 illustrates the dynamics of the two-input SNL in simulation. The panels of Fig. 5(b) show colormaps of the JJ-phases $\phi_n(t)$ versus position x in the individual LJJs: $x = 0$ corresponds to the position of the storage cell, $x < 0$ is assigned to the input and clock LJJs to the left, and $x > 0$ to the output LJJs to the right. Fig. 5(c) shows the currents in the storage cell and at the end of the clock LJJ. When a data fluxon arrives from one of

(a)



(b)

input		SNLs		output	
A	B	rout to		C = A ⊕ B	D = A
0	0	C1	D1	0	0
0	1	C1	D2	1	0
1	0	C2	D1	1	1
1	1	C2	D2	0	1

Fig. 6. (a) Schematic for a composite CNOT logic gate designed with RFL components: Two ballistic IDSN gates, two 2-input SNL clocking gates, three NOT gates, a splitter, and LJJs as "wiring" (blue). (b) CNOT logic table resulting from gate actions and routing in (a). The bit states A and B (columns 1 and 2) are defined by the two data fluxons coming in on one of the input ports A1 or A2, and on one of B1 or B2, respectively. The input bit states A and B are each stored in an SNL gate. A clock fluxon is sent in and at a splitter fans out into two half-energy ones. These clock fluxons power the synchronized launch of the stored data bits. The launched data bits are routed on bit-state dependent paths (columns 3 and 4). After action of the IDSN and NOT gates the bit state D (appearing either on path D1 or D2) is a copy of A, and the bit state C (on path C1 or C2) is XOR(A,B).

the input LJJ(s)—here it is the upper one—it generates a current circulating in the storage cell, with evanescent excitations of the JJs in the input and output LJJs. The current distribution over the various inductors differs from that of a soliton in the LJJ, but of course the total flux is still one flux quantum. The circulation direction of the storage current is equal to that of the incoming data fluxon: For input bit state 0 (1), it circulates clockwise (anticlockwise). Due to the geometry of the SNL, the storage current is distributed symmetrically in the storage loop, $\hat{I}^A \approx \hat{I}^D$ [indicated by red and green arrows in Fig. 5(a) and corresponding data line in Fig. 5(c)]. The symmetry implies that no current $\hat{I}^E$ (ac or dc) is excited at the end of the clock LJJ (purple arrows and data line) during this storage stage of the operation.

Later, a clock fluxon is sent in through the clock LJJ and arrives at time $t_{\rm clk} \approx 8/\nu_J$. The clock fluxon, which is assumed to be of polarity equal to data state 0, induces a current $\hat{I}^E$ (purple arrows) at the storage cell, which adds constructively (destructively) with the current $\hat{I}^A$ ($\hat{I}^D$) in the upper (lower) part of the storage cell (red and green). This results in an imbalance, $\hat{I}^A > \hat{I}^D$, which grows and feeds the phase gradient in the upper output LJJ 1. The phase gradient in the upper output LJJ 1 gradually forms into a new data fluxon, which eventually launches. If the storage current were circulating anticlockwise instead, corresponding to a stored bit state 1, an antifluxon would get launched, but then into the lower output LJJ 2. After the launching process, the currents in the storage cell and in the clock LJJ go to zero since flux is no longer stored.

When the SNL gate stores flux, it stores a large fraction of the rest energy (potential energy) of the incident fluxon. However, some energy of the input fluxon is dissipated in the resistors to ensure that the fluxon is not immediately emitted from the storage loop back to one of the input LJJs, but settles into a static stored flux state. In the simulation shown in Fig. 5, the damping occurs as a two-step process, with temporary dissipation events at $\nu_J t \approx 3$ (when the incoming data fluxon is initially stopped close to $x \lesssim 0$) and at $\nu_J t \approx 6$ (when the data fluxon is finally absorbed fully such that the storage current rises to a saturation value). Later, when the clock fluxon arrives, it generates dissipative currents mostly on the bridge resistors $\hat{R}^x$. Dissipation is dominant on the lower of these two in the example shown in Fig. 5 where the storage current circulates clockwise (bit state 0) and a fluxon is launched into output LJJ 1.

One purpose of our SNL clocking gate is to restore the energy of a data fluxon to a value suitable for the input fluxon of a ballistic gate like the IDSN. For the SNL gate studied in Fig. 5, we use a data fluxon with input velocity $v_{\rm in} = 0.4c$, corresponding to $E_{\rm fl}(v_{\rm in}) = 8.7E_0$, cf. (1). This value is close to the minimum of the operational range of the SNL. (An input fluxon with velocity below this minimum would get reflected instead of being stored.) The bit gets stored as a flux quantum in the storage cell with an energy of $U_{\rm stored} \approx 8E_0$, close to the rest energy of the data fluxon. The clock fluxon is sent in with $v^{\rm clk} = 0.6c$ in the simulation of Fig. 5, corresponding to the fluxon energy $E_{\rm fl}^{\rm clk}(v^{\rm clk}) = 5E_0$ (recall that the rest energy of a clock fluxon is smaller than that of a data fluxon, $E_{\rm fl}^{\rm clk}(0) = E_{\rm fl}(0)/2 = 4E_0$). The initial energy of the input fluxons is $E_{\rm init} = E_{\rm fl}(v_{\rm in}) + E_{\rm fl}^{\rm clk}(v^{\rm clk}) = 13.7E_0$. In the simulations the output data fluxon has an energy of $E_{\rm fl}(v_{\rm out} = 0.51c) = 9.3E_0$, giving an energy efficiency of $E_{\rm fl}(v_{\rm out})/E_{\rm init} = 69\%$. Even though this is less efficient compared with the ballistic RFL gates, it is efficient relative to irreversible logic (CMOS or irreversible SFQ), which consumes at least the entire potential energy of the bit state in switching.

The SNL energies and efficiencies are summarized in the second column of Table IV, both for the case of $v_{\rm in} = 0.4c$ (shown in Fig. 5) and the case of a larger input velocity, $v_{\rm in} = v_{\rm out}$, where the efficiency drops to 65%. One may compare them to the values that are theoretically achievable in an ideal case. We define an "ideal" SNL as one where the energy of the new data fluxon equals the sum of the original data fluxon's rest energy and the energy of the clock fluxon, $E_{\rm fl}(v_{\rm out}) = 8E_0 + E_{\rm fl}^{\rm clk}(v^{\rm clk})$. In other words, the clock fluxon transfers its entire energy to launch a fluxon from the stored bit state, which is stored at an energy $U_{\rm stored} = 8E_0$ corresponding to that of a static fluxon in the LJJ bulk. This choice of $U_{\rm stored}$ ensures that input data fluxons of (in principle) arbitrary input velocity $v_{\rm in}$ could be successfully stored. (Whereas in the realistic case of Fig. 5, a lower $v_{\rm in}$-bound exists, as mentioned earlier.) The third and last column of Table IV list the resulting maximum efficiencies, for $v^{\rm clk} = 0.6c$ and two clock LJJ scaling factors $s = E_{\rm fl}(0)/E_{\rm fl}^{\rm clk}(0)$. The ideal energy efficiency (at $v_{\rm in} = v_{\rm out}$) for the SNL gate with $s = 2$ is 72% (third column). The one-input SNL introduced earlier [10] uses $s = 4$, and here, we find the ideal efficiency (again at $v_{\rm in} = v_{\rm out}$) for this gate to be 81% (last column).

For the two-input SNL circuit of Fig. 5(a), we have tuned the parameters of the storage cell for an efficient conversion of the

TABLE IV
SNL GATE PERFORMANCE, WHICH DEPENDS ON s (CLOCK LJJ SCALING), v^{CLK}, AND v_{IN}

	parameters of Fig. 5	'ideal': $E_{\mathrm{fl}}(v_{\mathrm{out}}) = 8E_0 + E_{\mathrm{fl}}^{\mathrm{clk}}(v^{\mathrm{clk}})$	
s	2	2	4
$E_{\mathrm{fl}}^{\mathrm{clk}}(v^{\mathrm{clk}} = 0.6c)$	$5E_0$	$5E_0$	$2.5E_0$
$E_{\mathrm{fl}}(v_{\mathrm{out}})$	$9.3E_0$	$13E_0$ (**)	$10.5E_0$ (**)
v_{out}	$0.51c$ (*)	$0.79c$	$0.65c$
Slow input case: $v_{\mathrm{in}} = 0.4c$			
$E_{\mathrm{fl}}(v_{\mathrm{in}})$	$8.7E_0$	$8.7E_0$	$8.7E_0$
efficiency	69%	95%	94%
Fast input case: $v_{\mathrm{in}} = v_{\mathrm{out}}$			
v_{in}	$0.51c$	$0.79c$	$0.65c$
$E_{\mathrm{fl}}(v_{\mathrm{in}})$	$9.3E_0$	$13E_0$	$10.5E_0$
efficiency	65%	72%	81%

(*) Measured in the simulation. (**) According to stated criterion.
Note: Relations $E_{\mathrm{fl}}(v)$ are according to (1), and the efficiency is $E_{\mathrm{fl}}(v_{\mathrm{out}})/(E_{\mathrm{fl}}(v_{\mathrm{in}}) + E_{\mathrm{fl}}^{\mathrm{clk}}(v^{\mathrm{clk}}))$. "Ideal" performance assumes that the bit state is stored at the rest energy $8E_0$ of the data fluxon, i.e., its kinetic energy is lost, and that the entire clock fluxon energy is transferred to the launched fluxon (see text).

clock-fluxon energy into kinetic energy of the launched fluxon. The optimization is done for fixed clock fluxon energy and under the condition that the input energy of the data fluxon lies in a range that covers at least the interval $(8.7E_0, 10E_0)$. Using these criteria, we find the following parameters of the storage cell: $\hat{I}_c^L/I_c = \hat{C}_J^L/C_J = 2.6$, $1/\hat{R}^L = 0.1/Z$ (JJs J1 and J4), $\hat{I}_c^R/I_c = \hat{C}_J^R/C_J = 2.4$ (JJs J2 and J3), $\hat{L}^A = \hat{L}^B = \hat{L}^y \ll L$, $\hat{C}^x = 2.0C_J$, $1/\hat{R}^x = 1.7/Z$, $\hat{C}^y = 1.0C_J$ (storage cell with damping elements and coupling to clock LJJ). Herein, $Z = \sqrt{L/C_J}$ is the characteristic impedance of the data LJJs. As mentioned earlier, the clock LJJ has bulk parameters $I_c^{\mathrm{clk}}/I_c = C_J^{\mathrm{clk}}/C_J = 0.5$ and $L^{\mathrm{clk}}/L = 2.0$; however, the last JJ is here also modified $\hat{I}_c^{\mathrm{clk}}/I_c = \hat{C}_J^{\mathrm{clk}}/C_J = 1.0$. These parameters of the two-input SNL gate are used in the simulation shown in Fig. 5.

We note that we have found parameters with improved energy efficiency compared with the parameters used in Fig. 5. However, these usually only allow a very narrow range of input velocities: If the input velocity lies below that range, the data fluxon gets reflected before entering the storage cell. If the velocity exceeds the upper limit of that range, the input data fluxon is also not stored but moves directly into the other input LJJ. In contrast, the previously studied one-input SNL [10] does of course not have the latter limitation. Besides, the one-input SNL can have a higher launch efficiency because the stored current excites evanescent phase fields in one fewer LJJ. In some applications, however, it is necessary to have an SNL gate with the same number of input and output LJJs (as well as bit dependent routing). One important example is the CNOT gate discussed in the following section.

V. CNOT GATE IN RFL

Some of our 2-b logic gates are purely ballistic, i.e., the logic action is generated alone through the inertia of (synchronous) input fluxons. Examples include the NSWAP [9] and IDSN gate. However, fluxon dynamics in the 2-b gate circuit, Fig. 1(b), can only render a subset of all reversible 2-b logic gates: Namely those that act in the same way on an input state combination as on its inverse, e.g., on the input state (0,0) as on (1,1). Clearly, the NSWAP gate and IDSN gate (see Table II) belong to this subset. The above restriction originates from the absence of an external magnetic field or stored flux, making the circuit dynamics invariant under a sign change of the phases. Additionally, a sign change of the input LJJ phases corresponds to the inversion of the input fluxon polarities and, thus, to the inversion of the input bit states. Thus, the gate dynamics resulting, e.g., for the input state (0,0) is fully equivalent to that for input state (1,1).

Other reversible logic gates, such as the CNOT do not belong to the abovementioned subset and, thus, cannot be achieved by a ballistic RFL gate alone. However, by combining ballistic logic gates with circuit elements for synchronization and routing, we can construct more complex logic gates such as the CNOT [10]. Fig. 6(a) shows the schematic for an RFL implementation of a CNOT, which consists of two SNL clocking gates, two IDSN logic gates, and other routing components.

We shortly describe the operation of the composite CNOT: The input consists of two fluxons, carrying bit states A and B, respectively. Bit A comes in from the left on either of the input ports A1 or A2 of a two-input SNL where it is stored. Similarly, bit B comes in on either B1 or B2 and is stored in a second SNL. Later, a clock fluxon is sent in on a clock LJJ, which has regular LJJ characteristics (C_J, I_c, L, a). A T-branch splitter [25], [26] divides the original clock LJJ into two clock LJJs with characteristics $(C_J/2, I_c/2, 2\,L, a)$, and as a result the original clock fluxon splits into two half-energy clock fluxons moving at the original speed. The two clock LJJs are each connected to an SNL, where the impinging clock fluxons synchronously launch the stored bits A and B as a fluxon or antifluxon. The launch is bit-state dependent, where the bit state 0 (1) is launched as a fluxon (antifluxon) into the upper (lower) output LJJ of each of the SNLs. We note that the two clock LJJs have to be wired to their respective SNL in a different way, in order to achieve the same launch directionality in both LJJs. This difference is indicated in Fig. 6 by the two distinct circuit symbols for the two SNLs. While the upper SNL corresponds exactly to the schematic of Fig. 5(a), the lower SNL has a half-twist in the clock LJJ relative to that schematic.

The output LJJs of the two SNLs are connected to two IDSN gates in such a way that any bit state 0 of the two launched data fluxons will arrive at the upper IDSN and any bit state 1 will arrive at the lower IDSN. Depending on the initial bit states (A,B), either both IDSN gates receive a single fluxon as their input, or only one IDSN gate receives two-input fluxons with the same polarity. According to the logic action of the IDSN, Table II, in the former case, the single-input fluxon or antifluxon undergoes an ID operation. In the latter case, the two fluxons are well synchronized thanks to the simultaneous launch from the two SNLs. They will then both undergo NOT dynamics in the IDSN gate. The output fluxon(s) of the IDSN appear on its upper (lower) output LJJ if they entered on the upper (lower) input LJJ. Next, some of the fluxons pass through a NOT gate on the way to the output ports C1, C2, D1, D2 of the CNOT. The routing to these ports is done such that exactly one fluxon arrives on either C1 or C2, and thus uniquely defines the output bit C

of the CNOT gate. Similarly, exactly one fluxon arrives on either D1 or D2 and defines the output bit D. The combined action of the clocking gates (SNL), ballistic logic gates (IDSN, NOT), and the routing ensures that these output bit states are related to the input bit states in form of the CNOT logic, see table in Fig. 6(b). These bits can then each be stored in another SNL for subsequent processing if desired. For example, one can cascade two CNOTs after one another to logically reverse the operation.

VI. Conclusion

Reversible digital logic is important for the future development of computing because of the much higher energy efficiency compared with irreversible logic gates, including industry CMOS gates and the most developed SFQ logic. Recent demonstrations of such gates in superconducting circuits are *adiabatic*-reversible, making use of the inverse scaling between gate time and energy cost. In contrast, we are developing RFL based on *ballistic*-reversible gates. These are powered alone by the inertia of incoming fluxons, which at the same time are the input bits themselves. The ballistic gates in RFL exploit a resonant scattering process at special interfaces between LJJs. This scattering achieves conditional polarity inversion of an input fluxon, dependent on the gate type and input bits. The advantage of RFL over irreversible logic is the full conservation of the rest (potential) energy of fluxons in logic operations. In our simulations, this makes up 80% of the fluxons' total energy. Ballistic-reversible gates moreover conserve a large fraction of the kinetic fluxon energy, thus yielding conservation of up to 97% of fluxon energy. Ballistic-reversible gates include the 1-b NOT and ID, and the 2-b NSWAP and IDSN gates.

The CNOT is implemented in RFL as a composite gate from a set of ballistic and nonballistic gates. This includes two IDSN gates, three fundamental NOT gates, and two SNL gates. The SNL is a clocking gate that stores the bit state of an incoming fluxon and later launches it as a new fluxon on a bit-state dependent output LJJ. In the SNL version described here, the launch is powered by a clock fluxon at half of the data fluxon energy. In the CNOT, the data fluxon launch from the two SNL gates is synchronized, using the simultaneous arrival of clock fluxons that are fanned out from a single source.

Unlike the ballistic RFL gates, which are nominally undamped, the SNL gate uses damping resistors to ensure that the incoming data fluxon gets stored as a static flux in the SNL storage cell. In the launch process, the clock fluxon is annihilated. A part of its energy goes to the launched data fluxon, which then may end up with larger energy than the input data fluxon. The other, larger part of the clock fluxon energy is dissipated in the resistors. However, since the clock fluxon has only a fraction of the data fluxon's energy, and since much of the rest energy of the input data fluxon is preserved, the SNL gate may be very efficient by irreversible logic standards.

These studies indicate that reversible computing should not be thought of only in terms of the adiabatic model. Ballistic-reversible gates enabled by resonant fluxon scattering seem to be an implementable alternative. Combined with clocking gates that preserve the rest energy of the bits, ballistic gates can be used to build complex logic gates.

Appendix
Modelling an LJJ With Weakly Excited Edge State

In the single-fluxon operation of the IDSN gate, where, e.g., the fluxon comes in and leaves on LJJs S_1 and S_1', the two other LJJs S_2 and S_2' are only weakly excited throughout the gate operation, cf. Fig. 3(b). The phase fields temporarily excited in these LJJs have the form of exponentially localized edge states at the interface and undergo a slow coherent oscillation. The contribution of each of those LJJs—including the parallel interface JJ—can then be analyzed in terms of a model, which parameterizes the phase fields as edge states, e.g., on the lower right interface JJ and LJJ S_2'

$$\phi_n = \phi_R(t) e^{-\mu a n} \tag{3}$$

with an inverse decay length μ. Herein, $n = 0$ labels the lower right interface JJ with characteristics $(\hat{C}_J, \hat{I}_c)$, and $n = 1, 2, \ldots$ label the JJs in S_2' in increasing distance $x = an$ from the interface.

For concreteness, we show here how the model is applied to the right LJJ S_2'; the same procedure applies to S_2. The starting point for the analysis is the circuit Lagrangian of S_2' together with the lower right interface JJ

$$\begin{aligned}\mathcal{L} = {} & \left(\frac{\Phi_0}{2\pi}\right)^2 \left[\frac{\hat{C}_J}{2}\dot{\phi}_0^2 + \sum_{n=1}^{N} \frac{C_J}{2}\left(\dot{\phi}_n\right)^2\right] \\ & - \left(\frac{\Phi_0}{2\pi}\right)\left[\hat{I}_c(1-\cos\phi_0) + \sum_{n=1}^{N} I_c(1-\cos\phi_n)\right] \\ & - \left(\frac{\Phi_0}{2\pi}\right)^2 \sum_{n=1}^{N} \frac{(\phi_n - \phi_{n-1})^2}{2\,L}\,. \end{aligned} \tag{4}$$

For small amplitudes $\phi_n \ll \pi$, (4) can be expanded to quadratic order in ϕ_n. We insert (3) and extend the sums, $N \to \infty$, under the assumption that the LJJ size is much larger than the decay length of the edge state, $(N-1)a \gg \mu^{-1}$. With these approximations, the Lagrangian reduces to that of a simple LC-oscillator of the edge phase ϕ_R

$$\mathcal{L} = \left(\frac{\Phi_0}{2\pi}\right)^2 \left[\frac{C_J^\alpha}{2}\left(\dot{\phi}_R\right)^2 - \frac{1}{2\,L^\alpha}\phi_R^2\right] \tag{5}$$

with μ-dependent effective parameters

$$C_J^\alpha = \hat{C}_J + C_J f(\mu) \tag{6}$$

$$\frac{1}{L^\alpha} = \frac{2\pi}{\Phi_0}\left(\hat{I}_c + I_c f(\mu)\right) + \frac{g(\mu)}{L}\,. \tag{7}$$

Herein, we have defined the functions

$$f(\mu) = \sum_{n=1}^{\infty} e^{-2\mu a n} = (e^{2\mu a} - 1)^{-1} \tag{8}$$

$$g(\mu) = \sum_{n=1}^{\infty}\left(e^{-\mu a n} - e^{-\mu a(n-1)}\right)^2 = (e^{\mu a} - 1)^2 f(\mu). \tag{9}$$

Since $\phi_R \ll \pi$, we can also interpret (5) as the Lagrangian of a single JJ expanded to lowest orders. This JJ has (shunt)

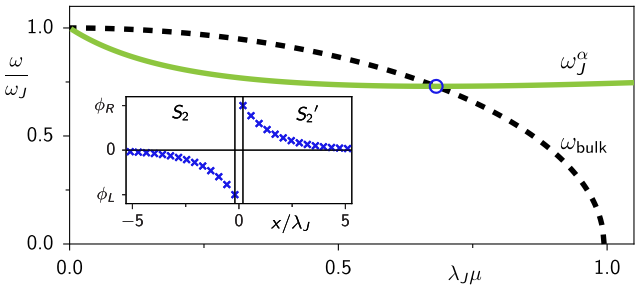


Fig. 7. Bulk frequency $\omega_{\rm bulk}$ from (13) (black dashed) and plasma frequency $\omega_J^\alpha = \sqrt{2\pi I_c^\alpha/(\Phi_0 C_J^\alpha)}$ of the effective JJ, (6), (10) (green solid), as functions of inverse decay length μ of an LJJ edge state, cf. (3). The edge states in LJJs S_2 and S_2', with μ according to the intersection point of the two frequencies, are shown in the inset. Equations (6) and (10) are evaluated with interface parameters of IDSN gate, see caption of Fig. 3.

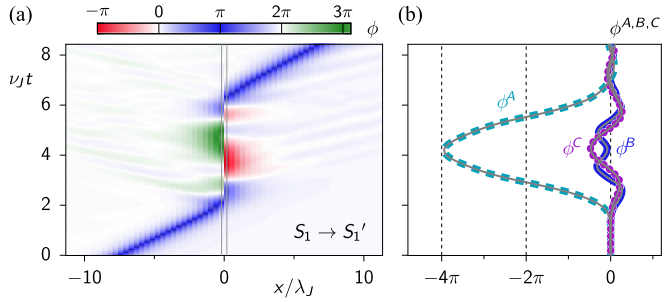


Fig. 8. Dynamics of 1-b gate circuit shown at bottom right of Table III, with interface parameters stated ibid. By construction, the dynamics is approximately equivalent to the IDSN gate dynamics under single-fluxon input. This is evident when comparing the JJ-phases ϕ_n shown here in (a) with the JJ phases on LJJs S_1 and S_1 of the IDSN gate, shown in the first panel of Fig. 3(b). Also the rail-JJ phases shown here in (b) for both the 1-b interface (thick lines in color) and the IDSN gate with single-fluxon input (thin gray lines) are basically indistinguishable on this scale.

capacitance $C_J^\alpha(\mu)$ and critical current $I_c^\alpha(\mu)$

$$I_c^\alpha = \frac{\Phi_0}{2\pi}\frac{1}{L^\alpha(\mu)} = \hat{I}_c + I_c f(\mu) + \frac{\Phi_0}{2\pi}\frac{g(\mu)}{L}\,. \qquad (10)$$

By construction, the dynamics of this JJ should be equivalent to the dynamics of the lower right interface JJ together with the parallel LJJ S_2', provided that it is only weakly excited by a fluxon from S_1. We can apply the same model to the lower left interface JJ and LJJ S_2, with edge state ansatz

$$\phi_n = \phi_L(t)e^{-\mu a n} \qquad (11)$$

where $x = -an \le 0$ and $n = 1, 2, \ldots$ label the JJs in the LJJ with increasing distance from the interface. Because of the left–right symmetry of the 2-b gate structure, the resulting equivalent JJ of course has the same parameters, $C_J^\alpha(\mu)$ and $I_c^\alpha(\mu)$.

In the edge state ansatz, (3) and (11), the inverse decay length μ is still an unknown parameter and remains to be evaluated. Here, we fix μ by the condition that the plasma frequency $\omega_J^\alpha = \sqrt{2\pi I_c^\alpha/(\Phi_0 C_J^\alpha)}$ of the effective JJ matches the frequency, with which the edge state oscillates, $\dot{\phi}_n = \omega\phi_n$. We approximate the latter as the oscillation frequency $\omega_{\rm bulk}$ in the bulk of the LJJ, which follows from the bulk equations of motion

$$\ddot{\phi}_n - \frac{c^2}{a^2}\left(\phi_{n+1} - 2\phi_n + \phi_{n-1}\right) + \omega_J^2 \sin\phi_n = 0\,. \qquad (12)$$

After linearizing for small excitations, $\phi_n \ll \pi$, and inserting (3) or (11) we obtain the bulk dispersion relation

$$\omega_{\rm bulk}^2 = \omega_J^2 + \frac{2c^2}{a^2}\left(1 - \cosh(a\mu)\right)\,. \qquad (13)$$

In the homogeneous limit, $a \to 0$, where (12) turns into the sine-Gordon equation, $\ddot{\phi} - c^2\phi'' + \omega_J^2 \sin\phi = 0$, (13) simplifies to $\omega^2 = \omega_J^2(1 - \lambda_J^2\mu^2)$.

Fig. 7 shows $\omega_{\rm bulk}$ from (13) (black dashed) together with the plasma frequency ω_J^α of the effective JJ (green solid). For the latter, we have used the parameters of the IDSN interface, cf. the caption of Fig. 3. At the intersection point, $\lambda_J\mu = 0.68$, $\omega/\omega_J = 0.73$, both relations between frequency ω and inverse decay length μ are satisfied. The inset of Fig. 7 illustrates the edge states in LJJs S_2 and S_2' for this μ-value, and for $\phi_L = -\phi_R$. With $\lambda_J\mu = 0.68$ and the parameters of the IDSN interface, we obtain $C_J^\alpha \approx 7.3C_J$ and $I_c^\alpha \approx 3.9I_c$. With these parameters, the 1-b structure shown in the right column of Table III is approximately dynamically equivalent to the 2-b IDSN structure under single-fluxon input, as demonstrated in Fig. 8, in comparison with Fig. 3(b).

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