Development of RF Power Dividers for the Josephson Arbitrary Waveform Synthesizer

Hao Tian, Oliver Kieler, Ralf Behr, Ruediger Wendisch, Rolf-Werner Gerdau, Karsten Kuhlmann, and Johannes Kohlmann

***Abstract*—To make the experimental setup of the Josephson arbitrary waveform synthesizer less complex by reducing the number of RF cables between room and cryogenic temperature, we developed on-chip RF power dividers. By integration of these components, we can eventually increase the number of Josephson junctions operated by one single pulse-pattern generator channel, and thus reduce the costs of the setup. At Physikalisch-Technische Bundesanstalt, we designed, fabricated, and investigated the performance of two different RF power dividers types: the serial–parallel and the Wilkinson power divider. Spectrally pure sinusoidal waveforms were successfully synthesized with both types of power dividers. With the Wilkinson power divider, we obtained 17.55 mV (rms) at a clock frequency of 15 GHz combined with a test array of 1000 Josephson junctions. As for the serial–parallel power divider combined with a test array of 2000 Josephson junctions, we synthesized rms output voltages of 19.0 mV.**

***Index Terms*—AC Josephson voltage standards, pulse-driven Josephson series arrays, serial–parallel power divider, SNS Josephson Junctions (JJs), wilkinson power divider.**

I. Introduction

THE Josephson arbitrary waveform synthesizer (JAWS) is based on a series array of nonhysteretic SNS Josephson junctions (JJs) (S: superconducting, N: normal metal) driven by a high-speed digital sequence of short current pulses from a commercial pulse-pattern generator (PPG), in which the corresponding waveform is encoded by $\Sigma\Delta$ analog-to-digital conversion. These pulse-driven series arrays operated at 4 K enable spectrally pure ac voltages to be synthesized in a wide frequency range from dc up to MHz [1]–[3]. The short current pulses (pulse repetition frequency f_{p}) transfer flux quanta $\Phi_0 = h/2e$ (h is Planck's constant and e the elementary charge) through each junction, which result in a quantized ac voltage of high spectral purity with no drift and low noise. According to the Josephson equation, the output ac voltage and its frequency are in general given by

$$V_{\mathrm{rms}} = \left(\frac{1}{\sqrt{2}}\right) A_{\Sigma\Delta} mn \Phi_0 f_{\mathrm{clock-PPG}} \tag{1}$$

$$f_{\mathrm{AC}} = T_{\Sigma\Delta} f_{\mathrm{clock-PPG}} / L_{\Sigma\Delta} \tag{2}$$

where m is the number of JJs, n is the Shapiro-step number (typically: $n = 1$), $f_{\mathrm{clock\text{-}PPG}}$ is the clock frequency of the PPG, and $A_{\Sigma\Delta}$ is the code amplitude factor ($0 < A_{\Sigma\Delta} < 1$, i.e., density of pulses in the code). The frequency of the output ac voltage is dependent on the code length $L_{\Sigma\Delta}$ and the number of periods $T_{\Sigma\Delta}$. The maximum code length $L_{\Sigma\Delta}$ of the PPG limits the lower frequency that can be synthesized. DC output voltages are possible by sending pulses with a constant pulse repetition frequency. On the other side, the JAWS signals can be synthesized up to the megahertz range and above [2]. The JAWS systems are used in different metrological applications and measurements, e.g., for ac calibrations [3], Josephson impedance bridges [4], [5], and Johnson noise thermometry [6], [7].

For many years, it was difficult to generate high output voltages with a JAWS, because each series array of JJs requires the drive by its own channel of the PPG. In addition, the length of the series arrays is limited because of the attenuation of the transmission line; all JJs in the series arrays must show common Shapiro steps at all different pulse repetition frequencies. In our previous work of JAWS, we connected each JJ array on a 10 mm × 10 mm chip to a single high-speed PPG channel with a RF cable, which transmits the pulses from the PPG at room temperature to the JAWS chip operated at 4 K. By using eight JJ arrays (arranged on 4 separate chips) with 63 000 junctions in total, rms output voltages of 1 V were generated [8]; similar results were also achieved by Benz *et al.* [9]. For higher output voltages, extra PPG channels and RF cables were needed, which caused unwanted cross-talk between the PPG channels and additional costs of the equipment. To reduce the number of electrical pulse-channels at room temperature and to lower the costs of the PPG, broadband on-chip RF power dividers have been developed at NIST [10], with a goal to deliver equally optimal pulse transmission into each parallel JJ array. This article describes the latest achievements of broadband on-chip RF power dividers for JAWS circuits developed at Physikalisch-Technische Bundesanstalt (PTB). These power dividers will be used for the operation of a larger number of JJs and to eventually increase the output voltage that is generated by a single chip.

II. Design and Simulation

Power dividers are straightforward passive RF components, that are used for power division or power combination. For

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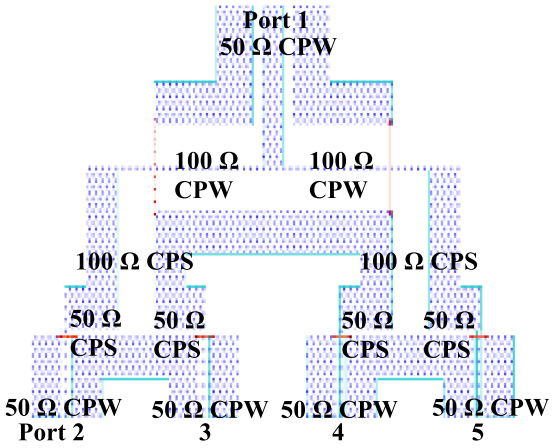

Fig. 1. Structure of serial–parallel power divider and its port definition.

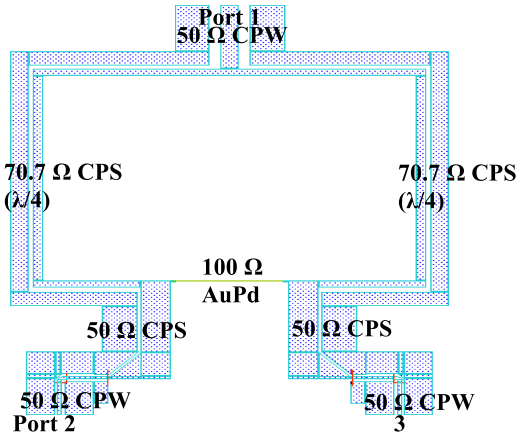

Fig. 2. Structure of Wilkinson power divider and its port definition.

integration into JAWS circuits, a power divider must be rather broadband to enable the transmission of the short current pulses containing frequency components from sub-GHz up to about 30 GHz. At PTB, we have developed two major types of on-chip power dividers. One type is a two-stage four-way serial–parallel power divider with the transition of coplanar waveguide (CPW) to coplanar stripline (CPS) (see Fig. 1). This type of power divider, which theoretically has quite a wide bandwidth, was first implemented in the programmable Josephson voltage standard (PJVS) by the AIST voltage standard group in Japan [12]. We developed a completely new version of this divider, to adapt it to pulse-driven JJ arrays and match it to the structure and dimensions of our carrier and JJ arrays. Each segment of the divider has a geometry and electrical length different from the Japanese design.

Based on the equivalent circuit [13], the power is divided by connecting two parallel 100-Ω CPWs and further divided utilizing two 50-Ω CPSs connected in series, having a combined impedance of 100 Ω. The number of splits is normally 2^n, where n is the number of stages for the power divider. To have the same 50 Ω characteristic impedance of each output port, n needs to be an even integer. Another advantage of this type of power divider is that it saves chip area due to its compact size. The size of our design is about 1078 μm $\times$ 795 μm.

This type of power divider does not have any frequency-dependent components. Therefore, the transmission coefficient is very smooth over a wide range of frequency and it shows no resonance frequency [12]. Different layouts were completely numerically simulated in the commercial three-dimensional electromagnetic simulation software CST Microwave Studio.[1]

The following parameters were defined in the simulation (see Table I). We used the magnetic boundaries to model the power dividers because the real chip is operated in a cryoperm shield. To identify the thin layer and avoid short circuit between the layers, the mesh cells were defined quite fine, which can cause a long simulation time, but it would give us accurate results. For each port of the divider, a structure must be defined, which guides and propagates the electromagnetic wave in order to calculate the S-parameter results in CST. In the waveguide setup, the input port 1 and output ports 2–5 of the serial–parallel power divider were defined. Unlike the Wilkinson power divider, there is no isolation resistor between the output ports. By using the S-parameter sweep, the layout structure was simulated and optimized. In Fig. 3, the simulation results show that the transmission coefficients are close to the theoretical value of –6 dB and the reflection coefficient S_{11} is smaller than –20 dB. These results were comparable to the design from AIST [12]. Furthermore, the transmission coefficients are identical: $S_{21} = S_{51}$ and $S_{31} = S_{41}$, because the structure we designed is symmetrical. In addition, S_{21} and S_{51} of this power divider have a 180° phase shift compared to S_{31} and S_{41}. Such a phase difference is quite critical to the experimental setup, which is discussed later.

[1]Commercial equipment is identified in this article to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by PTB.

TABLE I
MATERIAL DEFINITION AND THICKNESS OF EACH LAYER OF THE POWER DIVIDER (PEC: PERFECT ELECTRIC CONDUCTOR)

Layer	material	Thickness (μm)
Nb wiring	PEC	0.6
SiO_2 insulator (ε_r=4)	SiO_2	0.4
Nb vias	PEC	0.4
Nb base electrode	PEC	0.16
Si substrate (ε_r=11.9)	Silicon	380

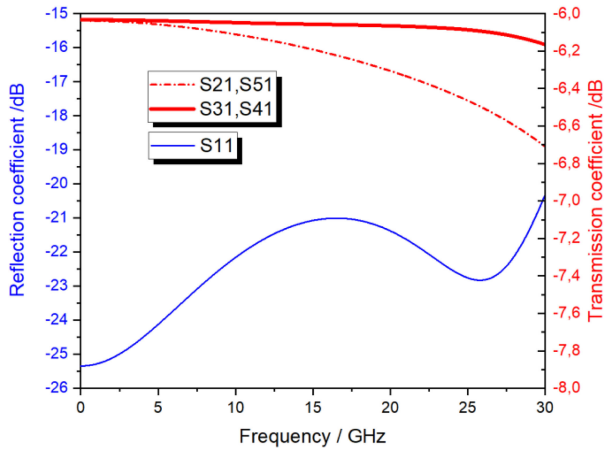

Fig. 3. Simulation results of a two-stage serial–parallel power divider.

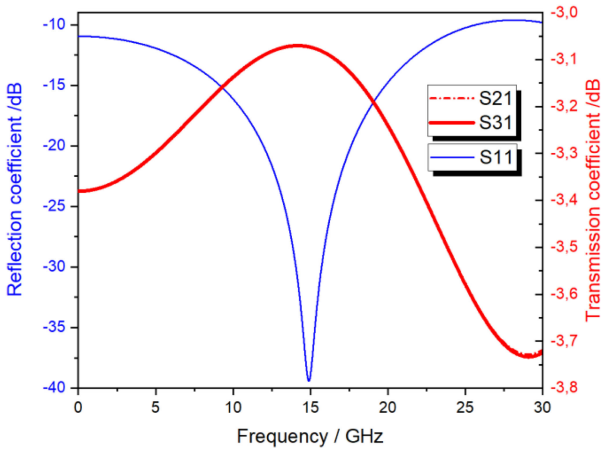

Fig. 4. Simulation results of a one-stage Wilkinson power divider.

The second type is a one-stage Wilkinson power divider with CPS and CPW right-angle bending [14], [15] (see Fig. 2). The NIST voltage standard group has designed a broadband compact Wilkinson power divider using lumped microwave elements [10]. This special type of power divider was first successfully implemented in PJVS circuits and later also in JAWS circuits [11]. We designed a different version of this divider using a one-fourth λ resonator. The size of our conventional Wilkinson power divider is 1900 μm $\times$ 1500 μm, which is larger than the NIST's design. Its bandwidth is narrower than that of serial–parallel power dividers. However, due to its simplified structure, it is quite easy to design and fabricate. In the simulation, the simulation and parameter settings remain the same as the serial–parallel power divider. In the waveguide setup dialogue, the input port 1 and output ports 2–3 were defined. The Wilkinson power divider has an isolation resistor between the output ports to prevent that the reflected waves come back toward the input port and degrade the performance. According to the simulation results in Fig. 4, the transmission coefficients are very close to –3 dB and the reflection coefficient S_{11} is very small at the center frequency. It has a good matching at a wide frequency range from 10 to 20 GHz. For this power divider, there is no phase shift between S_{21} and S_{31}.

Each output of the power dividers is equipped with an extra on-chip dc-block capacitor (metal–insulator–metal structure) and a JJ array. Here, we use SNS-type junctions with barrier material Nb_xSi_{1-x} for the series array in JAWS [16], [17]. Nb_xSi_{1-x} is chosen for the barrier material to achieve a higher characteristic frequency f_c at a lower critical current density j_c. Each array (500 junctions for each parallel arm) was integrated with low pass *LR* filters [18] and terminated by matched lumped resistors. The nonstacked SNS JJs were embedded into the center conductor of the CPW. The wafer designs with two identical layouts on each chip were completed in the Design Workshop Technology dw-2000 software.[1]

III. Fabrication of JAWS Chips

The circuits were fabricated in the clean room center of PTB on 3-in Si wafers. On top of the thermally oxidized SiO_2 layer, an additional thin Al_2O_3 layer was sputtered as an etching stop layer. Then, the SNS trilayer of Nb–Nb_xSi_{1-x}–Nb was deposited by sputtering. The Nb_xSi_{1-x} barrier has a thickness of about 30 nm with an Nb content of about 20% and is deposited in a cosputter process (cf., [8]).

A standard window process was applied, which is described in more detail in [8] and which is composed of four major tasks: first, the definition of the JJs; second, the patterning of the Nb-base electrode; third, the deposition of the SiO_2 layer for insulation by plasma-enhanced chemical vapor deposition and opening of the vias; and fourth, the series connection by an Nb wiring. Besides that, two small additional tasks need to be fulfilled in the end: the definition of AuPd resistors by lift-off and opening of bond-pad windows by dry-etching. The whole process comprises the following steps: five depositions, five etching steps, six electron-beam lithography steps, one lift-off. The most crucial step in each major task is the dry etching by reactive-ion etching with inductively coupled plasma. It determines the thickness and the final layout of the structure on the wafer. After each etching step, the wafer is carefully investigated by scanning electron microscope, to make sure that the process was completely performed and no failures or residues from the e-beam resist or the etching process was left on top of the processed structures.

IV. Experimental Setup

Preliminary measurements were performed at low temperatures of 4.2 K in a measuring setup, which is based on the PTB's eight-channel JAWS setup. As described in [8], in the JAWS systems the desired waveforms are encoded by $\Sigma\Delta$ analog to digital conversion. These codes were transferred to the PPG (Sympuls BPG30G-TERx8[1]). The commercially eight-channel-ternary PPG delivers a high-speed digital sequence of bipolar current pulses with a maximum clock frequency of 15 GHz for the return-to-zero pulses. The outputs of the PPG were combined with the broadband pulse amplifier (Picosecond 5882[1]) with a gain of +16 dB. The digital pulses were transmitted to the JAWS chips through broadband RF cables at room temperature and semirigid RF cables (mounted in the cryoprobe) to low temperatures.

The JJ arrays at the chip were operated using the ac-coupled bipolar bias technique [19]. Each JJ array was provided with a three-level digital data signal and a low-speed compensation bias current signal. In our measurements, we need four compensation signals for the chip with a two-stage serial–parallel power divider containing four series arrays of JJs and two compensation signals for the chip with a one-stage Wilkinson power divider containing two series arrays of JJs. The compensation current signals deliver the low-frequency part of the pulse pattern, which is not transmitted through the RF lines because of the dc blocks and were provided for each JJ array from the arbitrary waveform generators (Agilent 33522B[1]), decoupled from the ground, through coaxial low-frequency cables. The frequency of the arbitrary waveform generator compensation is therefore the same as the synthesized signal frequency. The output waveforms were measured using a digitizer (National Instruments PXI-5922[1]).

A two-channel cryoprobe has been assembled with two semirigid high-frequency cables connected to two channels of the eight-channel PPG. Eight coaxial low-frequency cables for the compensation currents and two coaxial cables for the output voltage were required. The JAWS chip was mounted on a special-made PCB carrier and operated in a cryoperm shield at 4 K. To obtain the total voltage, all the JJ arrays were connected in series with superconducting wires (on-chip). As previously indicated in Section II, the output ports of the serial–parallel

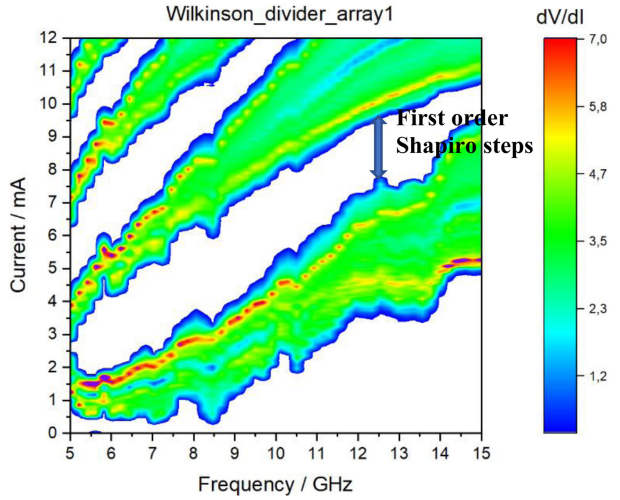

Fig. 5. Frequency dependent behavior for one of the test arrays containing 500 JJs integrated with the Wilkinson power. The width of the first order Shapiro steps is significantly larger than 1 mA over a wide frequency range at a fixed pulse amplitude.

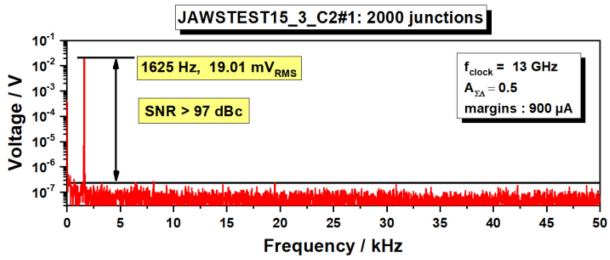

Fig. 6. Frequency spectrum of the test chip with the two-stage serial–parallel power divider and 2000 JJs ($f_{\mathrm{AC}} = 1.625$ kHz, $V_{\mathrm{rms}} = 19.0$ mV, $m = 2000$, $f_{\mathrm{clock\text{-}PPG}} = 13$ GHz, $\mathrm{A}_{\Sigma\Delta} = 0.5$).

power divider have a 180° phase shift. Therefore, to operate all JJ series arrays on one common Shapiro step, we need to set up the correct value of the compensation phase to each parallel array segment.

V. Results

First, we characterized the series arrays of JJs under DC bias. Our results show that without the pulse input all JJs on the arrays were properly biased at 4 K. The critical current is about 3–4 mA. An important investigation of the power dividers is their real pulse drive operation, when connected to series arrays of JJs. By feeding the return-to-zero pulses ($\leq$15 GHz, or $\leq$30 Gb/s) from the PPG to the arrays, the first-order Shapiro steps were clearly formed with sufficient step widths for both types of power dividers. Fig. 5 shows the measurement result of one of the test arrays integrated with Wilkinson power divider. The white area indicates that: $dV/dI = 0$. The first-order Shapiro steps were homogeneous and wide enough ($>$ 1 mA) over 5–15 GHz. The narrower Shapiro step at the beginning was caused by the excessive pulse amplitude. The other integrated parallel test array also shows a comparable performance.

As shown in Fig. 6, the chips with the two-stage serial–parallel power dividers and 2000 JJs are operational up to a maximum clock frequency of 13 GHz, providing good operation margins of 900 μA. With a total number of 2000 JJs, we synthesized

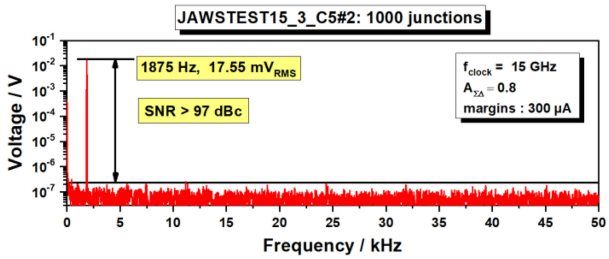

Fig. 7. Frequency spectrum of the test chip with the one-stage Wilkinson power divider and 1000 JJs ($f_{\mathrm{AC}} = 1.875$ kHz, $V_{\mathrm{rms}} = 17.6$ mV, $m = 1000$, $f_{\mathrm{clock\text{-}PPG}} = 15$ GHz, $\mathrm{A}_{\Sigma\Delta} = 0.8$).

a bipolar output voltage of 19.0 mV (rms); higher harmonics are not visible in the noise floor at –97 dBc. However, due to the limited performance of the pulse amplifier, for higher clock frequencies the pulse power is not sufficient to achieve maximum Shapiro step widths and consequently spectrally pure waveforms are not possible anymore. In comparison, when chips with the one-stage Wilkinson power divider and 1000 JJs were also operated at 13 GHz clock frequency with 50% code amplitude, it has a current operation margin of 1000 μA. These chips integrated with the one-stage Wilkinson power divider can be operated up to the maximal PPG clock frequency of 15 GHz. With a total number of 1000 JJs, the spectrally pure sinusoidal waveform of 17.6 mV (rms) was generated (see Fig. 7). Again, higher harmonics are not visible in the noise floor at –97 dBc.

VI. Conclusion

Two types of power dividers were successfully developed and integrated in JAWS test circuits. The array size was here limited to 1000 JJs (Wilkinson power divider: 2 $\times$ 500 JJs) and 2000 JJs (serial–parallel power divider: 4 $\times$ 500 JJs), respectively, to better compare the performance of the power dividers. When operated at 4 K, we synthesized rms output voltages up to 19.0 mV with these circuits driven by a single PPG channel. The test chips with the two-stage serial–parallel power divider and 2000 JJs could be operated up to a pulse repetition frequency of 13 GHz and a code amplitude factor $A_{\Sigma\Delta}$ of 0.5. This is caused by the limited pulse power due to the limited performance of the pulse amplifier. The chips with the one-stage Wilkinson power divider and 1000 JJs exhibited a very good result up to the maximum PPG clock frequency of 15 GHz. To further increase the output voltage of the circuits, our next step will focus on integration of multistacked JJs in each series array and development of an optimized broadband two-stage Wilkinson power divider. To provide sufficient power for higher voltages and clock frequencies, it is planned to use a new broadband pulse amplifier in the test system. To sum up, with the help of on-chip power dividers the number of RF cables between room and cryogenic temperature has been reduced. The integrated circuits with both types of power dividers deliver very promising results. Therefore, we will further improve the layout of our chip design for higher output voltages implementing both types of power dividers.

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