

Optimization of Transition Edge Sensor Arrays for Cosmic Microwave Background Observations With the South Pole Telescope

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Abstract—In this paper, we describe the optimization of transition-edge-sensor (TES) detector arrays for the third-generation camera for the South Pole Telescope. The camera, which contains $\sim 16\,000$ detectors, will make high-angular-resolution maps of the temperature and polarization of the cosmic microwave background. Our key results are scatter in the transition temperature of Ti/Au TESs is reduced by fabricating the TESs on a thin Ti(5 nm)/Au(5 nm) buffer layer and the thermal conductivity of the legs that support our detector islands is dominated by the SiO_x dielectric in the microstrip transmission lines that run along

Index Terms—Transition edge sensors, superconducting detectors, bolometers, cosmic microwave background, South Pole telescope.

Manuscript received September 7, 2016; accepted December 8, 2016. Date of publication December 15, 2016; date of current version January 10, 2017. The South Pole Telescope was supported in part by the National Science Foundation under Grant PLR-1248097, in part by the U.S. Department of Energy, in part by the Argonne National Laboratory and the Center for Nanoscale Materials, an Office of Science user facility, were supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract DE-AC02-06CH11357, in part by the NSF Physics Frontier Center under Grant PHY-1125897 to the Kavli Institute of Cosmological Physics, University of Chicago, in part by the Kavli Foundation and the Gordon and Betty Moore Foundation under Grant GBMF 947. NWH acknowledges additional support from the NSF CAREER under Grant AST-0956135. The McGill authors acknowledge funding from in part by the Natural Sciences and Engineering Research Council of Canada, in part by the Canadian Institute for Advanced Research, and in part by the Canada Research Chairs program.

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TASC.2016.2639378

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I. INTRODUCTION

CURRENT cosmic microwave background (CMB) [1], [2] experiments aim to precisely measure the CMB polarization, especially the parity-violating B-mode polarization [3], with the goal of measuring the energy scale of inflation, the number of neutrino species, and the sum of masses of neutrinos [4], [5]. The measurements require exquisite sensitivity, which means large-format cameras with many bands for removing foreground signals [6]. One such camera, which is being built for the next-generation experiment on the South Pole Telescope (SPT-3G) [7], has 2690 pixels, each with 6 transition-edge sensor (TES) detectors [8], [9] measuring 2 linear polarizations in 3 bands, and will be deployed at the end of 2016.

In this paper, we describe the optimization of the TES detector arrays for SPT-3G. The TES critical temperature (T_c) distributions of wafers prepared by two different detector fabrication processes and two different TES film structures have been systematically investigated. The result shows that the TES performance becomes more controllable if the TES is prepared on an unetched surface with a thin Ti(5 nm)/Au(5 nm) buffer layer. It is worth to mention that the main target of this work is the T_c scattering over the wafer rather than the absolute values. The thermal link, a LSN (low-stress silicon nitride)/Nb/SiO_x/Nb quadruple layer structure, is another critical component for the detector array. Two test wafers were fabricated to investigate the detailed thermal link properties as functions of the film structure and the leg dimensions. We found that the thermal conductance is approximately linearly dependent on the leg width-to-length ratio

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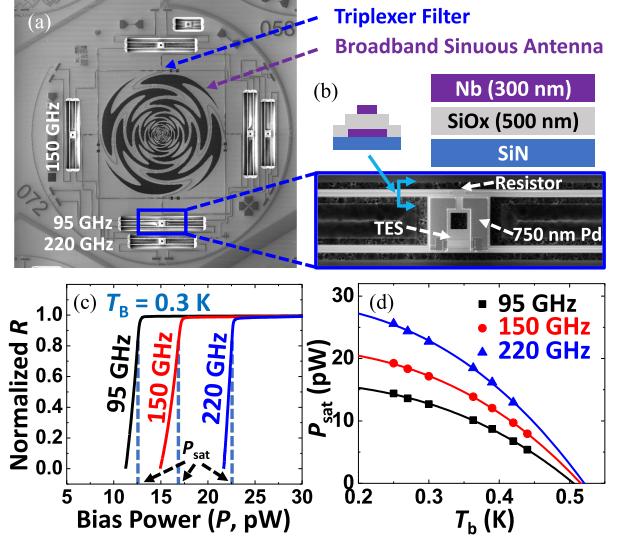


Fig. 1. (a) SEM image of a pixel. (b) Detail around the island. All TESs are with a dimension of $15 \mu\text{m} \times 80 \mu\text{m}$ in this paper. The sketch shows the cross-section of a leg. The LSN layer was $1 \mu\text{m}$ before processing and it will be thinner in the final devices. (c) TES resistance as a function of the P_{tot} for different bands. (d) P_{sat} as a function of the bath temperature T_b : measurements (points) and predicted trend (solid curves).

in our detector arrays, and the LSN contributes approximately 30% of the total thermal conductance of the whole leg. These results provide important information for improving the overall sensitivity of the detector array.

The paper is organized as follows: Section II gives an overview of the detector fabrication and characterization, Section III describes the TES performance with different substrate surfaces and film structures, and Section IV describes an investigation of the thermal link properties.

II. DETECTOR DESIGN AND CHARACTERIZATION

A. Design

The SPT-3G camera has 10 hexagonal detector arrays, each containing 269 pixels. Fig. 1(a) shows the details of a pixel. The millimeter-wavelength signal is received by a self-complementary, log-periodic, broadband, sinuous antenna [10], [11]. Three-pole, quasi-lumped-element filters [12]–[14] split the signal into three bands centered around 95, 150 and 220 GHz. Superconducting, 10Ω , Nb, microstrip, transmission lines [15] distribute the balanced signal for each band to the appropriate detector island, where it is absorbed by a 20Ω Ti/Au load resistor. The change in temperature of the island is then sensed by a Ti/Au TES. A 750 nm thick layer of Pd is deposited on the island to increase the heat capacity and stabilize the detector [16]. The thermal link of the TES detector is a set of four LSN legs that support the island. The leg length and width is designed to provide a detector saturation power (P_{sat}) roughly 2.5 times the expected loading (P_{load}) from the sky, telescope, and cold optics. Detailed information about the island and the leg are shown in Fig. 1(b). Fabrication details for the SPT-3G detector arrays are given in Posada *et al.* [17], [18].

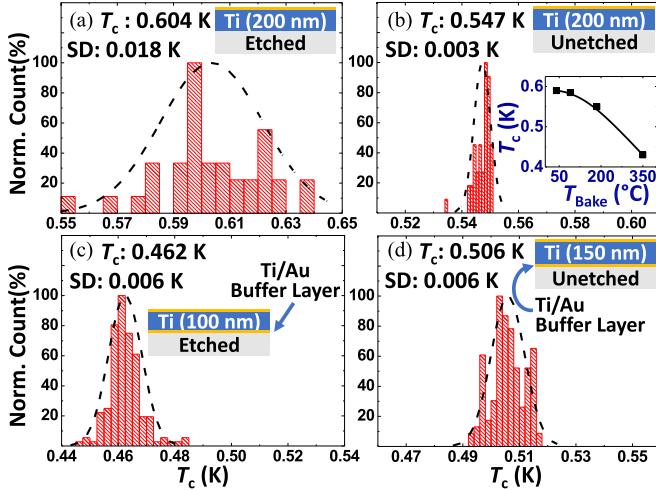


Fig. 2. T_c distribution for TESs (a) on etched SiO_x , (b) on unetched SiO_x , (c) with $\text{Ti}(5 \text{ nm})/\text{Au}(5 \text{ nm})$ buffer layer on etched SiO_x , (d) with $\text{Ti}(5 \text{ nm})/\text{Au}(5 \text{ nm})$ buffer layer on unetched SiO_x . TES T_c change as a function of the baking temperature (T_{Bake}) is shown in the insert of (b). The average T_c and standard deviation (SD) are labeled in each figure. All TESs are covered by 20 nm Au in this paper.

B. Characterization

A digital, frequency-domain, multiplexing scheme [19] has been developed to read out groups of 64 detectors using a single pair of wires [20], making it possible to quickly evaluate the performance of large numbers of detectors.

For this work, the detector performance was investigated using measurements of the resistance, (R), versus bias power P for different bath (i.e., wafer or wafer holder) temperatures (T_b) as shown in Fig. 1(c). $P_{\text{sat}}(T_b)$ is indicated by the dashed lines in Fig. 1(c). Values of $P_{\text{sat}}(T_b)$ from Fig. 1(c) can be plotted, as in Fig. 1(d), and fitted to [21]–[23]:

$$P_{\text{sat}} = K \times (T_c^n - T_b^n) \quad (1)$$

where the constant $K = N k A / l$, N is the number of legs, A is the leg cross section, l is the leg length, k is the thermal conductivity of the leg material, and, n is the index for thermal conductivity. The fit yields values of the parameters and the thermal conduction ratio $G(T_c) = dP_{\text{sat}} / dT = n K T_c^{n-1}$. Since the phonon noise equivalent power (NEP) [24] is directly related to G and T_c , it is important to keep P_{sat} within a reasonable range.

Currently in SPT-3G project, the target T_c is 510 mK and the target P_{sat} is 10.6 pW, 16.0 pW and 21.0 pW for 95 GHz, 150 GHz and 220 GHz bands, respectively. These values are equal to twice the expected optical loading during normal operation, assuming an overall optical efficiency of 85%. They may be varied depending on the measured optical efficiency.

III. TES PERFORMANCE

In some SPT-3G arrays, the TESs are fabricated on an etched SiO_x surface [17], while in others, the TESs are fabricated on an unetched surface [18]. The unetched surface gives much lower scatter in T_c , as shown in Figs. 2(a) and (b). It is possible that residual by-products and increased roughness, due to etching SiO_x during fabrication of the Nb microstrip, may

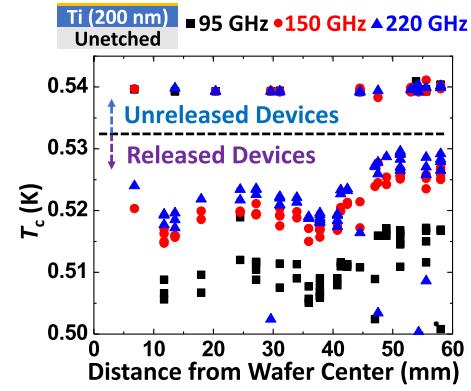


Fig. 3. TES T_c as a function of the distance from the wafer center for unreleased detectors (top panel) and released detectors (bottom panel, the detector legs and islands are released from the Si wafer). Every 4th row of pixelss on this wafer was left unreleased.

cause the large scatter shown in Fig. 2(a). The TESs on etched SiO_x have slightly higher T_c than those on unetched SiO_x , due to the fact that the latter are prepared at a much earlier stage, so they encounter more fabrication processing. Heating during processing reduces the TES T_c , as shown in the inset in Fig. 2(b).

We have also investigated adding a $\text{Ti}(5 \text{ nm})/\text{Au}(5 \text{ nm})$ buffer layer under the TES to isolate the TES from the substrate. The buffer layer results in lower T_c , and lower scatter in T_c , for both etched and unetched SiO_x , as shown in Figs. 2(c) and 2(d). In Figs. 2(c) and 2(d) the combination of the buffer layer and thinner Ti (100 nm for Fig. 2(c) and 150 nm for Fig. 2(d)) gives T_c in the range 450–510 mK, cf. 550–600 mK for the thicker TESs without buffer layer in Figs. 2(a) and 2(b).

The small scatter in T_c in Fig. 2(b) may be due to a smaller number of detectors for this measurement (~ 50 for Figs. 2(a) and 2(b), cf. ~ 150 for Figs. 2(c) and 2(d)) or variations in the etch that releases the detector legs and islands from the Si wafer (releasing process). Releasing decreases T_c , probably due to heating of the TESs, and increases the scatter in T_c , as shown in Fig. 3. Fig. 3 also shows a larger variation in T_c with radius and band. Since these effects are only observed in released devices, they could be due to (i) excess, band-dependent, optical loading in the measurement setup, or (ii) heating of the TESs during release (or during final oxygen plasma cleaning to remove photoresist), which may depend on band because detectors for different bands have different leg lengths with different thermal conductivities. Further investigations are still on going. One plan to further reduce the T_c scattering is to optimize the island releasing process to achieve a more uniform releasing across the wafer.

IV. PROPERTIES OF THE THERMAL LINK

We have fabricated two test wafers to investigate the effects of different film structures (Fig. 4(a-c)) and different leg widths and lengths (Fig. 4(d-f)), respectively. Fig. 4(a-c) shows results for detectors with (a) legs that have only LSN and Nb leads for reading out the TESs (black squares), (b) legs with LSN, the 500 nm SiO_x dielectric for microstrip transmission line and Nb

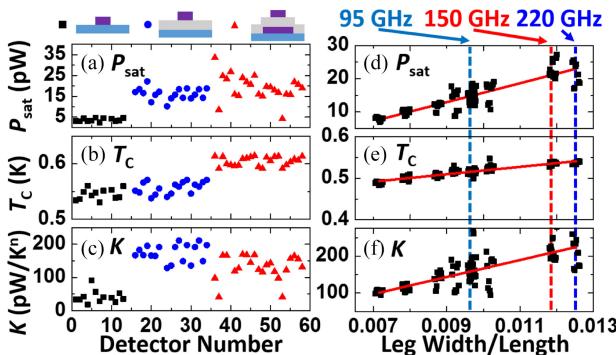


Fig. 4. Detector parameters for different leg film configurations (a)–(c), and different leg widths and lengths (d)–(f). For these measurements, $T_b = 300\text{ mK}$. The detectors in (a)–(c) are dark (no load resistors on the islands).

leads (blue dots), and (c) legs that have LSN and a complete microstrip transmission line (red triangles). K for detectors with only LSN and Nb leads is 3 times smaller than for the other configurations, and the microstrip Nb ground layer has little effect on K , as expected for a superconductor, so the thermal conductivity of the legs must be dominated by the SiO_x layer, with the LSN contributing only $\sim 30\%$.

Since the SiO_x layer thickness is constrained by the filter design, and the LSN layer on the legs must be thick enough to support the island without breaking, changes to the leg thermal conductivity may require a different leg width or length. Fig. 4(d–f) shows measurements of detectors from a wafer on which $\frac{1}{4}$ of the detectors have 23% longer legs and $\frac{1}{4}$ have 26% narrower legs. A complete discussion of these results is outside the scope of this paper (more discussion about thermal link can be found in [25], [26]) and the origin of the scattering of K in our results is still under investigation. However, it is clear that K is approximately proportional to the ratio of leg width to leg length (W/L), as expected for long legs. The scaling of K with W/L also suggests that the islands and legs are fully released, i.e., the legs are the only thermal link between island and the substrate. A touch between island and the substrate would give a higher K for long and narrow legs than the observed results.

V. CONCLUSION

In summary, we have shown that adding a thin Ti(5 nm)/Au(5 nm) buffer layer under a Ti/Au TES significantly decreases the scatter in transition temperature. We have demonstrated that the thermal conductivity of the legs that support the SPT-3G detector islands is dominated by the SiO_x microstrip dielectric layer, and that the thermal conductivity scales as expected with leg width/length. These results will be used to optimize the performance of the TES detector arrays for the new SPT-3G camera.

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