A Sub-Threshold Microwave RFID Tag Chip, Compatible With RFID MIMO Reader Technology

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Abstract—We present a fully integrated radio frequency identifications transponder chip operating at 5.8 GHz, which is compatible with the class-1 generation-2 of the Electronic Product Code protocol (EPC-C1 G2). The tag chip including the analog front-end and the digital baseband processor, are designed in the sub-threshold regime (0.5 V) with a total supply current of less than 50 μA. As a power scavenging unit, a single-stage differential-drive rectifier structure is designed and fabricated with standard threshold voltage (SVT) MOS elements in a commercial 65-nm CMOS process, to provide 0.8 V of rectified voltage. Measurements performed on the fabricated single-stage structure show a maximum power conversion efficiency of 69.6% for a 22 kΩ load and a sensitivity of –12.5 dBm, which corresponds to more than 1 m of reading range. The power conversion efficiency at this range is about 64%.

Index Terms—Wireless power transfer (WPT), wireless energy transfer (WET), Internet of Things (IoT), industry 4.0, passive RFID, MIMO/MISO reader, microwave RFID transponder, RF energy harvesting, dynamic threshold cancellation techniques, power/voltage conversion efficiency, sub-threshold design.

I. Introduction

INDUSTRIAL Internet of Things (IIoT) paradigm, defined as the technology enabling the interconnectivity of devices and instruments to each other and to the already existing Internet infrastructures can create a network of smart objects capable of knowing, sensing the environment, interacting, and cooperating in collecting, distributing, manipulating, and processing data. This ambient intelligence can substitute the need for a human operator for control and maintenance. In this sense, passive Radio Frequency Identification (RFID) technology is considered as a cost-effective method for automated information gathering and data processing, offering uniquely identifiable/addressable tags with sensing and communication capability under non-line-of-sight (NLOS) conditions, high sustainability, moderate circuit complexity and small size,

which are quite advantageous in applications such as, IoT/IIoT, wireless sensing and Industry 4.0 [1].

From the perspective of system and circuit design, however, the implementation of passive RFID systems for such applications necessitates the consideration of various emerging and advanced technologies and solutions including Wireless Sensor and Actuator Networks (WSAN), Wireless Power Transfer (WPT) and Energy Harvesting (EH). It is, therefore, necessary to initially investigate the features of passive RFIDs at different allocated frequency bands, and then navigate through the wireless power transfer mechanisms and energy harvesting techniques at these reading ranges and frequency bands, using the system and circuit level analyses.

During the evolution of RFID-based technologies, a wide range of frequencies inside and outside of the Industrial, Scientific and Medical (ISM) radio bands has been allocated and licensed for these applications, which are categorized in four different transmission bands of Low Frequency (LF) at 125-134 kHz, High or Radio Frequency (HF/RF) at 13.56 MHz, Ultra High Frequency (UHF) at 860-960 MHz, and microwave band at 2.4 GHz or 5.8 GHz. In this definition Medium Frequency (MF) and Very/Super High Frequency (VHF/SHF) bands are merged with the others. The usable frequency range in each band, and further associated regulations on power and data rates is adapted based on the regional guidelines [2], [3].

With the large wavelength of 2400 m to 22 m in the RFID transponders at LF and HF bands, generally several rounds of coil antenna are required for proper functioning, and the transponders work passively only in the near-field regime and within small distances from the reader [4]. UHF RFID tags exhibit long-range identification capability [5], [6], [7], [8], [9], [10], however the size of the antennae at UHF range can limit the applicability, if it is desired to attach or implant the RFID chip into a small target object. Governed by the radiative behavior of the signal at far-field regime, the performance of RFID tags at microwave bands are rather similar to UHF, however, with the wavelength decreasing roughly from 100 cm to around 5 cm in the microwave electromagnetic spectrum, the antenna design is uncomplicated, and the dimensions barely cause an issue. Beside the small antenna size at microwave band with shorter wavelengths, wireless power transfer with enhanced efficiency is achievable owing to significant electromagnetic "wave focusing" using directional antennae. Furthermore, in industrial applications, state-of-the-art UHF RFID technologies often fail in severe multi-path fading conditions. Switching to a higher frequency does not avoid interference, however, the higher available bandwidth
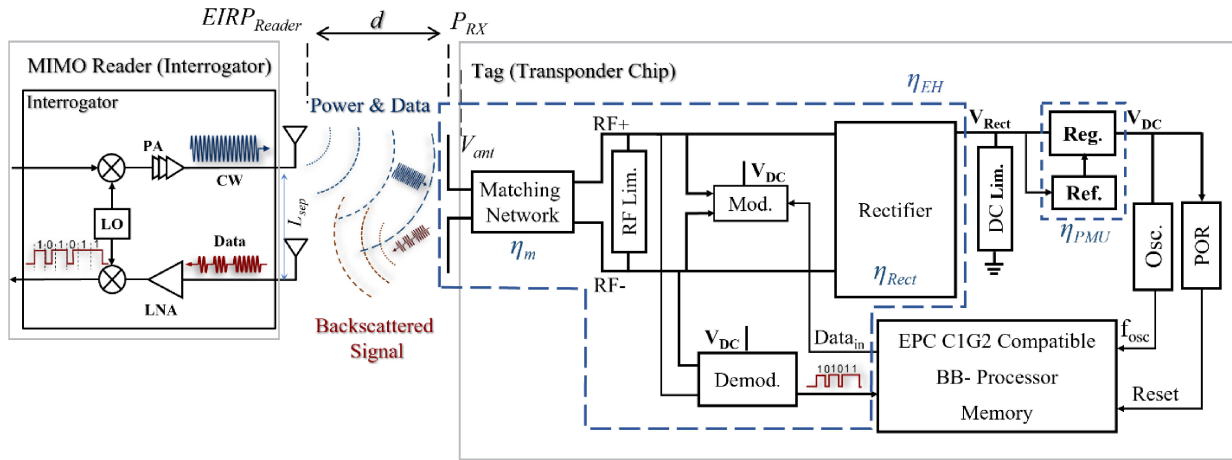
Fig. 1. Figurative representation of the RFID system building blocks [11].

can be used to counteract the detuning of the tag antennae and shift the dead zones while allowing for compact Multiple Input Multiple Output (MIMO) readers. However, the higher attenuation of the electromagnetic (EM) energy with distance, mediocre penetration through objects due to skin effect, and the typical challenges of high frequency electronic design are the main sources of design complexities and limitations in this frequency range [11].

As a practical scenario, in this paper, an RFID-based machine tool monitoring system is proposed for monitoring tool usage in Computer-Numerical-Controlled (CNC) machines. Instead of UHF bands, the system is designed for the unlicensed ISM band at 5.8 GHz. This ensures a smaller tag size compatible to CNC tools and enables a compact multi-antenna MIMO reader, which allows for a robust tag detection even under severe multi-path fading in manufacturing environments. The fully integrated RFID tag chip including the Analog Front-End (AFE) and the digital baseband processor, is purely passive and supplied by the transmitted EM wave from the reader, which dictates a rather different design approach in system and circuit level, compared to the conventional transceiver structure. According to the principles of passive system design, the most power-hungry elements of a generic transmitter (i.e., mixers and power amplifiers) are replaced by a backscattering mechanism. Hence, it is necessary to have a comprehensive system level analysis for the power-up and data communication phases, considering the governing principles of the backscatter radio communication [12].

Furthermore, an accurate assessment of the power gains and losses in a communication system has to be performed not only to guarantee the successful transmission and reception of the data across the wireless link, which is the typical purpose of a link-budget analysis, but also to ensure the successful power-up process of the tag's integrated circuit. The latter issue relates to the design of a highly efficient energy harvesting topology and the optimization of the total power dissipation of the system. According to the detailed literature review performed in [11], and the analysis presented in [13], [14], [15], a single stage of the Differential-Drive Rectifier (DDR) structure with dynamic threshold cancellation technique, presented in [16] is adopted for the implementation

of the power scavenging unit. The DDR topology working based on the full-wave bridge rectifier structure introduced by Facen and Boni in 2006 and as a power retrieving circuit for passive UHF RFIDS, is a prevalent solution for efficient high frequency rectification and provides a purely passive solution compatible with commercial Complementary Metal Oxide Semiconductor (CMOS) technologies without requiring any external or auxiliary components [17], [18], [19], [20]. A detailed analysis of the structure is provided in Section III.

The generated voltage from a single-stage DDR is, however, not compatible with the existing 1.2 V standard logic cell library of the commercial 65-nm CMOS process used for the implementation. Therefore, a new set of the logic gates required for the implementation of the digital baseband processor of the transponder chip is designed and characterized for operation as a custom-designed sub-threshold standard-cell library. The details of the design procedure and considerations for the matching network, energy harvester, Power Management Unit (PMU) with the regulator and reference-voltage generator, and the Data Management Unit (DMU) with the modulator and demodulator, are presented in the next sections.

II. SYSTEM ARCHITECTURE AND OPERATION PRINCIPLE

Fig. 1 shows the concept of MIMO passive RFID, and the detailed block diagram of the transponder chip, including the AFE, control logic compatible with Electronic Product Code (EPC) protocol in UHF range, and the memory. In the absence of supply voltage or battery, the passive RFID at 5.8 GHz works in far-field regime and the link-budget can be analyzed using Friis' transmission equation. It must be mentioned that for a MIMO and consequently a Multiple Input Single Output (MISO) system, the near-field to far-field boundary occurs at a shorter distance compared to a single antenna implementation. And this shift in the boundary is correlated to the separation distance of the multi-antennae structure. For a large separation distance (approx. at $L_{sep} > \lambda$), the MIMO system performs similar to a single antenna structure. If the separation distance decreases, the far-field boundary shifts toward the transmitter antenna. The lower limit of L_{sep} is of course the point

where the mutual coupling dominates the performance of the transmitting antennae. Consequently, if the far-field condition is valid for a single antenna system, it is also applicable to the corresponding MIMO/MISO systems implemented with the very same antenna dimensions and wavelength. It means, evaluating the far-field criteria assuming a Single Input Single output (SISO) system ensures the operation of the MISO system in the far-field regime [21], [22].

The process of generating a stable supply voltage (V_{DC}) to power up the chip from the available RF power in the tag antenna (P_{RX}) includes a path of matching network, rectifier, and regulator, which are introducing additional inefficiency factors. Adding the harvesting efficiency factor (η_{EH}) into the Friis' transmission equation, the theoretical communication range can be estimated as:

$$d = \frac{\lambda}{4\pi} \sqrt{\frac{EIRP_{Reader} \cdot G_{Tag} \cdot \eta_{EH}}{P_{Tag}}}, \qquad (1)$$

where, G_{Tag} is the antenna gain, P_{Tag} is the total power consumption of the tag, and λ is the wavelength of the RF incident wave.

Considering the limited maximum EIRP and antenna gain, an initial conclusion from (1) is that the tag harvesting efficiency (η_{EH}) and power budget requirements (P_{Tag}), are the factors directly affecting the communication distance d. However, comprehensive system analyses in [11] suggest that the V_{DC} requirements of the tag exhibit an even stronger influence on the communication distance and the sensitivity of the system. In other words, implementing the whole transponder chip in sub-threshold regime, not only allows for ultra-low-power operation of the AFE (lower P_{Tag} and V_{DC}), but also enhances both the rectifier and matching network efficiencies, caused by lower losses in the rectifier and higher Q-factor, respectively [13], [23]. The latter issue will be further discussed in Section III-A, along with the efficiency analysis of the system, and the rectifier as the core of the harvester unit.

III. CIRCUIT DESIGN AND IMPLEMENTATION

In the following, the design strategy for the AFE, including the harvester, power management unit, modulator, and demodulator, is presented.

A. Matching Network and Harvester

Prior to the design of the full tag chip, a differential-drive rectifier test chip was designed and fabricated in 65-nm CMOS process. Investigation of the system characteristics in [13], [14] reveals how shrinking the supply voltage to 0.5 V improves the efficiency and sensitivity, as only a single stage of the DDR is sufficient for rectification.

The goal is to achieve the rectified voltage of 0.8 V for a 22 kΩ load, representing the full chip power requirements. According to (1) and given a 5.8 GHz incident RF signal with an EIRP of 4 W, this condition allows the possible operation of a tag chip consuming nearly 30 μW of power, at a range higher than 1 m, in case a total harvesting efficiency factor (i.e., $\eta_{EH} = \eta_m.\eta_{Rect}$) of more than 50% is realizable. In this,
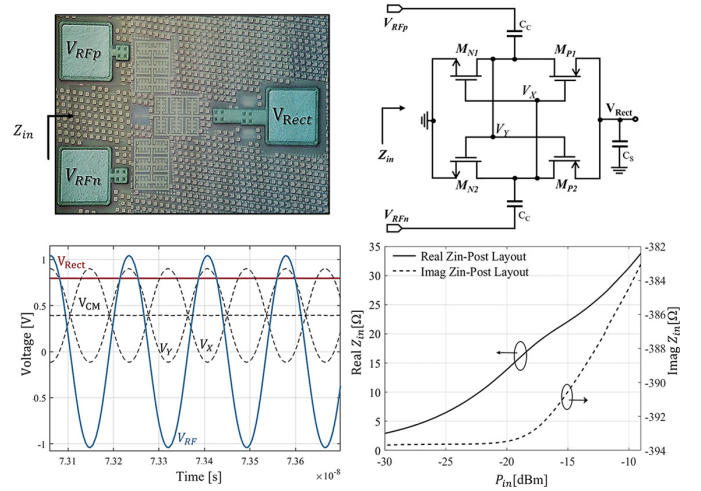

Fig. 2. Schematic, photomicrograph, and post-layout simulation of the fabricated single-stage bridge rectifier [11].

η_m and η_{Rect} represent the efficiency factors of the matching network and the rectifier, respectively.

In case of a perfect matching between the antenna and the harvester input impedance, i.e., $\eta_m = 1$, even a PCE of about 50% is sufficient for the DDR, which is quite feasible according to the literature. However, the nonlinear nature of the rectifier circuit and the variable input power level, makes the conventional conjugate matching strategy more complicated in case of an RFID system. To understand the matter, equation (1) should be rearranged based on the signal amplitude [24].

$$V_{ant} = \frac{\lambda}{4\pi d} \sqrt{2 \cdot R_{ant} \cdot EIRP_{Reader} \cdot G_{Tag}} \qquad (2)$$

with V_{ant} representing the voltage generated from the incident wave across a tag antenna with an input impedance of R_{ant}.

The tag receivable power of 63 μW (–12 dBm) at 1 m distance from the reader, calculated from the forward link-budget analysis according to Friis' transmission equation in [11], could be enough to power up the chip with the mentioned efficiency criteria. Though, a 50 Ω antenna, even with 7 dB gain according to (2), results in a peak open circuit voltage of 177 mV, which is insufficient to overcome the standard threshold voltage barrier of MOS rectifying elements in the applied technology. Hence, an effective input impedance matching for a tag chip must provide the maximum power transfer and the voltage boosting, concurrently.

The voltage boosting is realized if the input impedance of the rectifier is high enough or the chip input impedance exhibits a high Q-factor, resulting in:

$$|V_{RF}| = \frac{|V_{ant}|}{2} \sqrt{Q_{Rect}^2 + 1}. \qquad (3)$$

Enhanced rectifier efficiency can be realized by proper sizing of the transistor pairs in Fig. 2, which by generating a dynamic excessive bias voltage, simultaneously reduces the effective threshold voltage and leakage current of the MOS elements. This condition guarantees the optimized PCE as well as the optimized Voltage Conversion Efficiency (VCE), defined as the ratio of the rectified voltage (V_{Rect}) to the input voltage (V_{RF}).
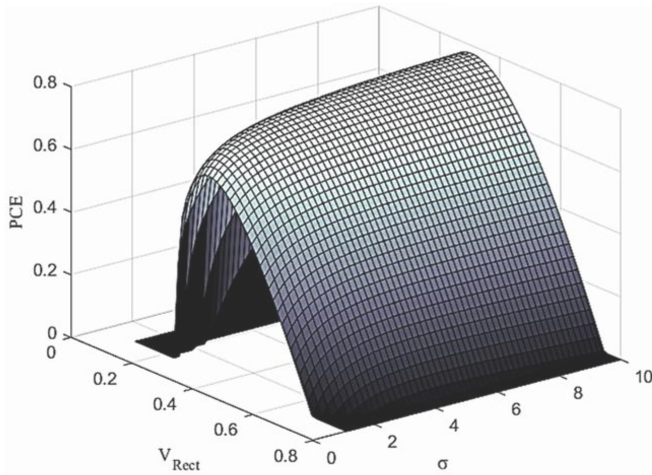
Fig. 3. PCE contour simulation vs σ, and V_{Rect}/VCE.

Fig. 4. Measured and simulated performance of DDR vs. P_{in}.

To perform the optimization, the PCE must be simulated versus the VCE and the parameter σ, which is defined based on the transistor's geometrical characteristics and the process-dependent properties of the employed CMOS technology [11]:

$$\sigma = \frac{k'_n}{k'_p} = (\mu_n \ C_{ox} W_n L_n)/(\mu_p C_{ox} W_p/L_p), \qquad (4)$$

where μ_p, μ_n and C_{ox} are technology dependent properties representing the carrier mobility factors and oxide capacitance.

Analysis of the transistor-level simulation results presented in Fig. 3, which are performed based on BSIM3 transistor model and for a constant input voltage of around 300 mV, reveals that for σ of around 7.5 the value of PCE reaches the maximum of about 0.73 (or 73%), and the output of a single stage DDR is roughly 0.25 V at this condition, which corresponds to a VCE of 80%. Considering a typical value of 2.5 to 3 for the ratio of the mobility factors (μ_p, μ_n), the optimal W/L ratios of the NMOS to PMOS can be defined using (4). It must be noted that, the assumption of 300 mV of input voltage is based on equation (3) and the previous link-budget analysis performed in [14], [24]. In the simulations the source-bulk voltages of 0 V are considered.

The single-stage rectifier structure consumes a total area of $160 \times 155 \ \mu m^2$, excluding the output DC pad. Metal Insulator Metal (MIM) capacitors are employed for the implementation of the coupling and storage capacitors due to the technology fabrication constraints.

On-chip S11 measurement of the fabricated DDR was carried out using the Anritsu Vector Network Analyzer (VNA) and Cascade Infinity GSSG differential RF probe.

Fig. 4 shows the power, and voltage conversion efficiencies and the DC output voltage with respect to the input power P_{in}. The required DC voltage of 0.8 V is achieved at -12.5 dBm for 22 kΩ, which is close to the point where the peak of the PCE curve is attained. Measured input impedance of the rectifier at -12 dBm is 4.7Ω-j51.4Ω, corresponding to a parallel resistance and capacitance of 500 Ω and 0.52 pF, or a Q-factor of 9.5. The full chip, dissipating 30 μW of power, can therefore, operate at a distance of more than 1 m from the MIMO reader.
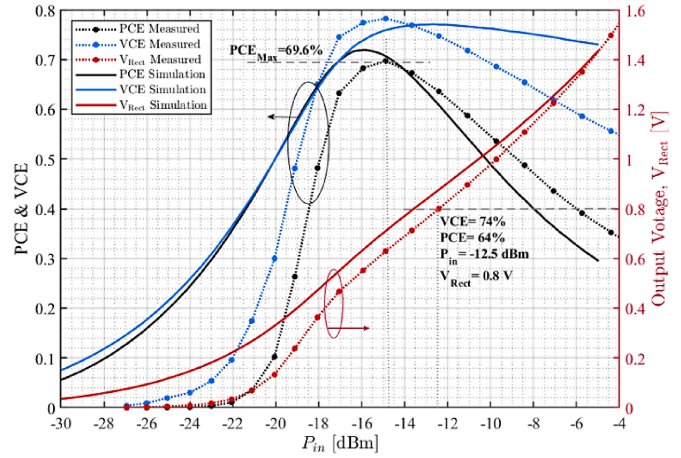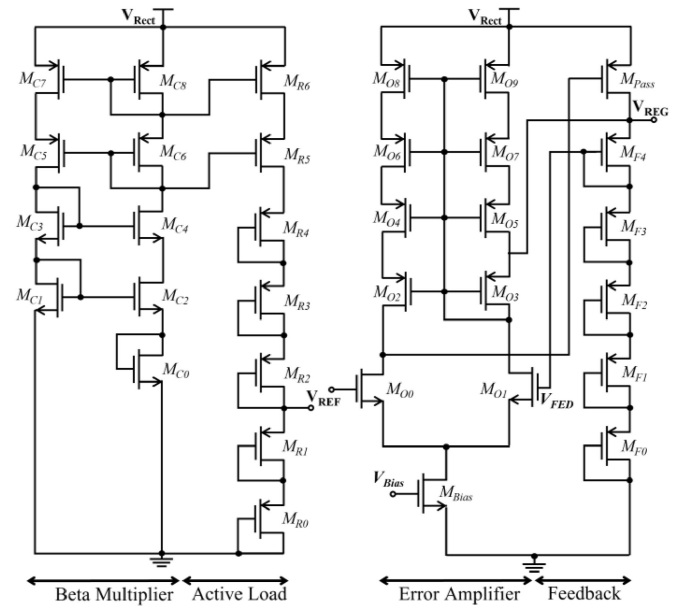

Fig. 5. PMU, including reference voltage generator and LDO.

B. Power Management Unit

The previous discussions revealed that the amount of harvested power and rectified voltage in a passive tag, are strongly related to the variable tag to reader distance and loading conditions of the rectifier, which makes the rectified voltage V_{Rect} a poor choice for a suitable supply voltage. It is, therefore, necessary to design a Low Drop-Out (LDO) voltage regulator to provide a stable output voltage with maximum ripple suppression, independent of the variations in the input voltage V_{Rect}, and the load current.

Fig. 5 illustrates the schematic of the LDO and the required voltage reference generator.

In order to reduce the total power consumption and the chip size, the LDO is designed resistor-free and is operating in sub-threshold region. The transistors are designed to operate in weak- to moderate-inversion based on the threshold voltage of the MOS elements ranging roughly from 0.45 V to 0.65 V. According to the methodology and analysis presented

TABLE I
TRANSISTOR SIZING FOR PMU

Device	Device Characteristics		
	Type	W(μm)	L(μm)
M_{O0} - M_{O1}	NMOS	16	0.28
M_{O2} - M_{O8}	PMOS	1	0.5
M_{F0} - M_{F4}	PMOS	1	0.28
M_{Pass}	PMOS	120	0.28
M_{Bias}	NMOS	1	0.5
M_{R0} - M_{R4}	PMOS	4	0.3
M_{R5} - M_{R6}	PMOS	3	0.3
M_{C5} - M_{C8}	PMOS	10	0.28
M_{C1}, M_{C3}	NMOS	1	0.5
M_{C2}, M_{C4}	NMOS	200	0.28
M_{C0}	NMOS	16	0.5

in [25] and [26] and considering the technology parameters, the Inversion Coefficient (IC) or Factor (IF) could be estimated to be between 0.09 to 0.12 for the core elements of the LDO. With the exponential behavior of MOS sub-threshold current, a higher voltage gain is also expected for the amplifier. Table I provides the information about the sizing of the elements used for the implementation of the LDO block.

The proposed LDO is capable of delivering a constant output voltage of 0.5 V within a range of 0.563 to 1 V and the load current variation of 25 μA, as the power drawn from the regulator could differ significantly in the read and write states of the tag. The error amplifier and the LDO are operating with the quiescent currents of 28 nA and 48 nA, respectively. The minimum drop-out voltage over the pass device is reduced to 0.63 mV, and the overall efficiency of LDO is above 50% with an optimum performance of about 88%. The designed LDO provides a power supply rejection ratio (PSRR) of –49.6 dB up to 1 KHz, and below –30 dB up to 10 KHz.

C. Data Management and Digital Control Units

The reader to tag communication and data transfer must comply with the standard air interface and protocols. ISO 18000-6C describes the communication standards for UHF Class 1 Gen 2. Class 1 structure provides the communication instructions for passive tags. Gen 2 details the air interface protocol and also modulation, encryption, and encoded systems [27].

Owing to its simplicity, Amplitude-Shift keying (ASK) scheme is adopted for both demodulator and backscattering modulator, which have to provide 640 kHz and 160 kHz of data rates, respectively.

Fig. 6.b depicts the schematic of the implemented demodulator. A single stage of DDR with modified size followed by a parallel R and C is used as the envelope detector. R and C are chosen according to carrier frequency f_c and the highest modulation frequency f_m.

The envelope detector is designed to obtain the maximum swing for the lowest input power level. Therefore, in case of higher power levels, the extracted envelope is first limited by
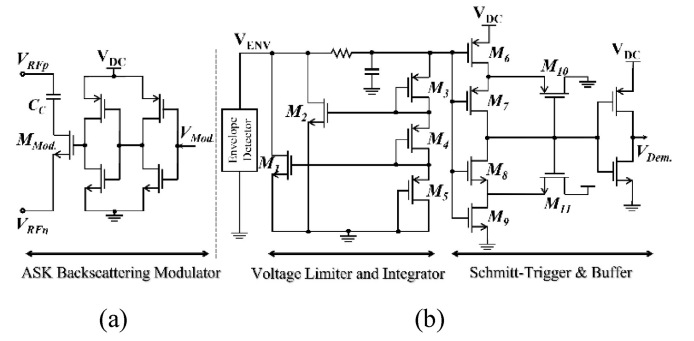

Fig. 6.   (a) ASK Backscattering Modulator (b) Demodulator.

TABLE II
SIZING FOR DMU

Device	Device Characteristics		
	Type	W(μm)	L(μm)
M_1 - M_1	NMOS	32	0.06
M_3	PMOS	8	0.28
M_4, M_5	NMOS	8	0.5
M_9, M_{11}	NMOS	8	0.06
M_6, M_{10}	PMOS	8	0.06
M_7	PMOS	2	0.06
M_8	NMOS	2	0.06

the voltage limiter and then shaped by a low pass filter. The output of the integrator varies for data 1 and 0, depending on pulse width of the Pulse Interval Encoded (PIE) data, which is categorized as logical 1 and logical 0 by the Schmitt-Trigger stage. The complete demodulator block, excluding the DDR, requires less than 5 nW to operate at highest data rate (160 kb/s) and lowest modulation index (0.8).

The ASK backscattering modulator of Fig. 6.a, comprised of inverter stages driving an NMOS switch, is realized in series-parallel configuration due to its advantage at microwave frequency range. Changing the input impedance of the tag chip using the switch, part of the incident wave is scattered back to the reader modulated by the data from the tag. To optimize the performance, the difference between the reflection coefficients of the on and off states of the switch is maximized by increasing the width of the transistor. C_c is added in series with the switch to compensate the parasitic capacitance caused by the larger transistor size.

The sizing characteristics of the main elements of the design are summarized in Table II.

IV. MEASUREMENT RESULTS AND DISCUSSION

The complete tag chip is designed and implemented in a commercial 65-nm CMOS process. The fabricated chip, shown in Fig. 7, consumes an area of 1.2×0.65 mm^2.

The important means to achieve ultra-low-power operation in this work, are the sub-threshold design of all blocks, including the data/power management units (DMU/PMU) and digital control unit at 0.5 V, while using a passive backscattering modulator with almost zero power consumption for signal transmission. The AFE consumes less than 500 nW.
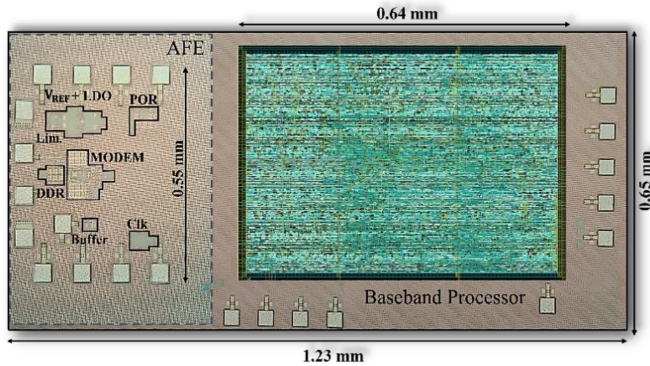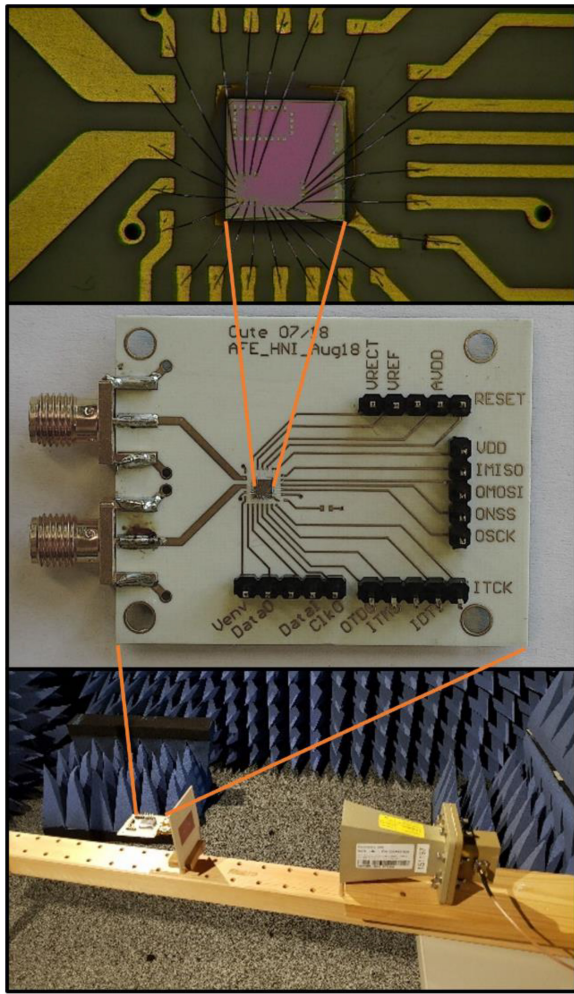
Fig. 7.   Microphotograph of the fabricated tag chip.

TABLE III
PERFORMANCE COMPARISON OF PASSIVE MICROWAVE RFIDS

Ref.	Process	EH Tech.	Sensitivity (dBm)	Load (Ω)	PCE (%)	V_{DC} (V)	Freq. (GHz)
This work*	65-nm	DDR	-12.5	22k	64	0.5	5.8
JRFID [11]*	65-nm	DDR	-12.4	44k	69.4	1.2	5.8
RFIC [10]	0.13-μm	DDR	-26.5	100k-1M	40	0.44	2.4
RFIC [28]	0.18-μm	DDR	-14.22	200k-1.8M	-	1.8	5.8
ISSCC [29]	65-nm	-	-	~3.5k	-	0.6	5.8
ISSCC [30]	65-nm	-	-	8M	-	0.85	5.8
JRFID [31]	0.13-μm	Charge Pump	-11	-	-	0.5	5.8

Fig. 8.   Measurement Setup & bonded prototype.

The measurement setup of Fig. 8 consists of a reader device with EPC-Gen2 baseband processor and custom designed 5.8 GHz analog front-end. Attached there is a standard gain horn antenna with G = 10 dBi and linear polarization providing an EIRP of 36 dBm or 4 W. The RFID chip is bonded to a test-printed circuit board (PCB) with differential RF inputs. A differential feed patch antenna with a gain of 5.7 dBi is matched to the test-PCB inputs with 50 Ohm resistance.

Using this setup, the measured signals of the baseband processor for the realized system are shown in Fig. 9. The signal in Fig. 9.a is measured within the reader after the down conversion and carrier rejection. This baseband signal is converted to the digital domain by an Analog to Digital Converter (ADC) and decoded in the baseband processor of the reader. Fig. 9.b shows the control signal of the modulator and output of the baseband processor, respectively, as well as the data packets (between 0.05 V and 0.35 V) transmitted from the tag to the reader. Due to the crosstalk, the decoded data from the reader is also visible below the baseline. The communication process starts with the query command, and then follows by the response of the transponder with the included random number in the first time slot starting from t=0.0. An acknowledgment from the reader and the transmission of the number, are the next sequences.

Table III provides benchmarking with similar works at microwave band of 2.4 GHz and 5.8 GHz and summarizes the chip performances. Assuming an EIRP of 36 dBm, [10] reaches a 13.5 m range at 2.45 GHz, for less than 2 μW of delivered output power with an external dynamic storage capacitor. In [28], a fully integrated multiband structure offers an operating range of 7.5 cm at 5.8 GHz. A range of 1.5 m is estimated for this chip in far-field regime with external antenna, while delivering only 16.2 μW of power. An RF-powered transceiver at 5.8 GHz with a communication range of 10 cm, using external processor unit and storage capacitor is presented in [29]. Near-field integrated antenna structure in [30], only achieves mm-range of communication. Reference [31] provides a relatively comparable sensitivity of –11 dBm at 5.8 GHz range, in a 130 nm technology and with a fully passive charge-pump structure, however, the AFE chip is limited to a simplified structure including the harvester unit, limiter, and backscattering modulator.

V. CONCLUSION

This paper presented the design and implementation of a fully integrated tag chip to be used for the next generation of passive RFID systems at 5.8 GHz. To fulfill the link budget restrictions at this range, a single-stage cross-coupled differential rectifier is designed and optimized for the sensitivity and PCE performance and the modules of the tag are designed in ultra-low-power, ultra-low-voltage regime. Considering that
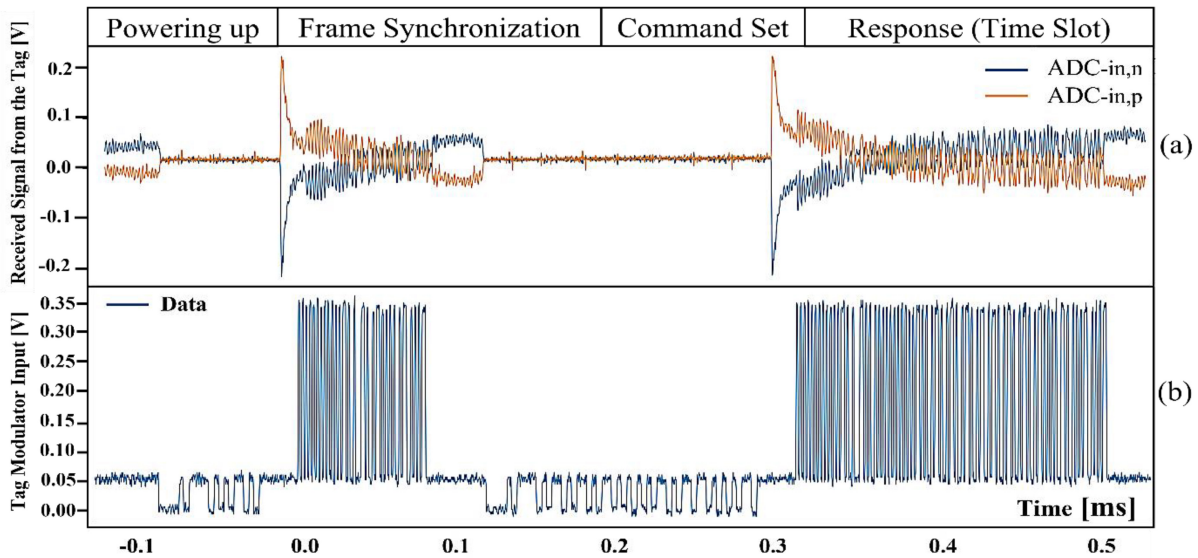
Fig. 9. Measured waveforms of tag-reader communications.

it is generally true to assume the forward-link limit as the overall restricting factor on the reading range of the current passive RFID systems with high power requirements, here only the forward-link budget analysis is presented. The full uplink and downlink analysis are performed in detail in our previous works [13], [14], [15].

To the authors' best knowledge, the presented work is the only RFID transponder chip with fully integrated AFE and processor, achieving 25 cm of reading range at 5.8 GHz, in preliminary measurements. It is worth mentioning that the measurements are performed without accurate matching implementation or relying on optimized antenna gains. From the measurements of the rectifier test chip presented in Fig. 4, and analysis in [11], we expect the RFID chip to reach a range of 1 m, with an improved matching network, and antenna performance.

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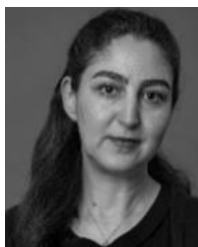[1] K. Gerd, F. Kawsar, D. Fitton, and V. Sundramoor, "Smart objects as building blocks for the Internet of Things," *IEEE Internet Comput.*, vol. 14, no. 1, pp. 44–51, Jan./Feb. 2010, doi: 10.1109/MIC.2009.143.

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