Blumino: The First Fully Integrated Analog SiPM With On-Chip Time Conversion

Andrada Muntean, *Graduate Student Member, IEEE*, Esteban Venialgo, Andrei Ardelean, *Student Member, IEEE*, Ashish Sachdeva, Emanuele Ripiccini, *Associate Member, IEEE*, Darek Palubiak, Carl Jackson, *Senior Member, IEEE*, and Edoardo Charbon, *Fellow, IEEE*

***Abstract*—Blumino is the first analog silicon photomultiplier with integrated amplifier, comparator and time-to-digital converter (TDC). The combination of a photodetector together with on-chip readout circuitry enables system-level advantages, such as internal parasitic reduction, compactness and simplicity. The analog silicon photomultiplier has a third output, called fast terminal (FT), in addition to the anode and cathode, which is used for timing measurements. The analog silicon photomultiplier presents excellent photon detection efficiency greater than 40% at 420 nm, making it suitable for positron-emission tomography. Measurement results of the TDC indicate a resolution of 128 ps least significant bit (LSB) with a differential nonlinearity and integral nonlinearity of $-1/+5$ LSB and $-2.4/+0.9$ LSB, respectively. The discriminator comprises two preamplifier stages followed by a complementary self-biased differential amplifier stage which is coupled to the analog silicon photomultiplier's FT through a decoupling capacitor. The sensor is also fully backward-compatible through the standard output which can be coupled to dedicated ASICs and standard readout integrated circuits. In addition to the electrical, radiation, and optical performance, the integration of a custom CMOS analog silicon photomultiplier process with standard CMOS process was investigated.**

***Index Terms*—Analog silicon photomultiplier, comparator, complementary self-biased differential amplifier (CSDA), fast terminal (FT), fully integrated, time-to-digital converter (TDC).**

I. Introduction

During the last decades, there has been a significant interest in the development of silicon photomultipliers (SiPM) as a replacement of the well know photomultiplier tubes (PMTs) which have been widely used in medical applications, such as positron emission tomography (PET) due to their stability, low noise, suitable spectral range, and fast response [1], [2]. Moreover, PMTs present important limitations, such as a high sensitivity to magnetic fields, bulkiness (physically large form factors) and operation at high voltages. Over the past 20 years, more interest has been shown towards the combination of PET and magnetic resonance imaging (MRI) scanners for small-animal research and clinical imaging. PET-MRI scanners are beneficial in many medical disciplines, such as oncology, cardiology, pediatrics, neurology, etc., as they provide both functional and anatomical information, with high spatial resolution and very good soft-tissue contrast while performing simultaneous acquisitions [3].

Integrating PET-MRI comes with many challenges that have to be addressed, such as combining two detector technologies without affecting the performance of each other [2]. At the beginning, semiconductor-based photodetectors, such as avalanche photodiodes were developed in order to detect red and near-infrared electromagnetic radiation with a relatively small active area. Later on, SiPMs which are arrays of avalanche photodiodes that operate above the breakdown voltage, proved to be suitable candidates for PET and PET-MRI scanners due to their robustness, insensitivity to magnetic fields, low noise, high PDE and low voltage operation [2], [4], [5]. In addition to all these features, SiPMs have a more compact form factor than PMTs [6]. There are two main types of SiPMs—digital (D-SiPM) and analog (A-SiPM). D-SiPMs have the output signal directly processed on-chip, with photons being detected and converted into digital signals. Due to the additional electronics presented in the D-SiPMs, in general, the fill factor could be highly degraded. Even if the conventional D-SiPMs do not use off-chip circuits, such as analog-to-digital converters (ADCs), time-to-digital converters (TDCs), discriminators, etc., compared with the A-SiPMs, routing skew could affect timing resolution. However, this can be compensated by design on D-SiPMs, for example, by using H-tree routing topology [7]. D-SiPMs have been used in many modular ToF-PET systems, coupled with scintillators for gamma photon detection. However, the design and optimization of D-SiPMs require long development cycles, complex user interfaces and their monolithic version constrain the SPAD performance with CMOS compatibility requirements [8]. In the case of A-SiPMs, the output

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Andrada Muntean, Andrei Ardelean, Emanuele Ripiccini, and Edoardo Charbon are with the STI-IMT AQUA, École Polytechnique Fédérale De Lausanne, 2002 Neuchâtel, Switzerland (e-mail: andrada.muntean@epfl.ch; a.ardelean@epfl.ch; emanuele.ripiccini@epfl.ch; edoardo.charbon@epfl.ch).

Esteban Venialgo was with STI-IMT AQUA, École Polytechnique Fédérale De Lausanne, 2002 Neuchâtel, Switzerland.

Ashish Sachdeva was with the CAS, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: ashishsachdeva.as@gmail.com).

Darek Palubiak and Carl Jackson are with Sensl Division, ON Semiconductor, Cork, T12 CDF7 Ireland (e-mail: darek.palubiak@onsemi.com; carl.jackson@onsemi.com).

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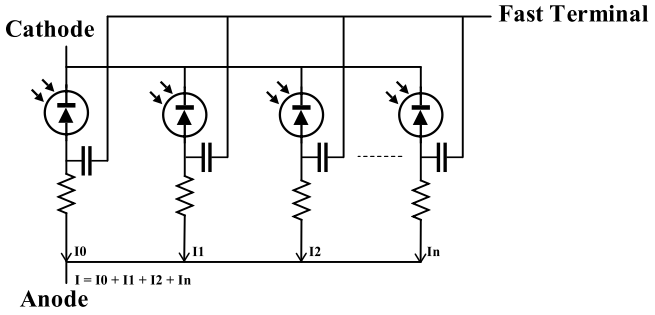

Fig. 1. Analog silicon photomultiplier with fast terminal (FT).

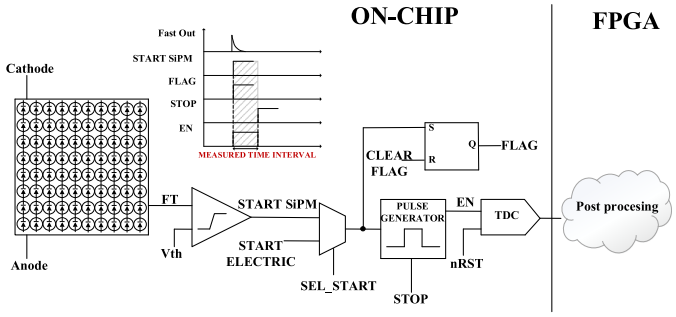

Fig. 2. Blumino's architectural diagram.

currents of each avalanche photodiode are summed up into one node and, in general, the output pulse is processed using off-chip circuits, such as shaping circuits, TDCs, etc. The large capacitance at the output path significantly impacts the timing performance of the detector.

Blumino has been designed to overcome the main limitations of A-SiPMs by integrating on-chip electronics, such as a discriminator and TDC while keeping the sensor backward-compatible. One of the limitations is related to the system compactness. Usually, A-SiPMs are coupled with external electronics or ASICs which comprise the readout electronics of the A-SiPM. This means that there will be two separate entities coupled together which results in a bulkier system. Considering, for example, an array of A-SiPMs, each of them with its own external readout, this will result in a very large system. Moreover, the power dissipation of multi-ASIC systems is very large. Another advantage is related to the reduction of the capacitive load on the fast output. By having the high speed and optimized electronics on the same silicon, the capacitive load should be substantially improved, thus improving the overall timing performance.

The backward compatibility is essential in order to measure the energy of a gamma photon as it triggers a scintillation independently from its time of interaction in the scintillator, which is independently performed in the fast output.

ON Semiconductor has developed a unique A-SiPM by adding a third terminal in addition to the anode and cathode called FT (Fig. 1). The FT presents a lower output capacitance of $\sim$40 pF compared to standard output that makes it suitable for ultrafast timing measurements [9]. A fast output signal with a very sharp rising time is present at the output of the A-SiPM without any need of extra circuits. However, while the lower capacitance reduces the electronics noise, the AC coupling of the FT also reduces the pulse amplitude and consequently the signal-to-noise ratio. In order to not degrade the pulse amplitude, the FT is first connected to an on-chip amplifier. Blumino is the first PET sensor consisting of a fully integrated A-SiPM with on-chip time conversion [10], [11]. The time estimation is done through the FT connected to a preamplifier, comparator and finally, to a TDC, while the energy is estimated through the standard-output, which has been preserved for backward compatibility. The resulting system is capable of measuring timestamps and performing energy estimations. Moreover, the fill factor is not affected by the presence of the readout circuitry, such as in the case of D-SiPMs. The current packing fraction is 57% because of the presence of test structures. By considering the A-SiPM, TDC and comparator only, the packing fraction is increased to 71%. The sensor serves as a proof of concept of future PET modules with A-SiPMs and integrated electronics. Future developments will target an increase in the packing fraction as well. As a result, Blumino is a simple, compact, and backward-compatible PET prototype module.

In this article, we describe the architecture in detail, along with extensive simulations and measurement results.

II. System Architecture

The sensor's architecture is presented in Fig. 2. The A-SiPM has three different terminals: 1) anode (standard-output); 2) cathode; and 3) FT. The system is accessible through the standard output, which can be coupled with external electronics, such as preamplifier and comparator, while the FT is connected directly to the integrated discriminator through AC coupling. The comparator output represents the input START signal for the TDC. However, the system has the capability to switch between the comparator output and an electrical external trigger to act as the TDC's starting signal. The STOP signal is always generated externally by an FPGA. A validation FLAG signal is generated every time there is a signal coming from the A-SiPM, which allows to select only the events that trigger the TDC and limit the readout time. The sensor can be read out in two different ways, parallel or serial. The range can be extended by adding an additional counter in the FPGA that takes as an input the most significant bit of the TDC's counter. The STOP signal is a 10-MHz clock generated by the FPGA. During electrical testing, an additional START signal is generated with the same frequency but an adjustable phase with respect to the STOP which allows different impulse pulse widths to be fed to the TDC. The FLAG is issued every time the START arrives at the TDC and it is read together with the output data. Currently, the FLAG is used in post-processing to eliminate invalid TDC readings during optical tests where there is a possibility of not receiving the START signal (no photon). The readout is performed using a 9-bit parallel bus, where 1 bit is dedicated to the FLAG and the rest is multiplexed output data. The resulting bandwidth is 20 MB/s due to the fact that readout is performed only once every 100 ns (STOP signal period is 10 MHz). The data is then accumulated on the FPGA in a large 65 535 words FIFO and transferred to the PC via USB 3.0. The data is then analyzed in MATLAB.

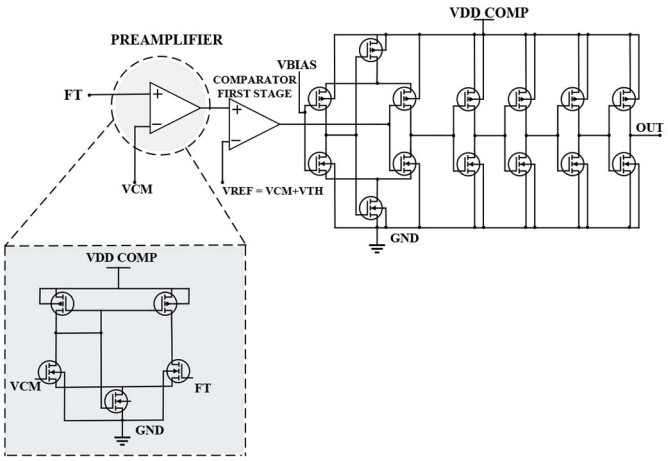

Fig. 3. High-speed asynchronous comparator. It comprises a first amplifying stage, a comparator, and a multistage buffer.

A. Preamplifier

Initial analysis has been performed by modelling the fast output pulse at the comparator's input to determine parameters, such as input rise time, input capacitance, and AC coupling capacitor value. The comparator is a self-biased differential amplifier (SDA), a modified version of [12], whereas the concept was introduced in [13] and [14]. A preamplifier stage is needed in order to increase the absolute threshold resolution with respect to the nonamplified input signal range. The comparator's first stage and the preamplifier are SDAs as depicted in Fig. 3.

B. Complementary Self-Biased Differential Amplifier

A CSDA consists of two complementary differential amplifiers with similar sizes but opposite polarity in terms of NMOS and PMOS (see Fig. 4). This amplifier comprises two equal bias voltages for current sources M3 and M4. Any shift in bias voltage results in an unequal current. The self-biased structure forms a negative feedback loop which stabilizes the bias voltage.

As Vin+ increases, the node VBIAS starts to decrease, as M2A turns on and M1A turns off. Consequently, M3 turns on and M4 turns off, which allows a current path from VDD until VH. At the same time, Vin− starts to decrease, M1B turns on and M2B turns off. As a result, the current can sink through VDD to the load capacitance. Thus, the output node reaches VDD$-I_{on+}\times$ ($R_{onM1B}+ R_{onM3}$). The CSDA provides large current sourcing and sinking property without the need of high quiescent current. Hence, the switching speed is high. Furthermore, M3 and M4 are sized to be in triode region, so the available swing at the output is also high [15].

C. TDC

The TDC is composed of three main blocks: a voltage-controlled ring oscillator (VCO), an asynchronous ripple counter which keeps track of the number of oscillations through the ring and determines the most significant bits of the TDC, and transparent phase detectors which capture the states of each phase when the ring freezes, thus determining the least significant bits (LSBs). The VCO has a multipath gated

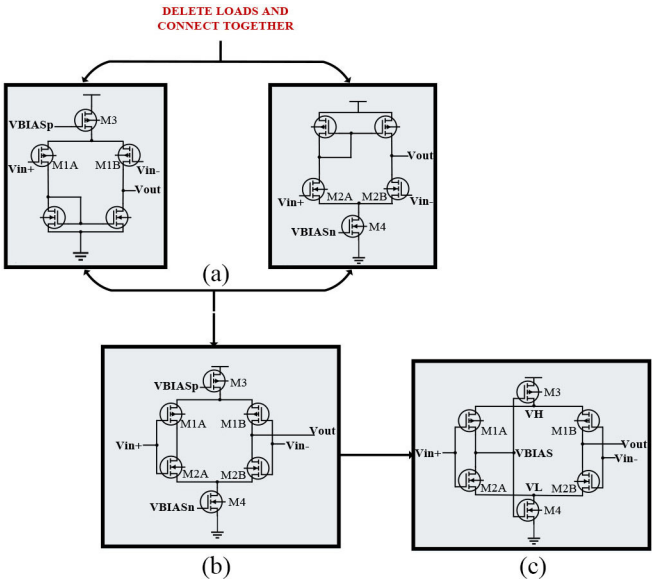

Fig. 4. (a) Two complementary differential amplifiers. (b) Merging two differential amplifiers with similar bias voltages. (c) Complementary self-biased differential amplifier (CSDA).

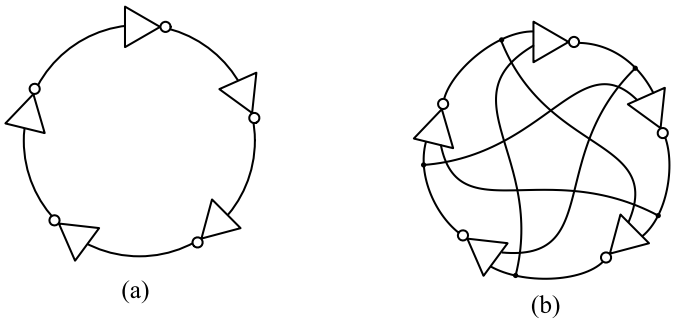

Fig. 5. (a) Conventional ring oscillator. (b) Multipath ring oscillator.

ring oscillator (MGRO) topology. In comparison with standard gated ring oscillators, MGROs have a higher oscillation frequency, resulting in a smaller delay per stage and a smaller LSB [16]. The difference between the two ring oscillators is presented in Fig. 5. Compared with a classic ring oscillator, in a MGRO architecture, the delay stage can have multiple inputs, one connected to the previous delay stage and the others connected to different delay stages along the ring. These types of connections help each delay stage to start transitioning ahead of time, decreasing the switching times and increasing the oscillation frequency. The decision of using a delay stage composed of a tristate inverter with three inputs (see Fig. 6) limits the minimum number of delay stages in the ring to nine. As a consequence, 18 phase states are used to determine the fine bits of the TDC. The 18 states are represented on 5 bits after decoding, which together with the 6-bit counter create a 10-bit result, with redundancy. The output processing is implemented off-chip, on the FPGA. The final result is calculated as

$$N_{\text{result}} = 18 \times N_{\text{coarse}} + N_{\text{fine}} \tag{1}$$

where N_{coarse} is the counter value and N_{fine} is the decoded value of the fine bits.

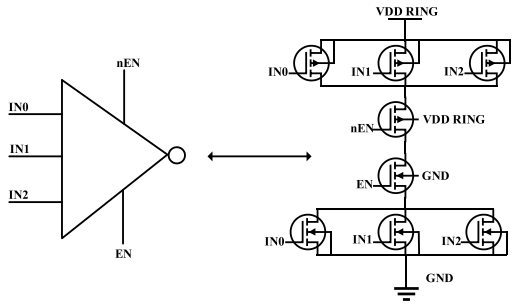

Fig. 6. Multipath gated ring oscillator's delay stage: tristate inverter with three inputs.

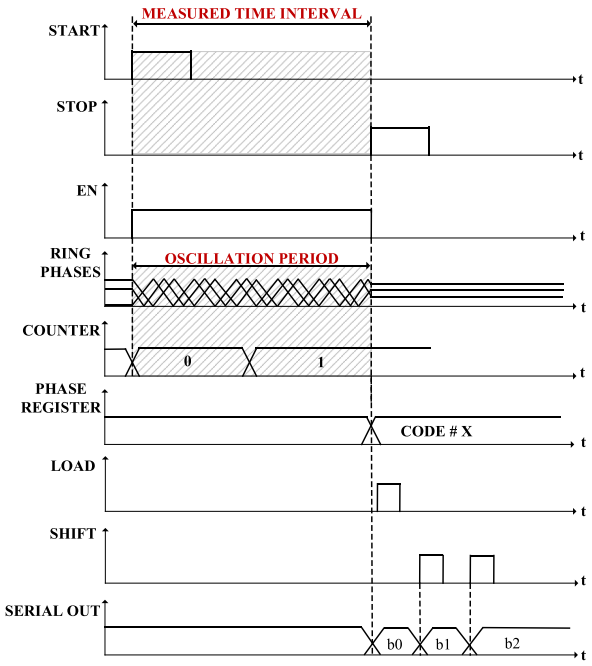

Fig. 7. Timing diagram of the TDC operation.

The operation of the TDC starts only when the ring oscillator receives a START signal from the comparator, which together with a STOP signal from the FPGA forms an enable (EN) signal. The ring starts oscillating when EN is high. At the falling edge of EN the ring freezes in its current state which is saved in a register along with the current counter value. The TDC can be read out in two different ways, serial or parallel, however, for all the performed measurements in this article, parallel readout was preferred because of its higher speed. The TDC's operation principle is illustrated in Fig. 7.

Due to the limitations of the technology node and the experimental nature of integrating two different CMOS technologies in the same design, the comparator targeted a relatively conservative typical threshold of 114 fired A-SiPM cells.

Once the concept was validated, future implementations will focus on improving both the TDC and comparator performance with a more aggressive approach.

D. Testing Platform

The chip was encapsulated in a ceramic pin grid array (CPGA) package with a quartz window. A custom PCB was designed to provide the power and bias voltages required to operate the chip as well as to serve as an interface between the photodetector and FPGA. The custom PCB connects to an Opal Kelly XEM7360 Kintex-7 FPGA board. The chip input-output pads are directly connected to the FPGA along with the control signals for the power supplies. The PCB makes use of digital potentiometers which allow the possibility of sweeping bias voltages for both the TDC and comparator. In addition, the power supply voltages can be digitally adjusted, which gives the possibility to create an automated test setup for the entire system that can also act as a phase-locked-loop (PLL) during normal operation. The testing platform is depicted in Fig. 8.

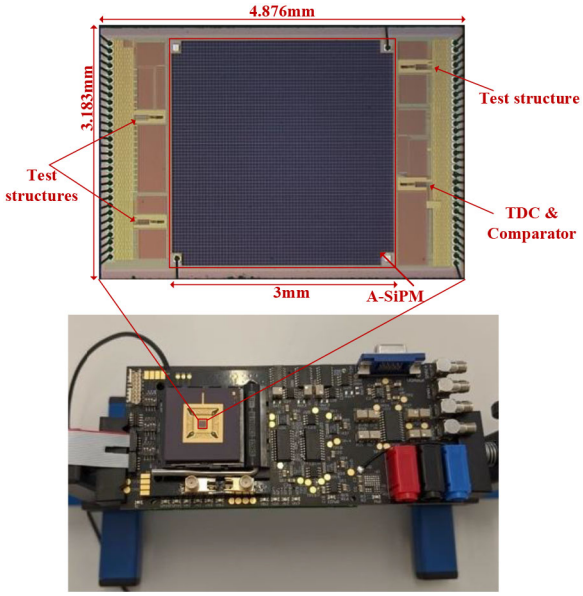

Fig. 8. Testing platform and chip micrograph.

III. Blumino Measurement Results

A. Electrical Characterization

Before characterizing the system as a whole, the main building blocks were analyzed separately. An internal multiplexer allows the FPGA to interface directly with the TDC and to bypass the analog frontend.

First, the TDC is set in a free running operation mode, which allows the measurement of the VCO's frequency and average power consumption. At this point, the dependency on the power supply variation is measured by sweeping the supply voltage. The TDC's resolution can be adjusted by acting on the TDC's power supply. The oscillation period (T_{OSC}) is read out from the sixth bit of the counter while manually changing the power supply of the ring oscillator. As expected, T_{OSC} decreases with power supply at an average rate of -1.24 ns/V, improving the LSB. This dependency was measured for three different dies, all of them presenting the same behavior as seen in Fig. 9(a).

The variation of the oscillation period with temperature was measured by using a temperature chamber. The temperature was varied in steps of 4 °C from -12 °C to 28 °C. The oscillation period thermal drift was determined to be 0.3125 ns/ °C

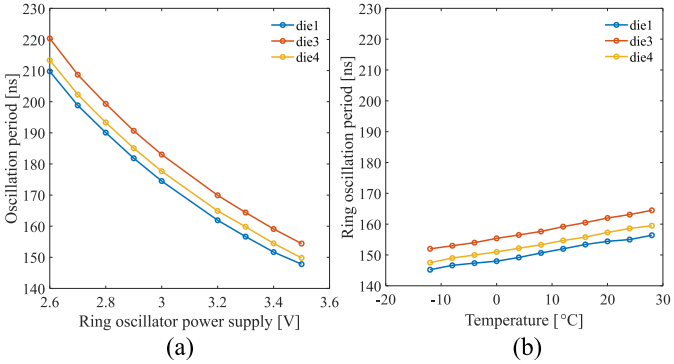

Fig. 9. (a) Oscillation period variation with power supply for three different dies. (b) Variation with temperature.

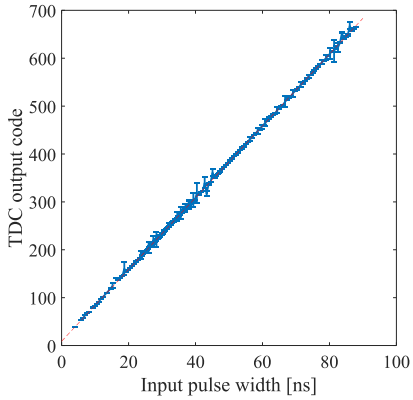

Fig. 10. Electrical transfer function measurement over a range of 80 ns.

as depicted in Fig. 9(b). The results indicate that the temperature variations can be compensated for by changing the power supply of the ring oscillator within a narrow range of around 300 mV.

The transfer function of the TDC was measured by generating the START and STOP signals with the FPGA and varying the time interval between them over a range of 80 ns, with 16 384 iterations per point. The transfer function of the TDC is depicted in Fig. 10 and indicates an average TDC LSB of 128 ps.

The full chain (A-SiPM-comparator-TDC) single-shot precision at multiphoton level was measured by using a 374-nm ps laser at a 10-MHz repetition rate for an A-SiPM excess bias voltage of 2.5 V. The results for three different delays between the laser and STOP signal are illustrated in Fig. 11. The measurements were performed in the multiphoton burst detection mode due to the minimum threshold of the comparator which corresponds to 114 fired cells in the A-SiPM.

The DNL and INL were measured by performing a density test which consists of illuminating the A-SiPM with white light and reading out all the timestamps from the TDC over a long period of time. Under ideal conditions, the resulting histogram is uniform, and therefore any deviations from this behavior are caused by the nonlinearities of the TDC. This test required the complete system functionality and as a result, it was performed last, after all blocks had been characterized.

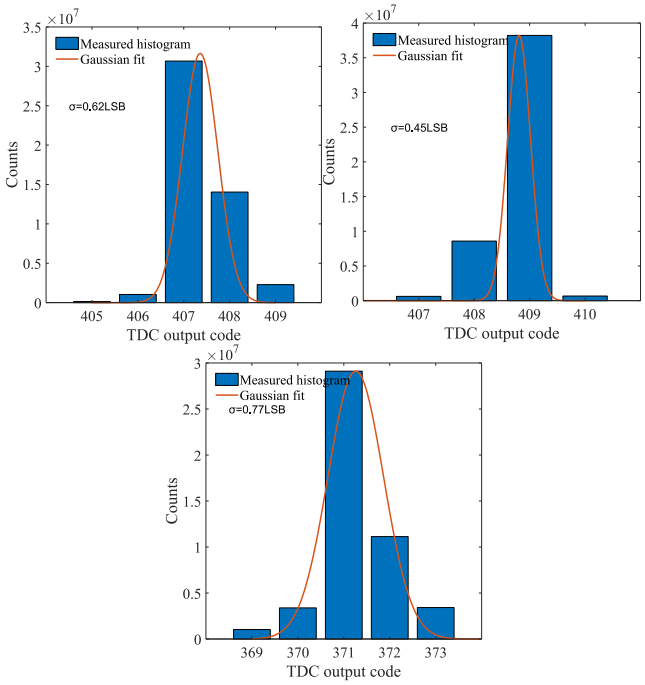

Fig. 11. Full system single-shot precision of three different TDC output codes.

The results are illustrated in Fig. 12 and present a differential nonlinearity and integral nonlinearity of $-1/+5$ LSB and $-2.4/+0.9$ LSB after compensation. The compensation consists of correcting the TDC output code based on a look-up table (LUT) which in turn was created from the INL results of a very large dataset. The approach of using a LUT for the INL calibration will not work across a wide range of temperature changes this being demonstrated through measurements at two different temperatures, 26 °C and 16 °C, where the VCO power supply was set at 3.3 and 3.25 V, respectively, to compensate for the change in the oscillation frequency. By using the same LUT, the compensated INL was noticeably degraded, however, the DNL was almost the same. If a wide range of temperatures is required, less naive compensation methods should be employed.

B. Optical Characterization

The A-SiPM was characterized in terms of PDP and DCR. The PDP was measured on Pandion—a 400 × 100 SPAD sensor for ToF LiDAR with 5Hz median DCR and 11 ns mean dead-time which uses exactly the same SPAD device as Blumino [17]. Both chips, Pandion and Blumino, were included on the same wafer and as a result, the fabrication process should affect the performance of both sensors in the same way. The results are illustrated in Fig. 13 and show that the PDP slightly decreases after integration when compared with the commercially available standalone SiPMs [18].

Additional possible performance degradations due to the integration of a custom process A-SiPM with standard process electronics on the same chip were investigated. The DCR was measured for several dies at different excess bias voltages. 500 frames were accumulated for each excess bias voltage for

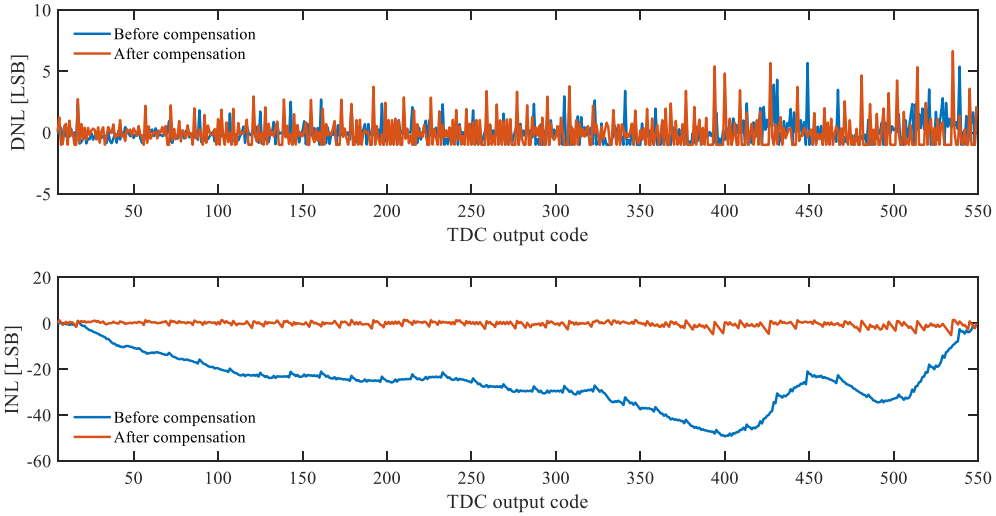

Fig. 12. DNL and INL measured through density test for the entire chain (A-SiPM-comparator-TDC).

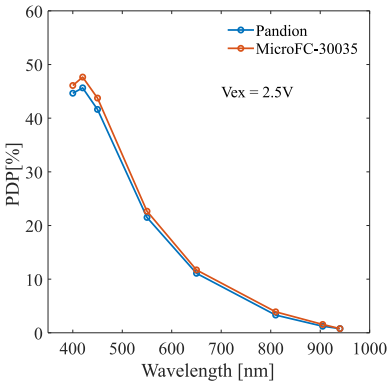

Fig. 13. Photon-detection probability (PDP) comparison before (C-SERIES: MicroFC-30035) and after integration (Pandion) [17].

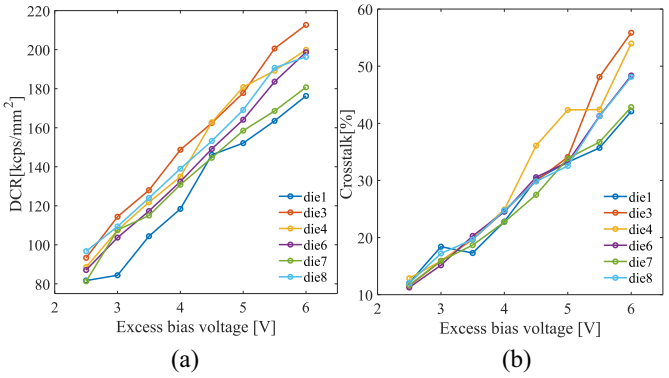

Fig. 14. (a) A-SiPM dark count rate versus excess bias voltage. (b) A-SiPM crosstalk versus excess bias voltage.

a duration of 5 μs. The DCR was calculated by taking into account the pulses above the 0.5 phe level [19] and is depicted in Fig. 14(a). The large peaks that correspond to 1.5 phe level are the contribution of crosstalk to DCR [19] and are reported separately in Fig. 14(b). The 0.5 phe and 1.5 phe levels are represented in Fig. 15.

The crosstalk probability was determined as the ratio of 1.5 phe and 0.5 phe rates. The DCR for this A-SiPM has

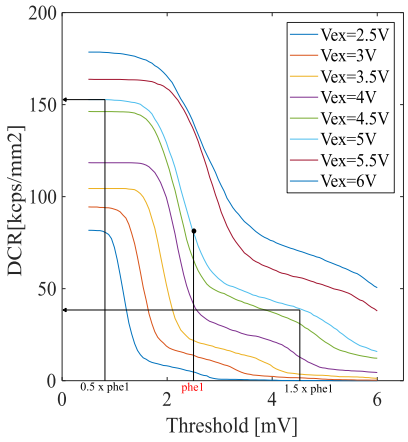

Fig. 15. First photoelectron, phe1 is taken as the trigger level at the middle of the drop from one step to the next. The count rate at the 0.5×phe1 is considered as dark-count rate (DCR) and the rate at 1.5×phe1 divided by the DCR value is the crosstalk probability.

already been measured by ON Semiconductor and presented in [19] and is used as a reference for this sensor. Single-photon timing resolution measurements were not performed through the fast-output, the reason being that the minimum threshold of the comparator was designed for an input pulse that corresponds to 2.5% fired microcells in the A-SiPM, that is, 114 microcells out of 4774 microcells in total. As a consequence, the sensor cannot be used in photon starved mode with the fast-output. However, this does not represent an issue because during the scintillation process a large amount of photons are produced and can be easily read out.

C. Radiation Characterization

The coincidence timing resolution (CTR) measurement is performed by placing a ^{22}Na source between two detectors which produces back-to-back 511-keV gamma photons. The two gammas are converted into visible photons by the scintillators which are then detected by the A-SiPM. For the following radiation measurements, 2.5×2.5×20 mm^3 LYSO crystals

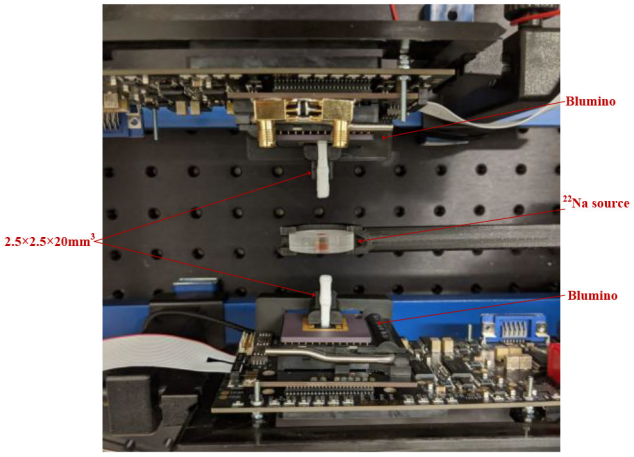

Fig. 16. CTR measurement setup. Two Blumino sensors are placed in coincidence.

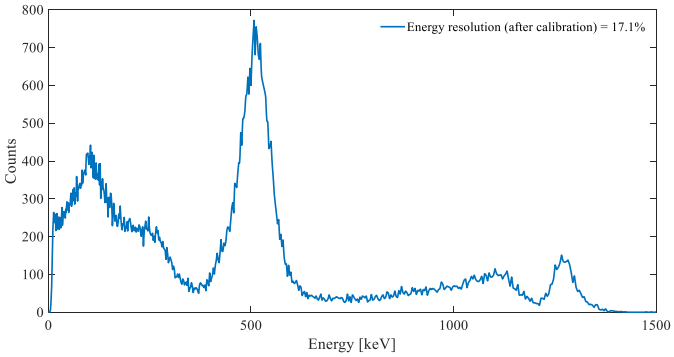

Fig. 17. ^{22}Na energy spectrum measured with Blumino.

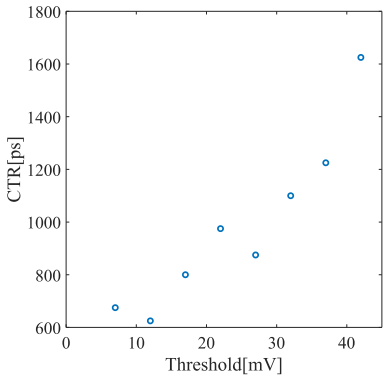

Fig. 18. Measured CTR (FWHM) at different threshold values.

wrapped with teflon tape about 0.5-mm thick and glued to the SiPM using optical grease were used. The measurement setup is shown in Fig. 16. Initially, all the measurements were performed only on the standard output of the A-SiPM demonstrating the capability of the system to be used as a conventional PET detector.

The energy resolution was determined by the charge integration of the A-SiPM without any amplification at 3-V excess bias through the standard output. The energy spectrum was analyzed and linearized in MATLAB and it is depicted in Fig. 17 presenting an energy resolution of 17.1%.

TABLE I
SYSTEM PERFORMANCE SUMMARY

	Performance	Post-layout simulated value	Measurement results
SiPM	PDE @420nm	> 40%	
	Fill factor	75%	
	DCR @2.5V excess bias voltage	53kcps/mm^2	81.7kcps/mm^2
TDC	Technology	0.35µm	
	LSB	65ps	128ps
	DNL	±0.55LSB	-1/5LSB
	INL	±1LSB	-2.4/0.9LSB
	Resolution	10 bits	
	Supply voltage	3.3V	
	Power (peak/standby)	<9mW/1mW	
System	Area	3×3.3 mm^2	
	Backward compatible	yes	

In order to determine the CTR, 100.000 frames were accumulated for both A-SiPMs placed in coincidence with a 40GS/s LeCroy oscilloscope triggered by one of the A-SiPMs. Only the frames where a pulse was present on both channels were kept. All the waveforms were analyzed afterwards in MATLAB. The frames containing pulses that did not correspond to the 511-keV photopeak (energy window of 408 to 613 keV) were discarded. The remaining data was analyzed for different voltage thresholds by extracting the absolute timestamps of the impulse for both channels and computing the difference between them. The FWHM of the resulting distribution for a specific threshold after the error introduced by the timewalk [20]–[23] was accounted for represents the CTR and is depicted in Fig. 18.

The summary of the post-layout simulation results and measurements are presented in Table I. As it can be noticed, there is a discrepancy in the LSB and nonlinearity values. An LSB of 65 ps was achieved in post-layout simulation while measurements indicate an LSB almost twice as large. This result is most likely due to inaccuracies in the transistor models because the variation is too big to be attributed solely to the layout mismatches and parasitic capacitances. Multiple measurements were performed on different dies indicating the same behavior, which suggests consistency with inaccurate model parameters. In future, the TDC design will be pushed towards an even better performance with improved resolution and linearity.

IV. CONCLUSION

Blumino demonstrates the first full integration of an A-SiPM with time-conversion on-chip. Optical, electrical and radiation measurements have been successfully performed. The system exhibits a timing resolution of 128 ps (TDC LSB) and an energy resolution of 17.1% when coupled to a 2.5×2.5×20 mm^3 LYSO scintillation crystal. Minor degradations due to the integration of custom CMOS SPAD process with standard CMOS were observed in the DCR with a measured value of 81.7 kcps/mm^2 at 2.5-V excess bias. Single-shot precision measurement results have a small standard deviation of 0.45LSB in the best case. Blumino represents the first step towards the digitization of A-SiPMs which comes along

with multiple benefits, such as the reduction of capacitive paths, simplicity, and compactness. Backward compatibility is also a feature of this design, which we believe will pave the way towards highly scalable, high performance, and low-cost A-SiPMs operating within digital systems. Future work will involve additional CTR measurements performed with the integrated comparator and TDC. Partitioning of the A-SiPM into multiple clusters along with improving the timestamping capability will also be studied.

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