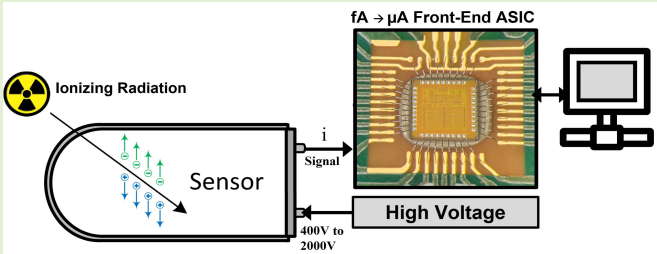
An Ultra Low Current Measurement Mixed-Signal ASIC for Radiation Monitoring Using Ionisation Chambers

Sarath Kundumattathil Mohanan, Hamza Boukabache, *Member, IEEE*, Vassili Cruchet, Daniel Perrin, Stefan Roesler, and Ullrich R. Pfeiffer, *Fellow, IEEE*

***Abstract*—Measurement of total ionizing dose in a radiation field is efficiently carried out by ionisation chambers. The paper details the design of a mixed-signal ASIC for the front-end electronics of ionisation chambers. A single chip solution for ultra-low current measurement is designed by combining the current processing analog section realized using low leakage thick gate transistors and the data handling digital section implemented using fast thin gate transistors. The design succeeds in limiting the cross coupling between the two circuit domains using deep n-wells and guard rings. The ASIC fabricated in 130 nm technology attains a wide dynamic range of −7 fA to −20 μA with maximum error in measurement less than ±4 %. The ASIC occupies an area of 3.52 mm^2 and has a total power consumption of 17.4 mW. The femtoampere range input leakage current of the ASIC contributed primarily by the ESD diodes was found to be varying exponentially with temperature. Dose rate measurements from 5 μSv/h to 7.4 Sv/h is demonstrated by interfacing the ASIC to an ionisation chamber.**



***Index Terms*— ASIC, ionisation chamber, femtoampere current measurement, mixed signal design, radiation monitoring, leakage current.**

I. Introduction

IONISATION chambers are some of the most used devices for radiation monitoring in the many fields spanning nuclear industry, high energy physics experiments, radiation therapy, etc. [1]–[3]. At the European Organization for Nuclear Research (CERN), different kinds of Ionisation chambers are used to address the complex nature of radiation fields present at various experimental facilities [4], [5]. These chambers convert ionizing radiation into electrical current. They have the advantage to operate throughout a very wide measurement range but often have low sensitivity. As a consequence, the generated current can be as low as a few femtoamperes for environmental monitoring while it can raise up to tens of microamperes when the detector is installed in the experimental zones with very strong pulsed radiations. This work demonstrates the design and development of an ASIC that can cater to this wide dynamic range.

In the current radiation monitoring system at CERN, the front-end electronics is implemented with discrete components and performs current-to-frequency conversion (CFC) using a reset counting method. This system, described in [6] and [7], is capable of measuring the current produced by the ionisation chamber from 1 fA to 2 μA. Another system is used for beam-loss monitoring where higher radiation levels are expected [3]. Its front-end electronic described in [8] is implemented with an ASIC that can measure current from 1 pA to 1.05 mA using charge balancing to perform CFC. Charge balancing method is also used in the work exposed in [9], [10], and [11] where a 64-channel ASIC is implemented.

Replacing the current discrete components solution for the front-end electronics of CERN's radiation monitors by an integrated circuit was already studied in [12] and [13]. However, as for the works mentioned above, this circuit requires some additional external logic to process and send its output to the external world. A new version of the ASIC was thus developed based on the results obtained in [13] and taking advantage

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of the high-speed core transistors to build a true single-chip solution that deals with current measurement, digitization, data processing, and communication.

Designing such a circuit for current measurement and real-time data transfer faces the dual challenges of low leakage requirements and high-speed capability. A possibility of using the high-speed digital cells of 130 nm technology node in combination with the low leakage IO transistors to design a complete single-chip solution was mentioned in [13]. This paper details the design of such a mixed-signal chip that can measure currents from femtoampere to microampere with real-time transfer to visualization software. All the major building blocks that are needed in a complete current measurement system are integrated into a single chip. The designed ASIC is a fully autonomous system that can process the injected current in its analog blocks, calculate various parameters, store the calculated data in its internal memory and send it to any test computer through a standard serial interface. The architecture of the Chip 3 explained in [13] is adapted to increase the range and forms the analog section of the ASIC presented. The details of the digital section of this ASIC along with the various challenges encountered in designing a mixed-signal current digitizer with femtoampere sensitivity are addressed in this paper. A brief overview of ionisation chambers used at CERN and their operation principle is also presented.

II. Ionisation Chambers for Radiation Protection at CERN

The Radiation Protection Group at CERN exploits two kinds of ionisation chambers. It uses high-pressure ionisation chambers filled with argon or hydrogen gas to monitor radiation doses to personnel and environment due to stray radiation emitted during operation of CERN's accelerators and experiments. Furthermore, air-filled monitors under atmospheric pressure are utilized for the measurement of residual dose rates from activated components inside accelerator tunnels and around experiments when the beams are off.

The basic operational principle of both detector types is similar, and it is based for both kinds on the ionisation of gas molecules caused by incident particles traversing the active medium. The choice of the gas depends on the application, the nature of particles and their energies. The higher is the gas pressure the better is the sensitivity of the detector.

Dose rates from radiation fields dominated by gamma rays and muons are monitored with argon-filled chambers pressurized at 20 bars. The gas is confined into a steel made container of 5.2 L. For neutrons and mixed radiation fields, the same chambers with pressurised hydrogen gas are used. The air-filled ionisation chambers under atmospheric pressure, that are employed for the measurement of residual dose rates, are installed close to accelerator and experiment components and are, thus, exposed to strong radiation fields during operation. Therefore, they are made of graphite and plastic to minimize the activation of materials of the chamber itself.

When subject to ionizing radiation fields, the interaction between the contained gas and the incoming particles generates ion-electrons pairs. To avoid recombination effects and collect the created charges, a strong electric field is applied through a high voltage electrode. The measurement that is done is directly proportional to the number of ion pairs collected and, thus, related to the strength of the radiation field. Although the ionisation chambers do not distinguish between the different types of radiation, these detectors allow precise assessments of absorbed dose over time. They have no dead time as other detectors can have and they are quite reliable.

TABLE I
Ionisation Chambers Used at CERN for Radiation Protection Measurements

Detector	Measurement range	Generated Current
Argon-filled Chamber	50nSv/h → 0.5Sv/h	γ : 80fA → 800nA
Hydrogen-filled Chamber	50nSv/h → 0.5Sv/h	γ : 5.7fA → 56nA n: 2fA → 20nA
Air-filled Chamber	0.5μSv/h → 10Sv/h	γ : 12fA → 250nA

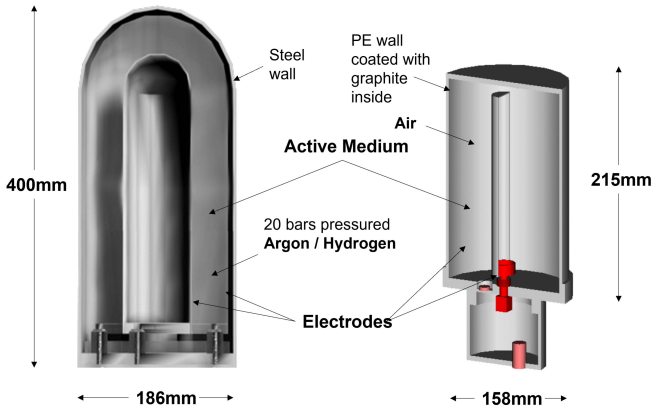

Fig. 1. Cross-sectional view of ionisation chambers used at CERN for radiation protection measurements. Left sketch: high-pressure ionization chamber, right sketch: air-filled ionization chamber [14].

It is however particularly challenging to design front-end circuits that can continuously measure generated currents without losses over large dose intervals such as presented in table I. The table summarises the required measurement range for different ionisation chambers used at CERN and the equivalent currents generated.

For high radiation areas with risk of activation, as is the case for the above-mentioned air-filed ionization chambers, the readout electronics is deported into areas with low radiation levels [6]. The charges produced by the ionisation chamber are transported using a specific SPA6 cable that CERN has designed to carry both the high voltage and the generated charges through hundreds of meters with minimal losses [15].

III. Low Current Measurement Methods

Current measurement in the presented ASIC is performed using direct slope measurement (DSM) method and charge balancing (CB) method [13], [16], [17] as shown in Fig.2. An operational transconductance amplifier (OTA) based integrator receives the input charges in its feedback capacitor. As the integrator output rises beyond set thresholds, two comparators are progressively asserted generating outputs Comp1 and Comp2. The time difference of their assertion is proportional to the input current and is used for current calculation in DSM method. In the CB method, when the

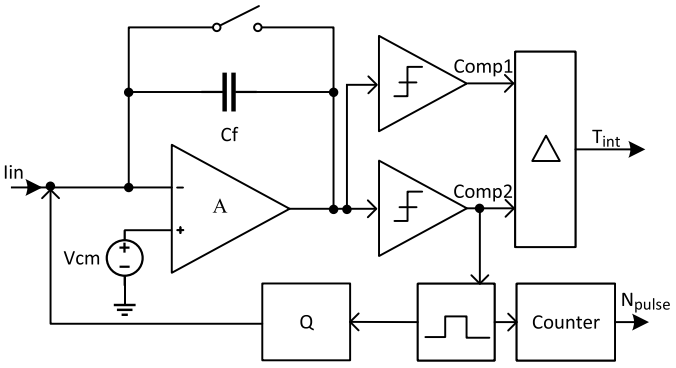

Fig. 2. Charge balancing and direct slope measurement method.

Comp2 is high, a pulse of fixed duration is generated which triggers the generation of a charge of opposite polarity as that of the input. This generated charge is injected to the input node thus effectively discharging the feedback capacitor. The number of such charge injections is proportional to the input current.

IV. Mixed Signal ASIC Architecture

The architecture of the ASIC is shown in Fig.3. The analog section was designed using the 3.3 V thick gate transistors and the digital section using the 1.2 V core transistors. An array of level shifters translates the signal between the voltage domains.

The ASIC consists of two channels. The primary channel is for the measurement of the input current while the secondary channel is left open to calculate the leakage current in the system input. Both the channels have similar architecture and the measured leakage by channel 2 is intended to compensate for the leakage in the primary channel. The input current is integrated in a feedback capacitor of channel 1. The integrated output is fed to four comparators. The outputs of the first two comparators are used for the current calculation by the DSM method. The charge generator block comprising of *Q_low*, *Q_med* and *Q_high* sub-blocks generates the charges for the current calculation using the CB method. The blocks are progressively enabled depending on the assertion of second, third and fourth comparator output respectively.

The digital section consists of two channel interfaces for processing the comparator pulses and generating different counts for the two current measurement methods. The generated counts are time-multiplexed and stored in a memory. The data from the memory is transmitted out through a serial interface to a measurement software. A controller orchestrates the entire data flow by generating various control signals. A clock generator block receives a stable clock supplied by an external oscillator and further generates various clocks for different internal modules.

The data generated by the analog section is treated by the digital blocks and transferred to an external interface. The asynchronous comparator outputs are synchronized to the local clock domain in the channel interface blocks. The two-stage synchronizer also eliminates the possibility of metastable states. The synchronized outputs are fed to pulse generators which generate one pulse each for each active edge of the comparator outputs. For the current calculation in the direct slope method, the time between two comparator threshold crossings must be measured. The interval counter module counts this after adding sufficient debouncing to the pulses to eliminate false transitions due to external noise.

The second comparator (Comp2) output also acts as the enable signal for the monostable pulse generator. The on and off times of the monostable pulses are stored in a register file which are programmed through the serial interface. The pulses are generated as long as the enable signal remains high. These pulses are fed back to the analog section for controlling the charge generation in the *Q_low*, *Q_med* and *Q_high* blocks. The output of comparator 2 also triggers the generation of the enable signal for the *Q_low* in the analog section. Two more enable signals are generated by the digital block for the *Q_med* and *Q_high* blocks based on the comparator 3 and 4 outputs. Pulse counter modules count the number of monostable pulses generated corresponding to the duration for which each of the low current, medium current, and high current paths are activated.

Channel 2 interface also generates similar pulses when comparators 5 and 6 are triggered. An interval count for the pulse duration between two comparator outputs and a pulse count corresponding to the monostable pulses of channel 2 are generated. The six different counts from the two channels along with different status signals are grouped into 32-bit registers. A total of eight different such 32-bit words are then sequentially passed on the transmit SRAM module through a multiplexer.

A wrapper module generates the addresses for writing and reading from the TxSRAM. The 32-bit data words are converted to 8-bit words and fed to the UART module. Multi-level handshaking from the UART module and the controller module generates the different control signals for the SRAM. Whenever there is new data available in the TxSRAM, the UART module is notified and the data transmission is initiated. The data flow in the output path is designed to have a real-time data transfer from the comparator outputs to the UART output.

In the input path, the received serial data is processed by the UART module and stored in the RxSRAM. The RxSRAM wrapper converts the 8-bit UART data to 32-bit words to be stored in the SRAM. The register write controller gets enabled when there is data in the RxSRAM. The first received data is treated as the address for the register file and the following 32-bit word is then written to this address in the register file by its controller. The register file holds various control signals, timing parameters, and voltages for the digital-to-analog converters (DACs).

The various threshold voltages for the comparators and the bias voltages are supplied externally to the ASIC. Two DACs on a test board generate these voltages. The DACs could be programmed by the ASIC through an on-chip I2C module. Reading of temperature and humidity data is also handled by the I2C module.

The controller for the ASIC is realized as a state machine. In the normal operational mode, the state machine is enabled by default. Depending on the configuration register, the

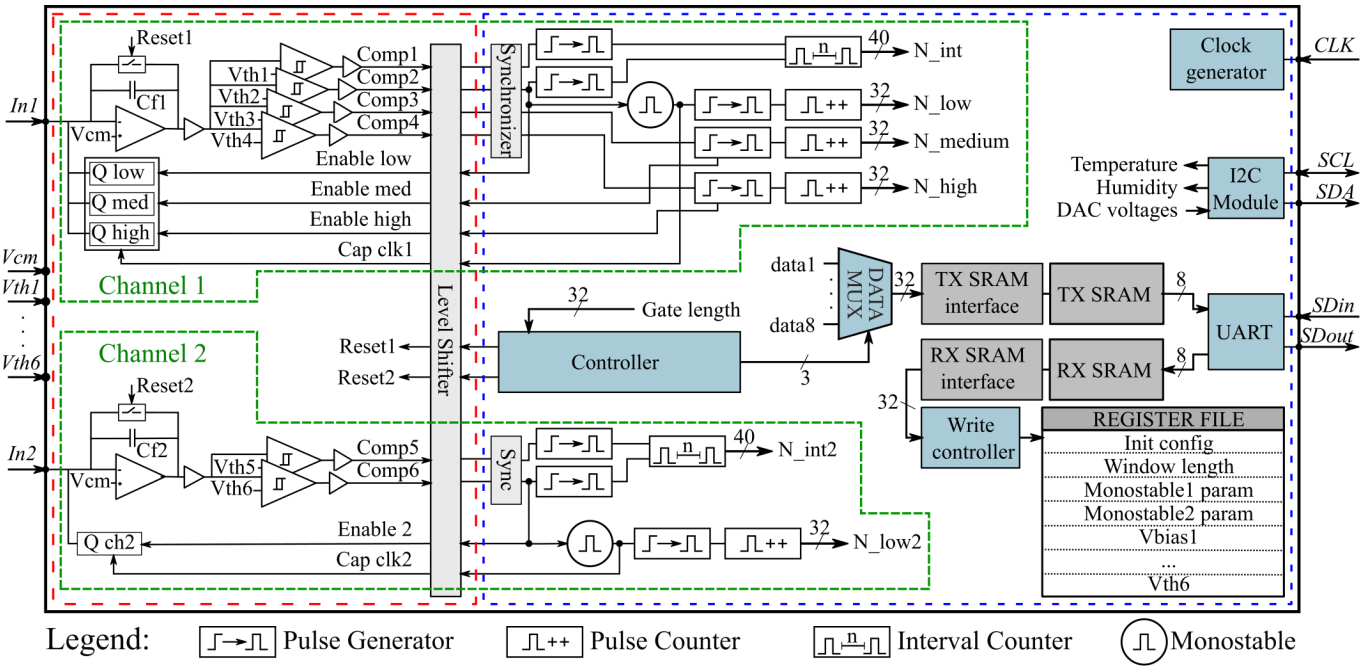

Fig. 3. ASIC architecture. Analog and digital sections are framed in red and blue respectively.

controller goes through states of DAC programming and temperature sensor reading. After these initialisation operations, the controller reaches the main counting state where a timing window generator counter is enabled. A gate end pulse is generated each time the counter reaches the programmed time window. At this moment various pulse counter and interval counter registers are updated. From the counting state, the state machine changes to eight data transmit states corresponding to different data words to be transmitted. Select signals for the data multiplexer for each of the data words are generated in these states. After sending the eight data words, depending on the enable signals the whole operation is repeated. The ASIC is designed to continuously calculate the different counts and transmit them in a loop unless disabled through the control register.

A. Reset Scheme

In the normal operation of the ASIC, the reset signals Reset1 and Reset2 are used only during the initialisation phase to discharge the residual charges in the feedback capacitors of channel 1 and 2 respectively. The ASIC has separate resets for the digital and analog sections with dedicated pins. The analog section could also be reset by digital logic. The reset scheme for the chip is shown in fig 4.

For the digital side, all the blocks have asynchronous reset. The long-debated pros and cons of asynchronous and synchronous reset are summarized in [18]. A recommended practice is to have an asynchronous reset for all the flip-flops but to synchronize the asynchronous reset at the top level. The reset synchronizer is made of two flip-flops connected in a chain. The input of the first flip-flop is connected to the supply voltage. The output of the second flip-flop is the synchronized reset. While the external reset (n_rst) is asserted

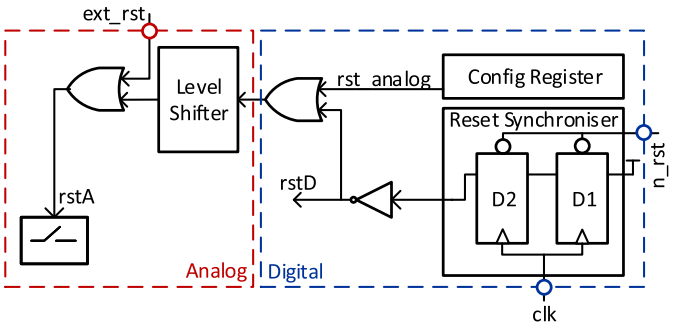

Fig. 4. Reset generation logic.

the digital reset ($rstD$) is asynchronously asserted. Upon de-assertion of the external reset, $rstD$ is also removed in two clock cycles. Thus, the assertion of reset is asynchronous and reset removal is synchronous. This methodology eliminates the issue of flip-flops getting out of reset in the metastable state due to asynchronous reset. The digital reset also resets the analog section. Additionally, writing to a configuration register can independently reset the analog section.

V. Layout Considerations

The main challenge in any mixed-signal design is the coupling of the substrate noise from the digital section to the analog section and interfering with the operation of the sensitive analog nodes [19]–[22]. For the ASIC handling currents with femtoampere sensitivity, the issue is particularly challenging. The various sources of noise in a mixed-signal environment are well studied and certain standard practices exist to minimize the impact [23].

Prudent floor planning of the design was undertaken to minimize the coupled noise from different sections. The cross-section of the designed ASIC is shown in fig 5.

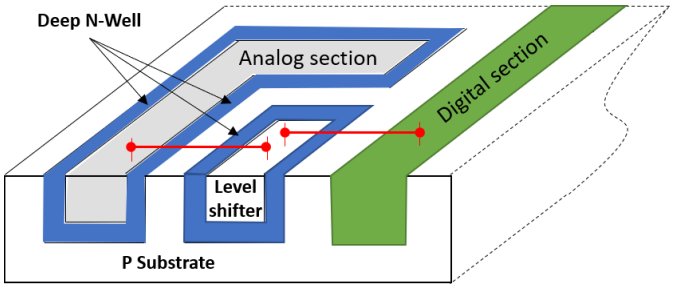

Fig. 5. Substrate separation using Deep N Well.

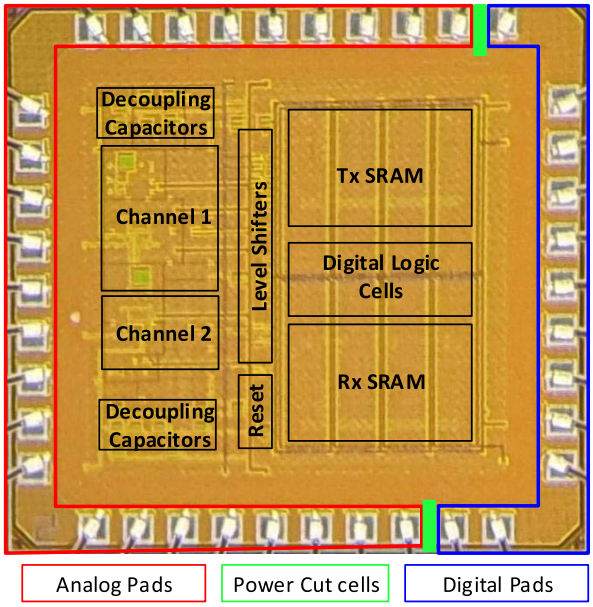

Fig. 6. Micrograph of the ASIC designed in 130 nm.

The entire analog section is surrounded by an N-Well with a guard ring tied to 3.3 V. A deep N-Well connected to this N-Well ring isolates the analog section from the rest of the chip. The current to be measured by the chip is received by the input stage of the OTA realized using PMOS transistors. This input stage is surrounded by another guard ring. The NMOS devices of the analog section are also surrounded by guard rings tied to analog ground. The level shifter module is housed within another N-Well Deep N-Well combination. The digital section has separate substrate taps connected to digital ground.

The micrograph of the ASIC showing different design blocks is shown in Fig.6. The chip occupies an area of 1920.37 μm $\times$ 1832.59 μm. In the analog section, channel 1 with the feedback capacitor of 5 pF and the charge generation capacitor of 4 pF occupies the maximum area. The area in the digital section is predominantly consumed by the SRAM modules. The other digital logic is realised with 4052 logic cells. The analog and digital pads are separated by power cut pads. Two sets of power and ground pads are provided for both the analog and digital sections. To ensure a similar environment for the input pins of channels 1 and 2, they are surrounded on both sides by common-mode voltage.

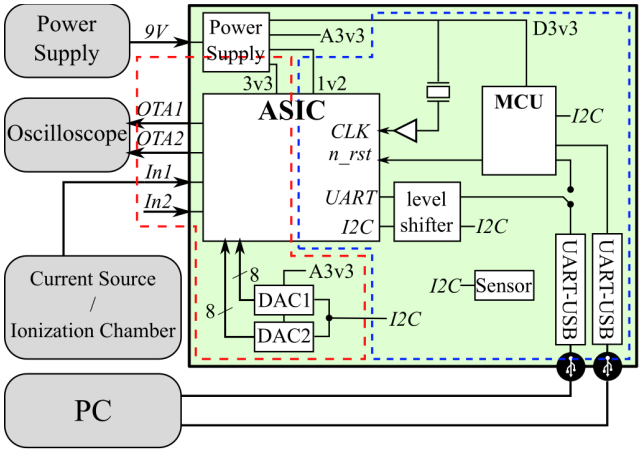

Fig. 7. Test board architecture and experimental setup. Digital island is framed in red on the left-hand side and analog section in blue on the right-hand side.

VI. Test Bench Details

The chip is directly wire-bonded to an FR4 based test board. Great care was taken in the placement and the layout of the printed circuit board (PCB) to separate analog and digital components to limit as much as possible noise injection from the latter. For this reason, four power buses are used, as seen in Fig. 7. Input tracks' layout is done to isolate them as much as possible from any sort of charge injection, with the help of a common-mode voltage ring and by removing all copper layers beneath them.

On-board communication is performed *via* an I2C bus. Either the chip or the microcontroller (MCU) can be used as the master to program the digital-to-analog converters that provide bias and threshold voltages to the chip and to read temperature and humidity data from the on-board sensor. Data transmission to the external world is done through two serial communication lines. It would also be possible to connect the chip's serial output to the MCU if one wants to process data on-board. The MCU can also trigger the chip's digital reset signal n_rst.

During operation, channel 2 input would typically be left open to measure leakage current, however, for the calibration tests, it was also connected to a Keithley 6430 current source, like channel 1. A computer was used to send parameters and process data read on the serial buses using MATLAB. To determine the femtoampere sensitivity of the integrators, their output voltage was directly recorded with an oscilloscope.

VII. Characterisation of ASIC

Ionisation chambers generate a negative current, therefore the ASIC is designed to measure only the current with that polarity, flowing *out* of the chip. However, for easier representation in all the plots that follow, it was decided to represent this input current as positive.

The data packet of eight 32-bit serial data from the ASIC are aligned by the measurement script in MATLAB by identifying a header pattern. Based on different counts received, two different currents are calculated. Using the interval count N_{int}, the DSM current is calculated as

$$I_{\text{DS}} = \frac{\zeta C_{\text{f}}}{N_{\text{int}} t_p}, \tag{1}$$

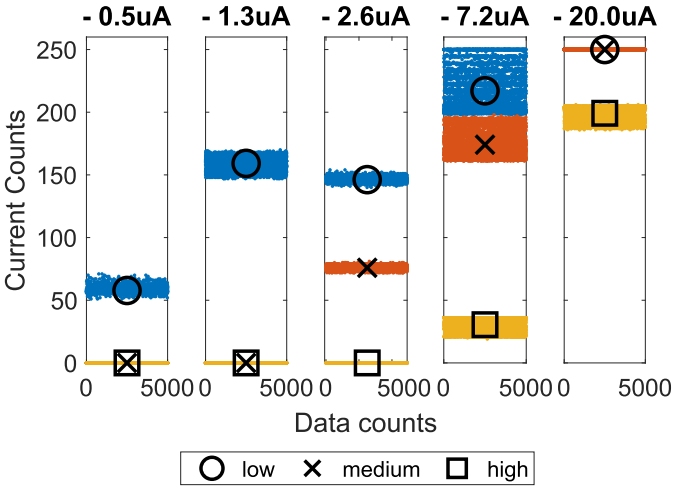

Fig. 8. Charge balancing counts for different current ranges.

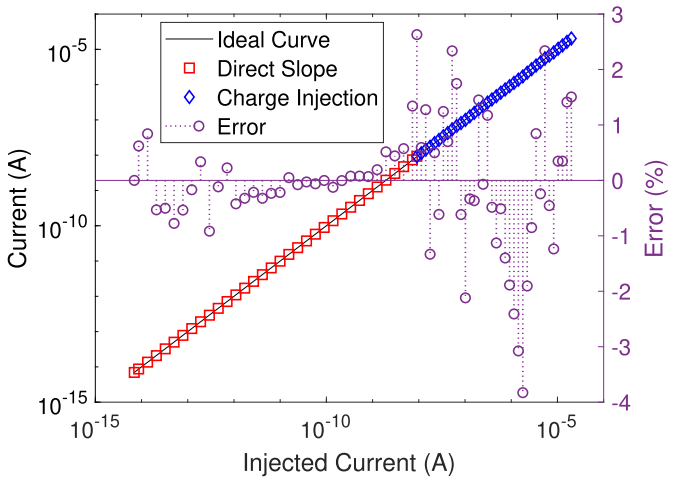

Fig. 9. Measured current from −7 fA to −20 μA, compared to the injected current.

where ζ is a constant that is found out by calibration, C_f is the feedback capacitance, and t_p is the period of the system clock. The theoretical value of ζ is calculated from the threshold difference of the first two comparators and the hysteresis ratio. The variation in the feedback capacitance from the ideal value is also accounted for in this factor.

The current using the CB method is calculated as

$$I_{CB} = \frac{aN_{low} + bN_{medium} + cN_{high}}{T_{window}}, \quad (2)$$

where N_{low}, N_{medium}, and N_{high} correspond to the number of low charge, medium charge, and high charge pulses generated in a fixed time period, T_{window}. The proportionality factors a, b, and c corresponds to the net charge generated by the different charge generation blocks.

The variation in data counts for different input currents is shown in Fig. 8. The threshold voltages of the comparators used for these plots are 1.7 V, 1.95 V, and 2.9 V for comparators 2, 3, and 4 respectively. For an input current of −500 nA, the integrator output crosses the 1.7 V level enabling the low charge branch. The charge balancing is handled by only the low charge branch for this current range. As the current increases above −2 μA, the second threshold is crossed and the medium charge counts are generated. Further higher currents close to −7 μA triggers all the comparators and the high charge branch also gets enabled. For the current above −20 μA, the digital counters reach the maximum possible value in a measurement time window. For the monostable period of 160 ns and a time window of 40 μs, the maximum value is 250. The digital section operates at 100 MHz for the generation of precise timing for the monostable and for measuring the time interval precisely in DSM method.

A. Characterisation in Controlled Environment

The full measurement range was tested at controlled room temperature using a Keithley 6430 current source. DSM method was selected for current up to −9 nA and CB was used for the upper range. Fig. 9 shows the results for a combination of both methods from −7 fA to −20 μA. It can be seen that the CB method is less accurate than DSM. Smaller current steps are thus used above −9 nA to have a better insight of the evolution of the error. In particular, a peak arises for a current of −1.8 μA, exactly where the third comparator's threshold is crossed, enabling the injection of *Q_med*. This effect is inherent to the transition between several levels of charge injection, but it could be smoothed by having more levels with charge values closer together.

The chip has a second channel which is designed to be used for leakage compensation. However, leakage currents appeared to be positive for this chip, making it impossible to directly measure them. Instead, the first point in the sweep where a net current is measured ($|I_{in}| > |I_{lkg}|$) was used as an estimate of the leakages according to (3). With this estimate of $I_{lkg,1} = 6.97$ fA correcting the following points, the measurement error was calculated relatively to the injected current given by the current source and is contained between −4 % and 3 %. One should notice that the first point is thus corrected by itself and has a relative error of 0 %.

$$I_{lkg,1} = |I_{in,1}| - |I_{meas,1}| \quad (3)$$

The influence of temperature on the leakage was studied between −10 °C and 50 °C. The temperature was swept with steps of 10 °C and held constant for 2.5 hours per step. Relative humidity was kept below 5 % to avoid any influence. As mentioned above, the circuit is not able to measure positive current. It was thus decided to inject −50 fA in both channels and use (3) to extract the effective leakage which is plotted on Fig. 10. Even though the depicted values are the cumulative leakage for each channel, since it is dominated by electrostatic discharge (ESD) diodes, the leakage variation effectively represents that of the ESD diodes. Indeed, the leakage currents of the two stacked ESD diodes should theoretically compensate each other, but if their matching is not perfect, a net current is measured. This explains why, even if designed identically, the two channels do not have the same leakages.

To effectively compensate the leakages variation with temperature, each ASIC should be characterised with a

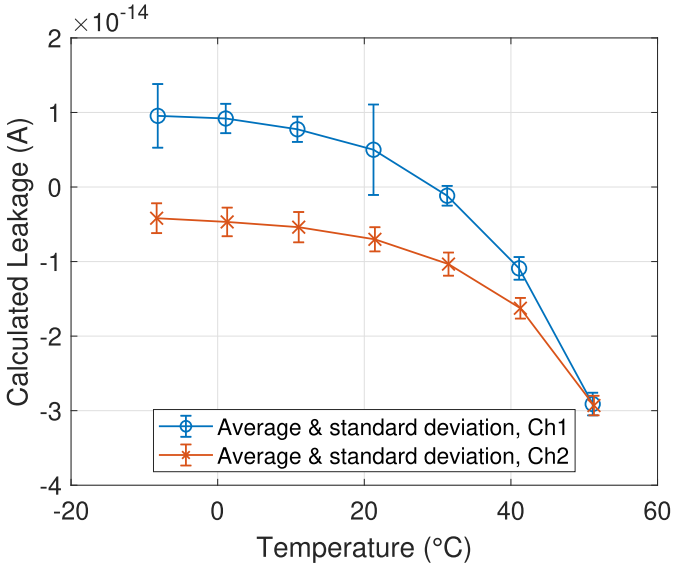

Fig. 10. Leakage currents for both channels. The measured current was averaged during each temperature step.

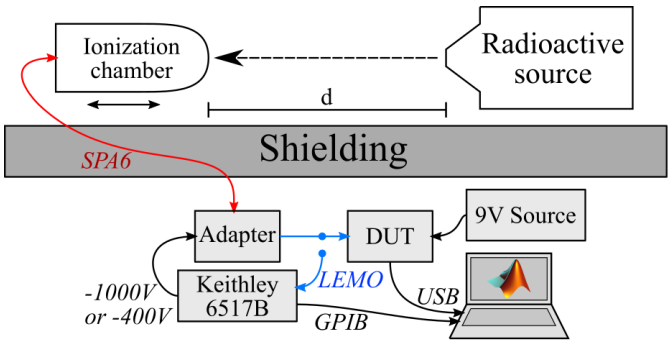

Fig. 11. General setup used for irradiation tests. All measurement electronics were deported behind a concrete wall and only the ionisation chamber was irradiated.

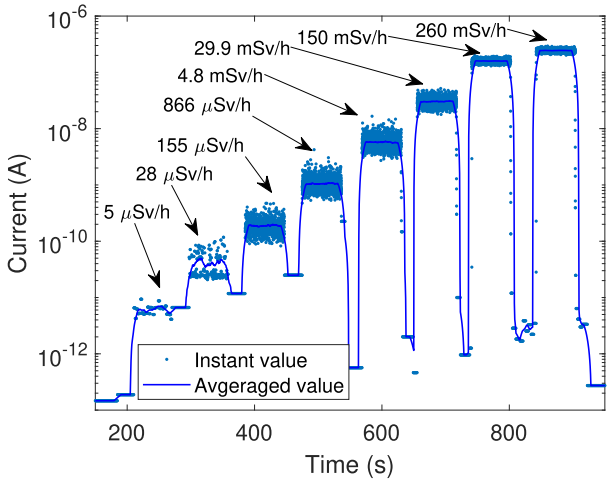

Fig. 12. Current measurement from the ASIC with an ionisation chamber exposed successively to several dose rates, for one minute each.

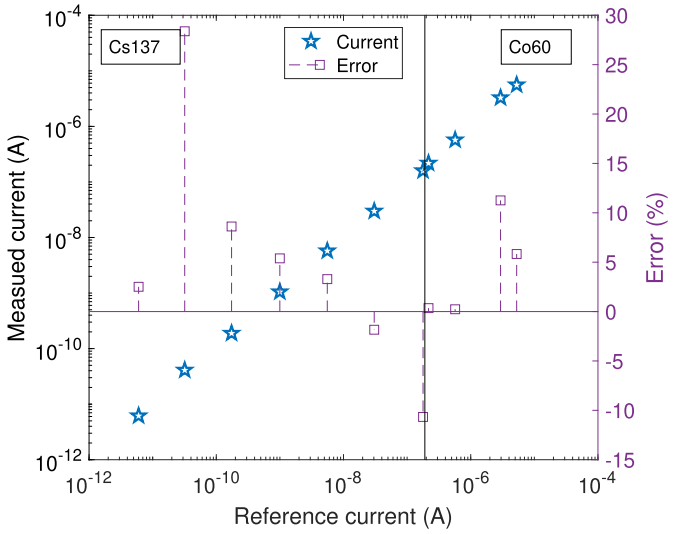

Fig. 13. Average measured current compared to the reference current for dose rates ranging from 5 μSv/h to 7.4 Sv/h. The vertical black line represents the separation between the two types of sources.

temperature cycling to determine the correction profile. Then using this profile and the current measured by channel 2, the net leakage of the primary channel could be corrected.

B. Characterisation With Ionisation Chamber

The circuit was tested in real conditions at CERN in two different irradiation facilities used to calibrate ionisation chambers. The first one uses Cesium 137 (^{137}Cs) sources with activities from 300 MBq to 3 TBq while the second has a Cobalt 60 (^{60}Co) source of 110 TBq. As shown in Fig. 11, a Centronic IG5-A20 ionisation chamber was placed on a moving table and the distance d separating the source from the chamber was automatically adjusted in function of the desired dose rate, ranging from 5 μSv/h to 260 mSv/h for the ^{137}Cs and from 160 mSv/h to 7.4 Sv/h for the ^{60}Co. An SPA6 cable was used to convey the polarization voltage of -1000 V to the chamber and the measurement signal to the control room. Then, an adapter separated the high voltage from the signal, which was successively measured by a Keithley 6517B electrometer and by the ASIC. A Windows PC with MATLAB was used to program the devices and record data.

The measured current is averaged for each exposition time and compared to the one measured by the electrometer. Fig. 13 shows the averaged measured current and the reference current. This type of comparative measurement made it possible to eliminate uncertainties in the delivered dose rate, which was either given by theoretical values or by an auxiliary chamber. However, as the radioactive sources are brought to the collimator by a pressurized air system, their position is not always identical and small variations in radiation between successive expositions might occur. Their value was measured to be around 2.5 % for a given position. In results shown in Fig. 13, except from the point at 28 μSv/h which was particularly noisy, the linearity is good across the whole measured range, with a global relative error between $\pm$10 %. Observation of the OTA output voltage showed that the signal generated by ionisation chambers can be very noisy. The noise

associated with current read out integrators is studied in detail in [24]. A similar analysis resulted in a cumulative noise voltage of 119 μV in frequency band of 1 mHz to 10 GHz at the OTA output. However in the real application scenario when the ASIC was interfaced to an ionisation chamber the mean value of the noise voltage observed at the output node was around 100 mV. Debouncing logic and comparator hysteresis limit the effect of this noise, nevertheless, it also explains why measurements of ionisation chamber current is less accurate than that of the current from the Keithley source.

VIII. Conclusion

The ASIC presented was demonstrated to meet the specification requirement of ionisation dose rate measurement for CERN radiation monitors. Though the measurement linearity in an application scenario is dictated by the ionisation chamber which is calibrated to be around 10%, the accuracy of the ASIC could be improved further for use in other applications demanding stricter error limits. The presented modular architecture can be easily adapted to have finer charge generation blocks decreasing the quantization error appearing during band switching. The ASIC with its femtoampere sensitivity and 189 dB dynamic range can very well be used for applications in various fields, like read-out of bio-nano sensors [25], structural health monitoring using piezoelectric sensors [26] or device characterisation.

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