A Low-Noise Instrumentation Amplifier With Built-in Anti-Aliasing for Hall Sensors

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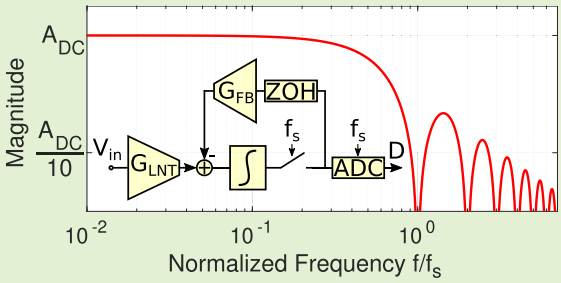
***Abstract*—We present a compact, versatile Hall readout system with digital output, fully integrated in 180 nm technology. The core of the system is an instrumentation amplifier architecture that provides inherent anti-aliasing filtering, where the anti-aliasing characteristic is locked into a shape that maximally prevents aliasing to low frequencies. The efficiency for blocking out-of-band white noise is comparable to that of a second-order filter, eliminating the need for an explicit anti-aliasing filter before the ADC. Chopping/spinning is applied for up-modulating offset and 1/f noise to just beyond the signal band. A mostly-digital ripple reduction loop (RRL) is added for mitigating offset-related dynamic range limitations. In this, a bilinear integrator is introduced for eliminating the impact of the RRL on the system's DC gain. Moreover, the resolution of the DAC generating the analog offset compensation is reduced significantly, and the effect thereof is eliminated by digital noise cancellation logic. The one-step amplification and the simple, low-resolution DAC for offset compensation both aid in keeping the area footprint low: the analog circuits (including DAC and ADC) only occupy 0.21 mm^2. Notable performance characteristics are an input-referred noise floor of 55 nT/$\sqrt{\text{Hz}}$ within a 410 kHz bandwidth, a current consumption of only 5.1 mA, and a 47 dB dynamic range. The amplifier architecture can be easily applied as an analog preconditioning circuit in other sensor readout situations as well.**



***Index Terms*—Instrumentation amplifiers, sensor readout, hall sensor, in-the-loop sampling amplifier (ILSA).**

I. Introduction

THE subject of this work is a compact, all-round integrated Hall readout system that can serve a large variety of applications. It incorporates many state-of-the-art techniques: Hall plate (HP) readout with current spinning [1]–[8], low-noise signal amplification [9]–[11], the application of zero-banding [7], [9], a digitally assisted ripple reduction loop (RRL) [1], [4], [12], anti-aliasing filtering [1], [13], [14], and analog-to-digital conversion (ADC) [1], [9], [12]–[14]. Combining all these functionalities creates opportunities for exploiting synergies between the different techniques. The result is a compact, versatile Hall readout system in which the analog interfacing chain from the weak Hall signal up to the ADC is essentially a single circuit. Targeted specifications of our work are a Hall-only sensor with a bandwidth of at least 400 kHz and a (post-ADC) noise level not larger than 50 μT_{rms}. This allows to address applications ranging from bandwidth-demanding magnetic-field current-sensing [15]–[17], up to high-accuracy magnetic position sensing [18]. Note that bandwidth can be easily traded for resolution by low-pass filtering in the digital domain. Furthermore, within our Hall readout system a Nyquist-rate ADC will be used, which adds to the flexibility and versatility of the overall sensor system, because the ADC can then easily be multiplexed, e.g. over multiple readout channels, for readout of an on-chip temperature sensor, etc.

Within the open literature, the presented Hall readout system can be situated between two extremes. On the one side, there are efforts to stretch performance specifications such as bandwidth and resolution. At this part of the spectrum we find hybrid dual-path set-ups that combine Hall with inductive pick-up [6], [7]. The high performance, for instance a notable bandwidth of 3 MHz, comes at an inherent large cost in terms of silicon area (due to the large required coils) and design complexity (since the sensitivities of the hybrid paths need to be adequately matched). Therefore, this hybrid multi-path approach cannot be easily scaled for lower chip area. At the other end of the spectrum we have [19], which presents the readout of a large array of Hall plates. Because 160 copies of the readout chain operate in parallel, in this niche the area is of primary importance. Hence, the design in [19] is fully optimized for the particular application, providing low bandwidth and so-called baseline suppression to only detect changes in the magnetic field. However, this design is not

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suitable as a general purpose Hall sensor because DC magnetic fields are rejected by autozeroing.

Our work approaches in some aspects that of [20], which also features a notably small area. This work is however optimized toward low current-operation and hence does not reach the high bandwidth and low-noise performance we target. Furthermore, the signal amplification in [20] is time-based, hence a clock that is stable over process, voltage and temperature (PVT) variations is required to have a well-defined gain. In contrast, we retain in our solution the advantage of defining the gain in a ratiometric way, as is the case in many amplifier topologies.

The main progress introduced by our work revolves around the design of an instrumentation amplifier architecture that provides inherent anti-aliasing filtering. Also conversion to the digital domain is incorporated. These aspects are typically not included in Hall sensor publications, which means that the power and layout costs associated with anti-aliasing filtering and A/D conversion are also not considered. It is however exactly in the combination of these aspects that we can demonstrate a strong synergy that allows to fully eliminate any explicit anti-aliasing filtering, arriving at a compact, low-noise readout architecture with a digital output.

II. Low-Noise Amplifier With Implicit Anti-Aliasing

A. Basic in-the-Loop Sampling Architecture

In many sensor systems, an instrumentation amplifier (IA) is used as a first low-noise amplification stage. The three-opamp based IA [21], the current feedback IA (CFIA) [10], [11], [22], [23] and the capacitively coupled IA (CCIA) [24] are three standard IA topologies that have proven records. In the context of low-noise amplification, three-opamp based IAs are not preferred [11], [25], leaving the CCIA and the CFIA as potential candidates. This work was built on the CFIA structure, but the core in-the-loop-sampling concept (see below) might also be applied to the CCIA structure. Within the CFIA family, many higher-order structures have been proposed in literature [10], [22], but even up to the present the simple first-order structures remain attractive as a means to arrive at area-efficient low-noise amplifiers [23]. In our work, an innovative adaptation of a first-order structure [26] is proposed. Moreover, we aim for a one-step high-gain amplification. Because Hall signals are on the order of 1 mV, the needed gain is as high as 1000×. Traditionally, the gain of the low-noise amplification stage is not that large, sometimes even as low as 10× [3]: high enough to alleviate the noise requirements of all subsequent blocks, but low enough that offsets cannot cause problems. The implication of our choice for a one-step high gain is that the problem of offset will have to be fully addressed. This will be discussed further on in Section III.

The block diagram of our proposed instrumentation amplifier is shown in Fig. 1.a. It is called an In-the-Loop Sampling Amplifier (ILSA). The forward path consists of a low-noise transconductance (LNT) with transconductance G_{LNT} followed by a current-to-voltage integrator. An important innovation is that a sample and hold (S&H) block is added *inside* the feedback loop, at the end of the forward path.

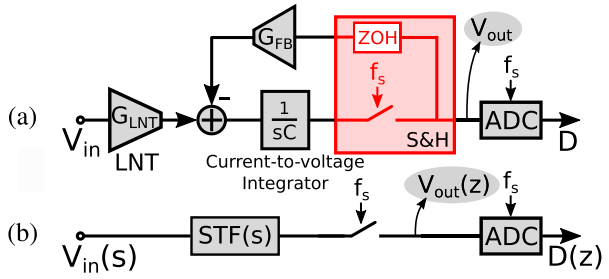

Fig. 1. (a) ILSA block diagram (b) Equivalent system.

The S&H functionality can be represented by a sampler, operating at sample frequency f_s, and a zero-order hold (ZOH) block. The sampling operation in the ILSA is purely analog and therefore does not introduce any quantization error. Digitization occurs only *after* the analog feedback loop: each analog sample taken by the S&H block is converted to the digital domain by an ADC. Note that the sampling frequency of the ADC and the S&H are exactly equal. Because the ADC and ILSA are required to operate in perfect synchronism, the ADC has been explicitly depicted in Fig. 1.a. We propose to use a Nyquist-rate ADC, implying that the ADC does not have a state that persists from one sample to the next. Because the ADC taps its input signal from the S&H block of the IA, there is a stable input signal available over a full sample interval $T_s = 1/f_s$. Therefore, any type of Nyquist-rate ADC (SAR, pipelined, incremental, etc.) is readily applicable.

Let us now analyze the ILSA in more detail. Its DC gain, denoted by A_{DC}, has not been altered by our adaptation, and is, as in a traditional CFIA, set by the ratio of two transconductances:

$$A_{\mathrm{DC}} = \frac{G_{\mathrm{LNT}}}{G_{\mathrm{FB}}} \tag{1}$$

The transconductances are preferably defined by passive components (resistors), which allows to implement these functions with good linearity. As A_{DC} is set ratiometrically, it shares with traditional CFIAs that it is robust against PVT variations (taking proper layout techniques into account). The main novelty of the proposed IA resides in the frequency characteristic that substantially reduces noise-aliasing. In order to quantify the anti-aliasing functionality, sampled-data analysis [27] is performed on the system in Fig. 1.a to find the following expression[1] for the output V_{out}:

$$V_{\mathrm{out}}(z) = \left[V_{\mathrm{in}}(s) \cdot \underbrace{\frac{G_{\mathrm{LNT}}}{sC} \frac{1 - z^{-1}}{1 - (1 - \frac{G_{\mathrm{FB}} T_s}{C}) z^{-1}}}_{\mathrm{STF(s)}} \right]^* \tag{2}$$

In this $T_s = 1/f_s$ is the sample period, $z = e^{sT_s}$ and the *-superscript denotes the sampling operation [27]. STF(s), as indicated in (2), represents the signal transfer function that V_{in} experiences *before* sampling. From (2) the equivalent system-level representation visualized in Fig. 1.b is obtained.

[1]Continuous-time signals will be represented by their Laplace transform in this paper (e.g. $V_{\mathrm{in}}(s)$), whereas sampled-data signals will be represented by a z-transform (e.g. $V_{\mathrm{out}}(z)$).

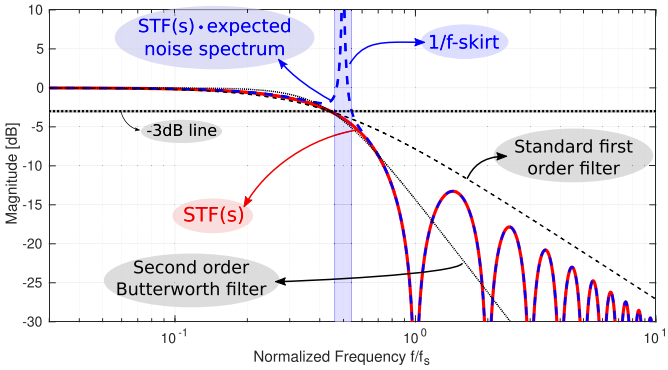

Fig. 2. Normalized transfer function (before sampling) of the ILSA's core STF(s), compared to a conventional 1st-order and 2nd-order Butterworth filter with the same bandwidth. The multiplication of STF(s) and the normalized expected noise spectrum is also displayed, including a 1/f-skirt (modulated offset and 1/f noise) due to chopping (see Fig. 3).

Note that the STF in (2) has a discrete-time pole $z = 1 - \frac{G_{FB}T_s}{C}$. To further fortify the ILSA against PVT variations, it is made maximally stable by requiring the nominal pole position to be at $z = 0$, leading to the design equation:

$$\frac{G_{FB}T_s}{C} = 1 \tag{3}$$

Using (1) and (3), (2) reduces to:

$$V_{out}(z) = \Big[V_{in}(s) \cdot \underbrace{A_{DC}\frac{1 - z^{-1}}{sT_s}}_{\text{STF(s)}} \Big]^* \tag{4}$$

The STF of the nominal ILSA architecture (4) is plotted in Fig. 2. To focus on the filtering, the plot is normalized (i.e. the gain factor A_{DC} is removed). The first-order characteristic of a standard CFIA exhibiting the same bandwidth ($= 0.44 \times f_s$) is also plotted for comparison. By simply moving the S&H block inside the loop, notches are created at multiples of the sample frequency f_s, which provides inherent anti-aliasing filtering.

In order to further quantify the anti-aliasing performance of the system, we use as an anti-aliasing figure-of-merit (AAFoM) the relative increase of in-band noise power due to aliasing, assuming white noise at the input of the amplifier. This relative increase in noise power is for the ILSA:

$$\text{AAFoM} = \frac{\int_{f_s/2}^{+\infty} |\text{STF}(j2\pi f)|^2\, df}{\int_0^{f_s/2} |\text{STF}(j2\pi f)|^2\, df} \simeq 0.29 \tag{5}$$

Aliasing thus causes an in-band noise power increase of only 29 %. Evaluating this AAFoM for the classical first-order CFIA with the same bandwidth (see Fig. 2), the in-band noise power increase amounts to 89 %. We can also compare to a second-order filter. Taking as transfer function a second-order Butterworth transfer function, again with the same bandwidth as the ILSA (see again Fig. 2), the relative increase of in-band noise due to aliasing is 20 %, which is only slightly better than the 29 % increase of the ILSA. This confirms that the ILSA's anti-aliasing performance is significantly better than a first-order transfer, and close to that of a second-order system.

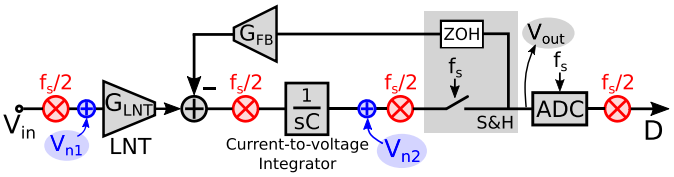

Fig. 3. Block diagram of the ILSA with choppers added, operating at $f_{chop} = f_s/2$. Two additional signals are added: V_{n1} represents the HP and LNT voltage offset, while V_{n2} represents the voltage offset of the current-to-voltage integrator.

Important to note is that the above AAFoM figures relate to the situation where the full bandwidth is used. If the bandwidth can be reduced, e.g. by filtering in the digital domain, the relative advantage of the ILSA becomes even larger. This is because the frequencies where the ILSA experiences aliasing (which is quantified by the STF shown in Fig. 2), are primarily around $f_s/2$. These aliased components can therefore be filtered out digitally, at the cost of some bandwidth. Almost no noise folds towards DC thanks to the broad notches around multiples of f_s. We repeat here that the advantageous shape of the anti-aliasing filtering entirely comes from the tight coupling of the analog sampling by the S&H and the digitization by the ADC after the ILSA.

It is instructive to discuss the size of the integration capacitor C (Fig. 1), as this is an important component to set the bandwidth of the sensor system. Because most sensor bandwidths are relatively low, the associated time constants tend to require a substantial area when implemented on-chip. For a compact readout circuit, the magnitude of the integration capacitance is therefore of concern. Combining (1) with (3), an expression for the magnitude of the integration capacitance is obtained as:

$$C = G_{LNT}\frac{T_s}{A_{DC}} \tag{6}$$

The value of the first factor in this expression, G_{LNT}, is largely determined by the targeted noise floor of the IA. The second factor, T_s, is also constrained, as will be explained in the next section. The last factor is the DC gain A_{DC}. So it becomes clear that the choice to go for a one-step high gain is optimal for reducing the area cost of the integration capacitor.

B. Introducing Chopping/Spinning

For a one-step amplification with high gain, it is essential to take offset into account already at the system level. This is especially the case because Hall plates are known to exhibit large offsets [28]. We now refer to Fig. 3. In order to separate offset from the useful magnetic signal, Hall plate current-spinning/chopping is applied. Each spin phase is attributed a length $T_s = 1/f_s$. The Hall plate spinning up-modulates the magnetic signal and can be represented by a chopper operating at $f_{chop} = f_s/2$ at the input in Fig. 3. Two more analog choppers that operate synchronously with the spinning are inserted: one in front of the current integrator, and one in front of the S&H. Finally, there is also a digital chopper that demodulates the ADC output. Note that in this scheme, the two transconductances G_{LNT} and G_{FB} are chopped, while the integrator is not. The dynamic behavior of the transconductances

can easily be made substantially faster than the bandwidth limitation introduced by the integrator. Hence, with this choice of chopper positions the STF of the chopped ILSA remains identical to the non-chopped variant, i.e. as in (4).

In Fig. 3, two important offset sources are introduced. The first one, V_{n1}, represents the Hall plate offset as well as the input-referred offset and 1/f noise of the LNT. The effect of the frequency translations can be referred to the input, resulting in an expected input-referred noise spectrum consisting of white noise and up-converted offset and 1/f noise. When accounting for the signal transfer function, we obtain the multiplication of STF(s) with this equivalent input noise signal shown in Fig. 2 (in dashed blue), where we normalized the noise power in order to focus on the frequency-selective effects that occur. The net effect is that in the sampled signal the 1/f noise is mostly concentrated in the frequency region from about the 3 dB bandwidth up to $f_s/2$. Therefore, the 1/f noise can be removed by filtering in the digital domain. The basic ILSA architecture has a 3 dB bandwidth about 89 % of f_{chop}, leaving a frequency band of 11 % of f_{chop} to be occupied by 1/f noise. This is almost an optimal situation, and allows us to make the following claim: the ILSA architecture provides the best-in-class ratio of bandwidth relative to chop frequency. In order to understand the significance of this claim for Hall sensor systems, it needs to be understood that there are practical limits with which a Hall plate can be reliably spun. In our system, each spin phase occupies $T_s = 1\,\mu$s, and the implied chopping frequency is therefore 500 kHz. Now, given the fact that f_{chop} is constrained, we can still try to maximize the bandwidth by extending it as close as possible to f_{chop}. This is exactly what the ILSA architecture allows us to do, and so the 400 kHz bandwidth target can be easily met with a perfectly feasible 1 μs/phase spinning scheme.

The second offset source V_{n2} in Fig. 3 represents the offset of the integrator block. As it is a current-to-voltage integrator (see also Fig. 11 below), its opamp voltage offset can be output-referred with approximate gain 1. The position of the choppers is such that V_{n2} contributes directly to the system's residual offset. However, since this integrator offset appears at the output without amplification, the equivalent offset is 1000× smaller when referred to the input of the ILSA.

C. First-Order Versus Higher-Order ILSA

Until now, we focused on a first-order ILSA architecture. Higher-order ILSA architectures are however perfectly possible. Let us consider the second-order variant, shown in Fig. 4 (inset). The stability of the second-order ILSA turns out to be much more critical. A reasonable compromise results in the coefficient set $a_0 = 2/3$, $a_1 = 6/5$, $b = 1$, leading to the STF also shown in Fig. 4. The bandwidth has dropped with 57 % compared to the first-order system. It is clear that when it comes to anti-aliasing filtering, the second-order ILSA outperforms the first-order ILSA. However, when aiming for the same bandwidth, the loss in relative bandwidth would have to be compensated by increasing f_s, which requires spinning at a 1.75× faster rate, and the ADC then needs a proportional increase in conversion speed. Finally, it can also be expected that the second integrator requires extra area and current.

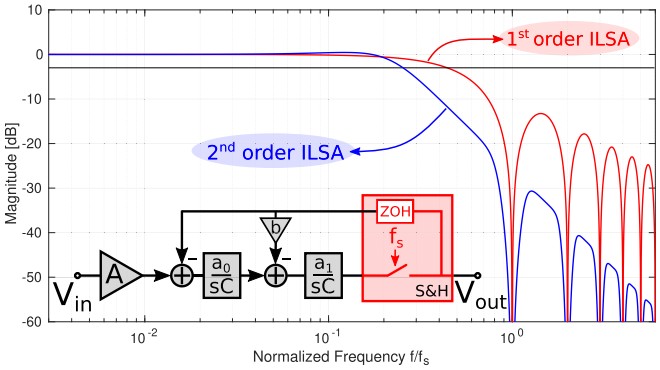

Fig. 4. Second-order ILSA structure (inset) and STF with a comparison to the first-order ILSA STF.

Taking these elements into account, the first-order ILSA was found to be more in line with the high-bandwidth and low area targets we pursued.

D. Position of the ILSA Relative to Related Prior Art

The ILSA architecture is on the border of different fields of expertise. Hence, depending on the reader's background, different prior art may come to mind. We discuss two of them.

There is a first link with continuous-time Sigma-Delta modulation (CTSDM), which shares with the ILSA that in-the-loop sampling is applied at the end of the forward path. Actually, by incorporating a quantizer in the loop, a first-order CTSDM would be formed. However, by doing so, a lot of quantization noise is added and the design of a CTSDM then concentrates on tackling the effect of this extra noise contribution. This is done by a combination of oversampling and optimized noise shaping. The resulting design approach as well as its properties are very different from the ILSA, which focuses on low-noise amplification with inherent anti-aliasing filtering. For this reason, an ILSA and a CTSDM (although similar at first sight) have very distinct properties.

Another place where in-the-loop sampling appears is in some chopper-stabilized operational amplifiers [29], [30]. For instance, in [29] a sampling-based notch filter is inserted in one path of a frequency-compensated amplifier in order to block offset ripple. As the measured open-loop gain and phase characteristics confirm [29, Fig. 11], this amplifier has a very classical 20 dB/decade slope over nearly five decades. Therefore, applying proportional feedback to this circuit (e.g. to have a definite gain of 1000) would, as far as anti-aliasing functionality concerns, result in a standard first-order behavior, which as explained before is much less efficient than the anti-aliasing notches exploited in the ILSA.

III. Ripple Reduction Loop

Until now we have shown that, by incorporating chopping and spinning in the ILSA architecture, offset and 1/f noise is translated to the edge of the Nyquist band, where it can be removed by digital filtering. In practice, the offset in Hall plates can be substantial, and in view of the high gain we want to ensure that even in worst case the chopped offset ripple does not saturate the amplifier nor negatively affects the

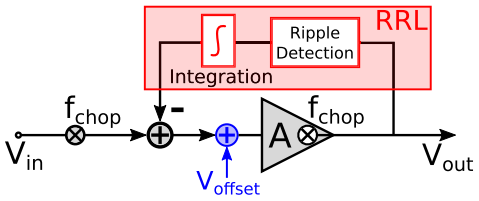

Fig. 5. Overarching concept of a ripple reduction loop (RRL).

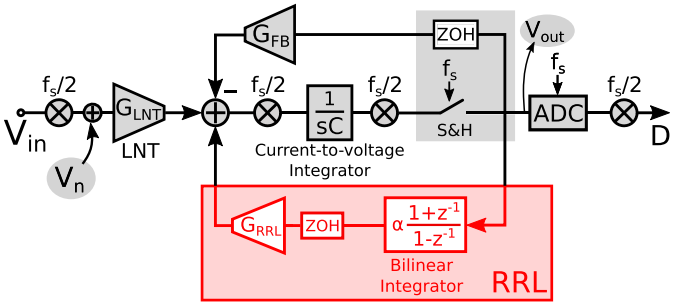

Fig. 6. Block diagram of the ILSA with a discrete-time RRL employing a bilinear integrator. V_n represents the primary offset source of the system.

dynamic range. This is possible by using a RRL which compensates the offset at the input.

There are quite a number of publications in which RRLs are used [4], [6], [7], [10], [24]. The overarching structure of these prior art RRLs is shown in Fig. 5. The RRL detects the amplitude of the offset ripple at the output V_{out}, and feeds a compensating signal back to the input through an integrating path. In many publications the RRL operates in continuous-time [6], [10], [31], [32], but also switched-capacitor [7] and digital approaches [1], [4], [9], [12] have been explored.

Considering the fact that part of the ILSA already operates in discrete time, it is obvious to consider discrete-time RRLs that operate in perfect synchronism with the ILSA and the ADC. The samples feeding the RRL are then exactly those samples in which aliasing has been suppressed. Compared to the cited prior art, we have explored two innovations in the RRL. A first aspect is the use of a bilinear integrator instead of a regular integrator, which makes it possible to broaden the notch bandwidth without affecting the DC gain. A second aspect is the use of a mostly-digital RRL in which the DAC has a reduced resolution (LSB $= 16.5\ \mu$V), where the associated quantization effects are compensated in the digital domain.

A. RRL With Bilinear Integrator

A block diagram of an ILSA with discrete-time RRL is shown in Fig. 6. V_n represents the primary offset of the system (from HP and LNT) which is to be compensated by the RRL. The main difference with prior work is the controller transfer function in the RRL:

$$H_{RRL}(z) = \alpha \frac{1+z^{-1}}{1-z^{-1}} \tag{7}$$

This is known as a bilinear integrator [33], [34], where α represents an integration constant. Unlike a standard

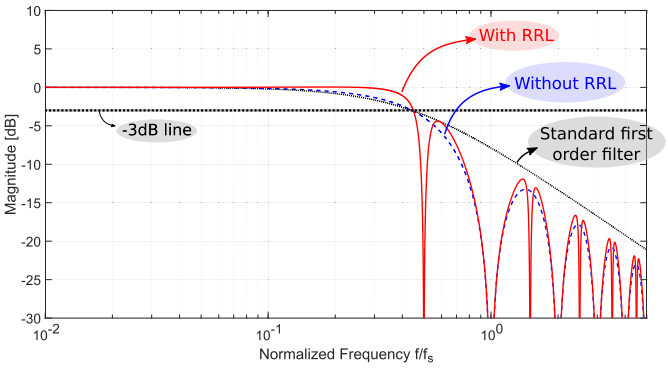

Fig. 7. Normalized STF of the ILSA without and with the bilinear integrator based discrete-time RRL.

integrator it has a zero at $f_s/2$. This helps the RRL feedback path to block the frequencies where the useful signal resides.

Thanks to the synchronous sampling applied in the full system, the resulting sampled-data system can again be analytically solved and brought in the equivalent form of Fig. 1.b, where the STF(s) takes the form:

$$\mathrm{STF}_{\mathrm{ILSA+RRL}}(s) = A_{\mathrm{DC}} \frac{1-z^{-1}}{sT_s} \frac{1}{1-\frac{G_{\mathrm{RRL}}}{G_{\mathrm{FB}}} z^{-1} H_{\mathrm{RRL}}(-z)} \tag{8}$$

Evaluating this expression for $s = 0$ allows to show that the DC gain of the system is always A_{DC}, independent of the value of α, thanks to the zero in (7) at $f_s/2$. When performing the same analysis using a standard integrator, the DC gain evaluates to $A_{\mathrm{DC}}/\left(1-\frac{G_{\mathrm{RRL}}}{G_{\mathrm{FB}}}\frac{\alpha}{2}\right)$. This shows that with a standard integrator the DC gain of the amplifier is affected by the RRL. In principle, the latter expression allows to compensate for the DC gain variation caused by a RRL with a normal integrator. This however requires knowledge of α and the $G_{\mathrm{RRL}}/G_{\mathrm{FB}}$ ratio. As a result, variability of these variables due to limited matching and PVT variations also needs to be taken into account. This becomes progressively more important when the RRL is sized for a faster response (larger values of α), as is the case in our system. Therefore, in our work the inherent separation of DC gain from the RRL behavior obtained by the use of a bilinear integrator was preferred.

The normalized STF associated with (8) is plotted in Fig. 7, comparing it to the results we already had in Fig. 2. The main effect of the RRL is the notch introduced at $f_{\mathrm{chop}} = f_s/2$. The width of the notch can be controlled with α, where larger α values broaden the notch bandwidth. The value of α chosen for the plot is such that $\alpha G_{\mathrm{RRL}}/G_{\mathrm{FB}} = 0.1$. This is a particularly attractive one, since the RRL helps to compensate some in-band drop off of the basic ILSA architecture, creating a system with a very flat passband and a bandwidth of $0.45 \times f_s$. Note that the notches of the RRL do not improve the anti-aliasing behavior, unlike the notches from the ILSA (cfr. Section II).

The above described discrete-time RRL concept was tested in the developed prototype based on a switched-capacitor

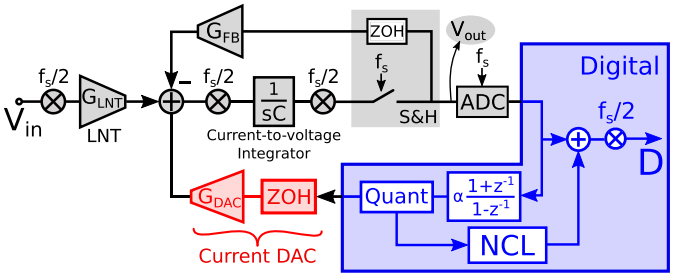

Fig. 8. Mostly-digital RRL with digital bilinear integrator and quantization noise cancellation logic to compensate for the limited DAC resolution.

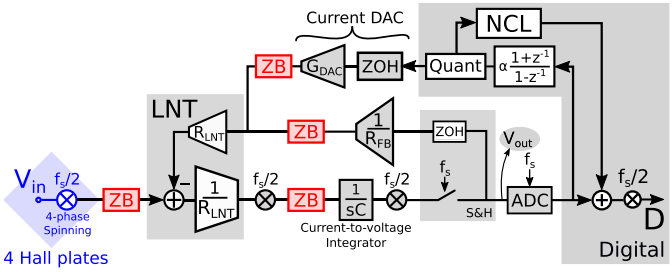

Fig. 9. System-level overview of the Hall sensor system with 'in-the-loop' operation of the LNT and with indication of the zero-banding.

bilinear integrator and was found to behave as expected. Page limit restrictions prevent us from reporting the results with this analog RRL here. Instead, present paper focuses on a mostly-digital RRL implementation, providing a competitive alternative.

B. RRL With Low-Resolution DAC and Noise-Cancellation

As explained before, the analog RRL of the previous section uses the samples taken by the S&H. Because the ADC converts these samples one-to-one to the digital domain, it is a small step to migrate some of the functionality to the digital domain. The resulting mostly-digital RRL is detailed in Fig. 8. The bilinear integrator (7) which required a switched-capacitor circuit in the analog implementation can now be directly implemented in the digital domain. The output of this digital bilinear integrator is then translated into an analog offset compensation signal by means of a current DAC. Such mostly-digital RRLs (based on ADC and a DAC) have been demonstrated before. For instance, [4, cfr.Fig.8] tested a RRL with 16-bit off-chip ADC and DAC, with digital accumulators (i.e. normal integrators) implemented in a CPLD. In spite of the high resolution, the offset compensation was reported to be noisy because the ADC under-samples the IA's wide-band noise. This necessitated the use of slower RRLs which have longer startup times and realize only narrow-band notches. In contrast, the anti-aliasing provided by the ILSA is an enabler for faster RRLs (larger α) exhibiting shorter start-up times and broader notches. Because in our case the ADC is already present on-chip, the only extra cost for fully implementing the mostly-digital RRL is to add an on-chip DAC. For the on-chip DAC we preferred an easily attainable 8-bit resolution. In contrast, the ADC output is 14-bit, and the digital bilinear integrator provides a 16-bit output. Therefore, after the bilinear integrator, 8 bits are truncated to obtain the 8-bit word to drive the current-mode DAC. The limited DAC resolution (steps of 16.5 mV at the output) implies that the large associated truncation error (or *quantization noise*) propagates through the system. However, because the truncated bits are known in the digital domain, this information can be used to cancel this residual ripple at output D. For this, a digital noise-cancellation logic (NCL) block is added which uses the 8 truncated bits to correct the negative effects of the truncation, as shown in Fig. 8. This configuration is similar to what is commonly used in MASH ADCs [35]. The transfer function implemented in the NCL is:

$$H_{\mathrm{NCL}} = \frac{z^{-4} A_{\mathrm{DC}}}{1 + z^{-1} H_{\mathrm{RRL}}(z)} \tag{9}$$

IV. Implementation Details

A system-level representation of the complete Hall sensor system as implemented is shown in Fig. 9. We go over some aspects which have not been discussed yet.

A. Hall Plate Spinning and Zero-Banding

In the prototype, four HPs are hard-wired in parallel, mostly to lower the noise. Each HP is biased in a different direction to cancel out asymmetries, decreasing the overall Hall sensor offset [28]. Current spinning is then applied to this combination, where each spin phase has a duration of $1/f_s = 1\,\mu$s. Our prototype supports both 2-phase and 4-phase spinning. It is known that the offset in each spin phase is almost equal in magnitude but still has some slight variations [4], [36]. Therefore, with 4-phase spinning, a secondary offset tone at $f_{\mathrm{chop}}/2$ will emerge. With 2-phase spinning, the secondary $f_{\mathrm{chop}}/2$ offset tone is at DC, causing a higher residual DC offset. We prefer to have the lowest possible residual DC offset, and therefore will limit ourselves to reporting only results with 4-phase spinning. Note that in most position sensing applications the bandwidth can be substantially reduced by digital filtering of the sensor output. For instance, commercially available Hall-based angle sensing products have bandwidths which are at least 10× lower than the present prototype [37, Table II]. The digital filter can then be used to remove the $f_{\mathrm{chop}}/2$ offset tone as well.

Spinning of the Hall plates inevitably causes large and poorly controlled transients on the Hall signal V_{in}. This is because during spinning the bias nodes, having a voltage difference between them on the order of 2 V, are swapped with the readout nodes, having a voltage difference in the mV-range (the HP readout voltage). Because each node of the HP has some capacitance to ground, there is charge at the bias nodes that needs to be removed before these can take the function of readout nodes. Zero-banding (ZB) disconnects the ILSA from the Hall plates and short-circuits the ILSA input signal while these spin transients are occurring. The timing is detailed in Fig. 10.

The chopping clock $\mathrm{CLK}_{\mathrm{chop}}$ operates at half the rate of the sample clock $\mathrm{CLK}_{\mathrm{s}}$ ($f_{\mathrm{chop}} = f_s/2$), and the signal $\mathrm{CLK}_{\mathrm{ZB}}$

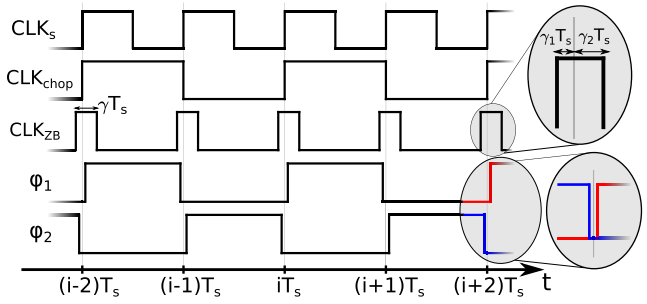

Fig. 10. Clocks in the system. CLK$_S$ is the sample clock, CLK$_{chop}$ is the chopping clock, CLK$_{ZB}$ controls the zero-banding blocks and φ_1 and φ_2 represent the complementary clock signals for the S&H (see Fig. 11).

activating the zero-banding is high during the transitions in CLK$_{chop}$. The zero-banding is initiated $\gamma_1\ T_s$ before an edge in CLK$_{chop}$, and ends $\gamma_2\ T_s$ after the edge. Therefore $\gamma = \gamma_1 + \gamma_2$ denotes the fraction of T_s during which zero-banding is applied. By blocking the large Hall plate spinning transients, the trade-off between a large spin frequency and a low residual offset [8], [38] is somewhat relaxed. Similar techniques were called 'dead band' in [7] or 'gating' in [9].

In order to preserve as much as possible the state of the circuit during zero-banding of the input signal, the feedback paths and the current going to the integrator are zeroed at the same time. The effects of zero-banding can also be incorporated in the analytical analysis of the system. Because of page limit restrictions, we only summarize the impact of zero banding. First, the expression (1) for the DC gain of the amplifier remains valid. Second, the design equation (3) for putting the nominal pole position at $z = 0$ needs to be adapted by replacing T_s with $(1 - \gamma)T_s$. The same adaptation then also needs to be done in (6). The STF (8) remains valid except for a change of the numerator $1 - z^{-1}$ into the factor $z^{-\gamma_1} - z^{-(1-\gamma_2)}$.

B. Main Circuits of the Hall Sensor System

An overview of some important circuits is shown in Fig. 11. The four parallel HPs are biased by a current of 400 μA/plate. Appropriate switches are added for the spinning. The resulting Hall signal is connected to the LNT, which defines its output current based on a poly-resistor R_{LNT}. The LNT is the main noise-critical circuit and is discussed separately further on. The LNT output current is received by an opamp-based current-to-voltage integrator. The differential integrator output then forms the input to the chopped S&H, which uses two pairs of capacitors operating on the non-overlapping complementary clock phases φ_1 and φ_2 (see Fig. 10). When φ_1 is high, the integrator output is being tracked on one pair of capacitors, while the other pair is put in the feedback of the S&H opamp for the hold function. During φ_2, the roles are swapped, as well as the sign of the S&H input, so that chopping is incorporated here as well. A simplified version of the LNT circuit, but using a much larger degeneration resistance (here $R_{FB}/10$, see Fig. 11) is used to generate the feedback current. In order to avoid that this degeneration resistor would become impractically large, a $\div 10$ current mirror is inserted in the current-mode feedback path. This way, for our gain of 1000, the degeneration resistor equals 100 R_{LNT}, while otherwise it would be 1000 R_{LNT}. Note that the source follower, which is the core of this transconductor, is embedded in the feedback loop around the chopped S&H opamp to reduce the effect of its nonlinearity.

An aspect that was not mentioned yet is that all feedback currents, i.e. the current from the feedback transconductance and the offset compensation generated by the current-mode DAC, are collected at the input section of the LNT. This brings the advantage that the LNT operates "in the loop": even when the ILSA receives a full-scale input signal, at sufficiently low input frequencies the LNT operates in a zero-state, since the feedback current will (nearly entirely) cancel the current due to the input signal. This way, the LNT nonlinearity is suppressed.

The output V_{out} is digitized by a Nyquist-rate extended-counting ADC [39]–[42] to a 14-bit word. The ADC is the exact same design as in [42] and so details on its operation and measurement results can be consulted there. The ADC is clocked at $10 \times f_s$ (10 MHz), performs $N = 5$ counting steps and 10 cyclic conversions in order to produce a sample every $1/f_s = 1\ \mu$s. Note that any other type of Nyquist ADC could have been used here provided that it operates fully synchronized with the spinning and sampling of the S&H, as is required for the ILSA concept to work. The ADC output is then combined with the output of the digital Noise Cancellation Logic (NCL) and digitally de-chopped to obtain the digital output signal D. For ease of experimentation, the digital parts of Fig. 8 (the bilinear RRL controller and the NCL) were implemented off-chip in an FPGA.

C. Low-Noise Transconductance

The LNT is the main noise contributor to the ILSA's overall noise performance. As shown in Fig. 11, the LNT is implemented as a so-called 'super source follower' [43] with current folding. The input V_{in} is source-followed towards V_1 over the degeneration resistor ($2R_{\mathrm{LNT}}$). The internal loop in the LNT keeps the bias current through the input transistors constant, improving the linearity compared to a standard source follower. The current through the degeneration resistor is folded to the output, resulting in the output current I_{out}:

$$I_{\mathrm{out}} = \frac{V_1}{2R_{\mathrm{LNT}}} = \frac{V_{\mathrm{in}}}{2R_{\mathrm{LNT}}} \tag{10}$$

As the resistor R_{LNT} forms a direct noise source at the input of the ILSA, its magnitude should be limited. On the other hand, if R_{LNT} is too low, the power consumption of the LNT will increase. The result of this trade-off is $R_{\mathrm{LNT}} = 165\ \Omega$. The noise result for the designed LNT is 4.3 nV/$\sqrt{\mathrm{Hz}}$ input-referred. This puts the LNT input-referred noise just below the noise level of the four parallel Hall plates.

The internal DC loop gain of the LNT is boosted by using cascades, and amounts to 54.6 dB. The input transistors are operated in weak inversion, which maximizes the current efficiency, but results in large input devices. However, this also helps in reducing the overall 1/f corner frequency to 40 kHz, so that the 1/f noise fits in the narrow frequency band near the end of the Nyquist band. In spite of the large input

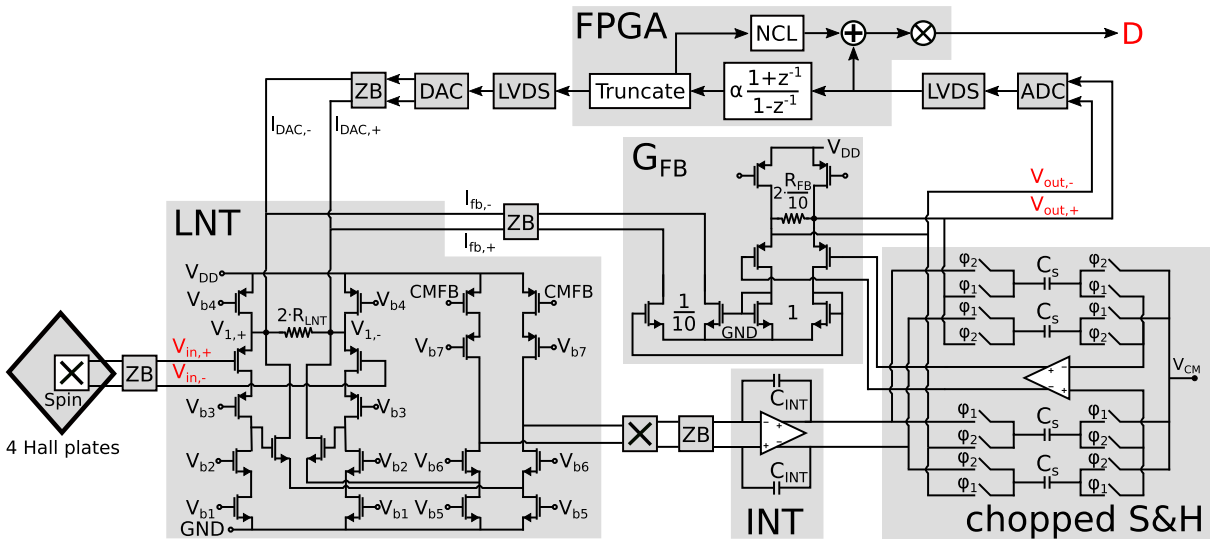

Fig. 11. Circuit level overview.

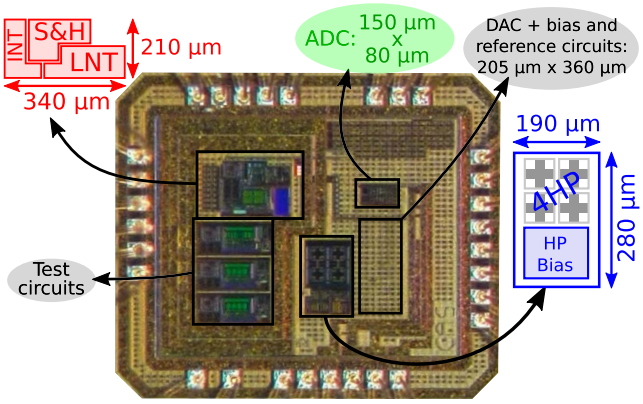

Fig. 12. Chip micrograph (1480 μm $\times$ 1240 μm including pads).

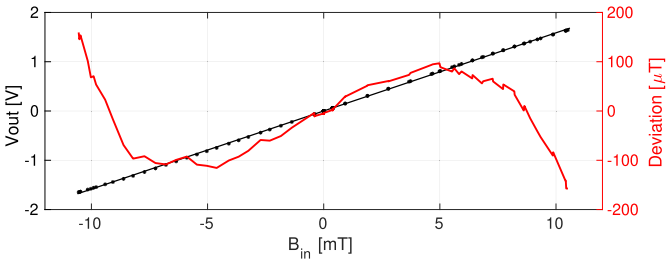

Fig. 13. Measured large signal input/output plot (left axis, black) and the nonlinearity deviation (right axis, red).

transistors, the LNT input capacitance is small because the C_{GS} capacitance is bootstrapped by the super source-follower functionality.

V. Measured Results

The proposed system was fabricated in a 0.18-μm CMOS technology with 3.3 V thick-oxide devices. A micrograph of the chip is shown in Fig. 12. The total size including bond pads is 1480 μm $\times$1240 μm, which is the size of the smallest Europractice Mini-Asic block. The die includes a variety of test structures not relevant for this work. The reported circuits are distributed over the die and occupy a total active area of 0.21 mm^2 (see dimension annotations in Fig. 12). The ILSA-based Hall sensor of Fig. 9 dissipates a total of 5.1 mA at a supply voltage of 3.3 V. Of this, 1.6 mA is for the four Hall plates (400 μA per plate), 0.85 mA for the LNT, 0.25 mA for the integrator, 0.3 mA for the S&H, 0.5 mA is for the ADC and the current DAC consumes less than 0.01 mA. The remaining power is consumed by bias and reference circuits (see Fig. 12). We estimate that the digital circuitry, which are currently in the FPGA, would require less than 0.02 mm^2 area and 0.5 mW of power. All the measurements reported below use the digital output D and are for an ILSA gain of 1000$\times$. The sampling frequency f_s is 1 MHz with a corresponding chopping frequency $f_{chop} = 500$ kHz.

A. DC Measurement

The static input/output plot was measured by applying a magnetic input signal with a Helmholtz coil. It is shown in Fig. 13 (black line). From the plot we obtain the magnetic sensitivity as 158 volt per Tesla. The measured Hall plate sensitivity is therefore 158 mV/T. The full scale input range is $\pm$10.6 mT. The corresponding nonlinearity plot is also shown (red curve) and exhibits a cubic nonlinearity. Over the full scale range, the nonlinearity is less than $\pm$160 μT. Within the restricted range of $\pm$5 mT, the nonlinearity is within the measurement accuracy of around $\pm$15 μT.

B. Anti-Aliasing Behavior

The anti-aliasing functionality of the Hall system is our main innovation and in order to validate it, we needed the ability to generate a reliable high-frequency magnetic field. For this, a spiral inductor is integrated on the test PCB just below the test chip and a current is driven into it to produce a magnetic field. A 1 Ω resistor is put in series to allow easy measurement of the actual current going through the

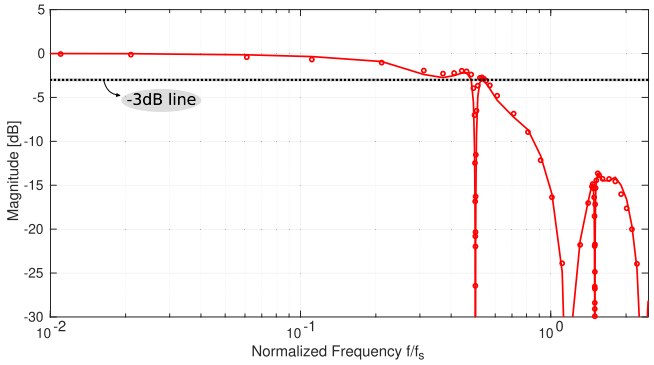

Fig. 14. Measured normalized STF (markers) together with the theoretically expected STF (continuous line).

inductor (which varies as a function of frequency because of its inductance). This configuration allows to generate magnetic signals up to the MHz range, but the maximum magnetic field strength is limited to 780 μT. This is however sufficient to measure the transfer function of the Hall system.

The STF from the magnetic input field to the digital output D can now be determined based on the amplitude of the digital output (taking into account that beyond $f_s/2$, the signal is located at the aliased frequency). The measured STF is plotted in Fig. 14, next to the theoretical prediction, where the plot is normalized with regard to the DC sensitivity. The theoretically expected STF is based on (8), but takes some other factors into account: (i) the zero-banding ($\gamma_1 = 0.05$, $\gamma_2 = 0.1$), (ii) the RRL setting $\alpha G_{\mathrm{DAC}}/G_{\mathrm{FB}} = 0.02$, and (iii) the excess delay in the RRL due to going off-chip to the FPGA and back to the on-chip DAC through serial links. The latter is taken into account by adding a z^{-3} factor to the bilinear integrator transfer (7). An extra complication comes from the fact that the time constant $R_{\mathrm{FB}}C_{\mathrm{INT}}$ of the ILSA loop is not trimmed. Hence, a deviation of up to 30 % can be expected due to process variations. This would blur the comparison between theory and measurements. Hence, this time constant was estimated through curve fitting. The estimated time constant is found to deviate 5 % from its nominal value, which is a statistically plausible value.

The plot confirms that the STF of the system behaves nearly exactly as predicted by the theoretical analysis, proving that the prototype exhibits the desired anti-aliasing functionality. The notches created by the mostly-digital RRL are clearly visible, and also the small peaking caused by the extra delay in the RRL matches the theory. This provides confidence that a design with on-chip integration of the RRL functions would allow to obtain the cleaner characteristic of Fig. 7. The small shift in the anti-aliasing notches is also expected because zero-banding reduces the time-window in which noise averaging occurs. This is something that occurs in all readout circuits that apply zero-banding, and shows that for noise reasons the zero-banding time should remain as low as possible. A bandwidth of around 485 kHz or $0.97 f_{\mathrm{chop}}$ is achieved, pushing the bandwidth to the limit imposed by the Hall plate spinning.

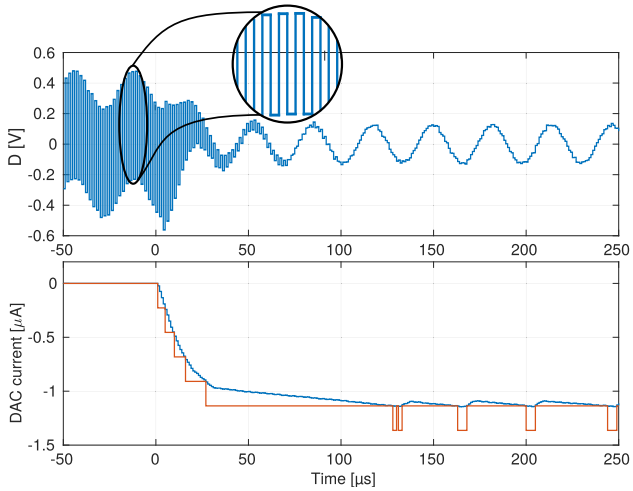

Fig. 15. Time domain plot of the ADC output D (top) and the offset-compensating DAC current (bottom: red = truncated DAC signal, blue = non-truncated DAC signal), when the RRL is activated at time 0. Input magnetic field with amplitude 780 μT and frequency 31 kHz applied.

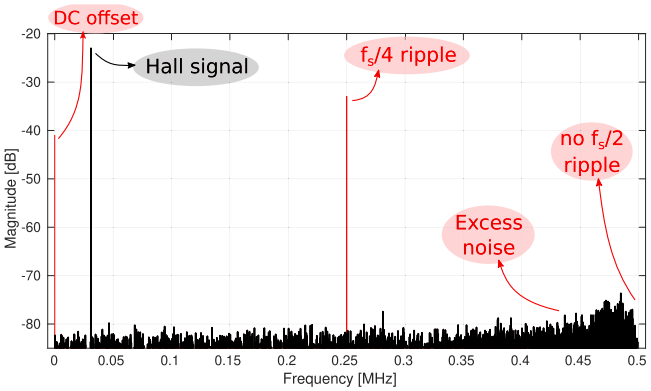

Fig. 16. Measured output spectrum (64K FFT) for a magnetic input at 31 kHz with amplitude 780 μT. The 0 dB reference level corresponds to a full scale signal output amplitude of 1.65 V.

C. Time Domain Measurement

A time domain plot for the ILSA's digital output D and the offset-compensating DAC current is shown in Fig 15, when applying a 31 kHz input magnetic sine wave with 780 μT amplitude. In order to quantify the start-up behavior of the mostly-digital RRL, the RRL is not activated before time '0' and the DAC current is kept zero. A large offset-related ripple of magnitude 370 mV is visible in the ADC output D. As the RRL is activated at time '0', the DAC output current shows a 10-90%-rise time of only 45 μs, while the offset ripple disappears completely in the ADC output. This is a major improvement over prior digital-like RRL implementations such as in [4], [7], which exhibit settling times over 100 ms, up to 6 s. The fastest RRL response time we found in literature was 0.8 ms in [11], which is still 18× higher than our results. This further supports the use of a bilinear integrator in the RRL so that a fast RRL can be designed without any effect on the system's DC gain.

D. Spectral Analysis

A typical measured output spectrum of the digital output D (Fig. 8) is shown in Fig. 16. Again a 31 kHz magnetic field

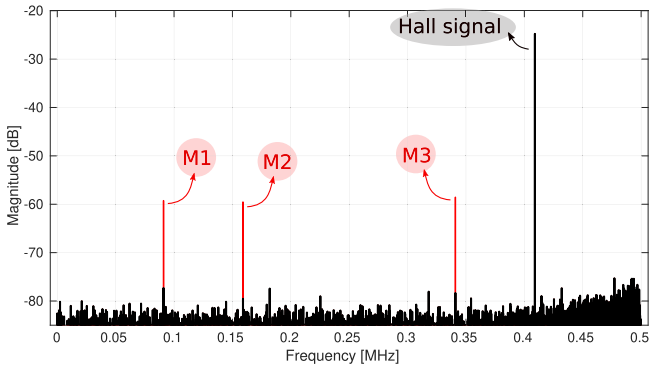

Fig. 17. Normalized output spectrum measurement (64K FFT) for a magnetic input tone at 409 kHz with amplitude 780 μT. The DC offset and offset ripple tone are removed through standard calibration techniques. Red plot: the spectrum before compensation of the magnetically induced tones M1, M2 and M3. Black plot (superimposed over the red plot): the spectrum of the calibrated output signal.

with a 780 μT amplitude is applied. The resulting output signal has an amplitude of 123.8 mV ($= -23$ dB of the full scale of ± 1.65 V). For this chip, the residual DC offset component is 11 mV (input-referred 70 μT). An important observation is that thanks to the digital RRL (which has an ideal offset-less integrator) there is no residual ripple at $f_s/2$. But there is an offset tone present at $f_s/4$, as a result of 4-phase spinning of the Hall plates. Its magnitude of 50 mV is not high enough to significantly influence the dynamic range. Hence, this small $f_s/4$ offset ripple can be removed in post-processing using standard calibration techniques similar as for a normal DC offset, or by digital filtering in case bandwidth can be traded for resolution (including a classical approach with averaging over the four spinning phases). Furthermore, as expected, a small increase of the noise around 450 kHz can be observed. This phenomenon is in part due to some residual high frequency noise aliasing and in part due to some residual 1/f noise.

Fig. 17 shows the output spectrum for a sinusoidal magnetic input signal of amplitude 780 μT at a much higher frequency of 409 kHz, where both offset components are removed through calibration. Next to the expected information signal, three additional spurious tones (labeled M1, M2 and M3) have appeared. Upon investigation, it turns out that these signals are caused by an (undesired) inductive magnetic coupling mechanism into wire loops formed by the interconnection of the Hall plates and the spinning-current switches. This potential problem was already suggested in [15] but was not explicitly taken into account up-front. Upon inspection of the layout around the Hall plates, several wire loops could be identified. Such loops can be expected whenever routing signals around the Hall plate, which as a rule of thumb is done in most cases. A typical shape of such a loop for a single Hall plate is shown in Fig. 18. According to Faraday's law, such a wire loop will lead to a magnetically induced voltage and hence the readout voltage will be:

$$V_{\text{readout}}(t) = V_{\text{HP}}(t) + \underbrace{\frac{d}{dt}\left[A_L(t) \cdot B_{\text{in}}(t)\right]}_{V_{\text{spur}}} \qquad (11)$$

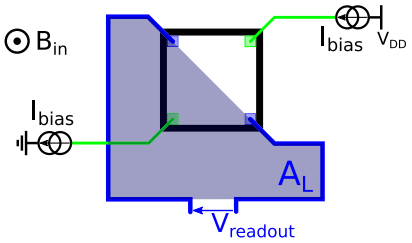

Fig. 18. Hall plate with a wire loop indicated. B_{in} is the input magnetic field, V_{readout} is the input voltage for the readout circuitry, A_L is the wire loop area and I_{bias} is the Hall plate bias current.

where B_{in} is the input magnetic field, V_{HP} is the desired Hall plate voltage and V_{spur} represents the spurious tone due to magnetic induction. A_L denotes the area of the wire loop, as shown in Fig. 18. Because of the spinning-current technique, the connections to the Hall plate differ substantially in every spin phase. $A_L(t)$ therefore corresponds to a time-dependent change of the loop area. For our particular layout, $A_L(t)$ turned out to consist of two square waves, one at $f_s/2$ and one at $f_s/4$. The tones M1, M2 and M3 arise through modulation with these waveforms, in line with what is predicted by (11).

In fact, the spurious tones M1, M2 and M3 can be calibrated based on (11). This can be understood by observing that the magnetic input signal B_{in} can be estimated from the digital output signal D and that the time dependent loop area $A_L(t)$ is fixed and known for a given spinning configuration. Hence, a digital correction signal D_{corr} canceling the contribution of the spurious tones can be constructed to obtain a calibrated output signal $\text{D}_{\text{cal}} = \text{D} - \text{D}_{\text{corr}}$. The result of such a calibration is shown in Fig. 17 as well (black curve superimposed over the red curve). As can be seen from the plot, this nearly eliminates all spurious components. We repeated this experiment for other input frequencies, yielding consistent results in all cases. This confirms that the observed spurious tones are due to the inductive coupling of (11). At this moment, the calibration of the spurious tones is a relatively complex Matlab script, as the STF needs to be taken correctly into account for all spectral components. It is at present not clear if an efficient real time DSP implementation can be made to automatically correct for such errors. Alternatively, it may be possible to avoid the problem by optimizing the layout around the Hall plates. In any case, thanks to the use of an appropriate high-frequency test set-up, new insights into the specific problems of high-frequency Hall readout have emerged.

E. Offset Measurements

To evaluate the offset, 11 samples were measured. Over this sample set, fitting a normal distribution to the overall residual input-referred offset yielded a mean of $\mu = 68\,\mu$T and a standard deviation $\sigma = 77\,\mu$T. These results include Hall plate offset, ILSA offset and residual demodulation of current-spinning transients.

As we can manipulate the Hall plate bias current in our prototype, the offset and offset ripples originating from the

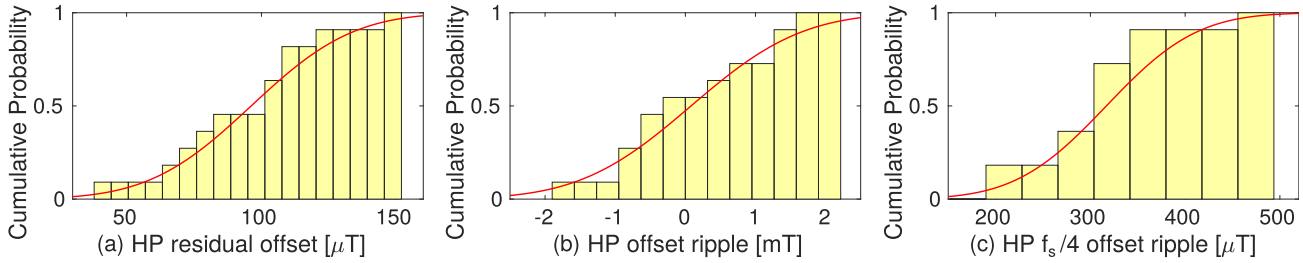

Fig. 19. Cumulative distribution of (a) the input-referred Hall plate residual offset, (b) the input-referred Hall plate offset ripple at $f_s/2$ (RRL de-activated) and (c) the input-referred Hall plate offset ripple ($f_s/4$) at a Hall plate bias current of 400 μA per plate. The red line corresponds to the fitted Gaussian.

Hall plates can be separated from those of the ILSA by sweeping the Hall plate bias current. After performing statistics over the 11 samples, we attain the following results. For the residual input-referred Hall plate offset, we get $\mu = 92.4\ \mu$T and $\sigma = 31.6\ \mu$T. When the RRL is deactivated, the residual input-referred Hall plate offset ripple at $f_s/2$ gives $\mu = 80.1\ \mu$T and $\sigma = 1.25$ mT. Remember that the latter offset ripple is reduced to zero when the RRL is activated (cfr. Section V-D). Because of 4-phase spinning, an additional offset ripple at $f_s/4$ is present that yields $\mu = 317\ \mu$T and $\sigma = 75\ \mu$T. The cumulative distributions for these three Hall plate offset components are plotted in Fig 19. It is important to note here that these reported offset results are for the parallel connection of 4 Hall plates.

F. Noise and Overall System Performance

The total input-referred rms noise was measured as 42 μTrms, including all residual high-frequency noise aliasing. However as mentioned before, noise will alias primarily to $f_s/2$ and not around DC, causing more noise to be concentrated at frequencies higher than 400 kHz (see Figs. 16 and 17). Using additional digital filtering with a bandwidth of 410 kHz, the noise result can be significantly improved to 35 μTrms at the cost of some bandwidth. Important to note here is that this noise result does not change whether the RRL is activated or not, proving that the NCL block in Fig. 9 is efficient in removing the DAC quantization noise. With our maximum input signal of $\pm$10.6 mT, this noise result leads to a dynamic range[2] of 47 dB.

In order to compare the ILSA as a general-purpose read-out amplifier to other architectures, the noise efficiency factor (NEF) [44] is calculated:

$$\text{NEF} = V_{\text{in,rms}}\sqrt{\frac{2I_{\text{tot}}}{\pi \cdot U_T \cdot 4kT \cdot \text{BW}}} = 6.18 \qquad (12)$$

where I_{tot} denotes the current consumption of the ILSA components only, U_T is the thermal voltage and the ILSA's simulated noise power density of 4.3 nV/$\sqrt{\text{Hz}}$ is put for $V_{\text{in,rms}}/\sqrt{\text{BW}}$. As stated in [44], the theoretical limit of a fully differential OTA is NEF = 2.02.

[2]The large-signal measurement was only for DC-signals. But for consistency with established standards [35], we calculate the dynamic range with a theoretically maximum sinusoidal and not with the maximal DC signal.

TABLE I
COMPARISON TABLE

	This work	[6]	[6]	[8]	[20]
	Hall	Hall + Hall	Hall + coil	Hall	Hall
Inp. range [mT]	$\pm$10.6	$\pm$12.5	$\pm$7.8	$\pm$14.8	10
Noise [μT_{rms}]	**35**	272	210	136	-
Noise [$\frac{\text{nT}}{\sqrt{\text{Hz}}}$]	**55**	430	121	136	-
Dyn. range [dB]	47	30	28	38	-
Typ. offset [μT]	68	40	40	>14000	<50
BW [kHz]	410*	400	3000	1000	7.8
Current [mA]	5.1	8	7.7	8.8	0.067
V_{DD} [V]	3.3	5††	5††	1.8	1.8
FOM [dB]	120.5	99.8	106.7	115.7	-
Tot. area [mm^2]	1.84	8.75	8.75	3.96	1.16
Est. AA [mm^2]	0.21	1.48†	>1.48†	0.95†	0.06
Digital output	**yes**	no	no	no	no

* Bandwidth after additional digital filtering (corresponding to the reported noise value). Unfiltered 3dB bandwidth is 485 kHz.
† Estimated from micrograph figures.
†† Estimated from Hall plate resistance and Hall plate bias current.

Table I compares our main results to other Hall sensors. The proposed ILSA achieves the best noise performance compared to the prior art, where it should be noted that our noise results are obtained from a digital output, i.e. including residual aliased noise and quantization noise. Also the dynamic range is significantly improved. Moreover, reasonable offset results are obtained even though we employ an f_{spin} that is 50 times higher than e.g. [6], confirming that the applied zero-banding technique is effective. Our readout circuit approaches the Hall plate bandwidth limits with a bandwidth up to $0.97 f_{\text{chop}}$, with an optimal noise performance obtained for a bandwidth of $0.82 f_{\text{chop}}$ by means of some additional digital filtering. To properly compare noise, bandwidth and power consumption, Schreier's FOM is used:

$$\text{Schreier's FOM} = 10 \cdot \log_{10}\left(\frac{\text{SNR} \cdot \text{BW}}{P_{\text{chip}}}\right) \qquad (13)$$

where BW is bandwidth, P_{chip} is the chip power and SNR is defined as the maximum input sine power with amplitude A in Tesla over the input-referred noise power in Trms:

$$\text{SNR} = \frac{\frac{1}{2}\,(\text{A}\ [T])^2}{(\text{Noise}\ [T_{\text{rms}}])^2}$$

It should again be noted here that our FOM calculation additionally includes residual high-frequency noise aliasing and the power consumption of the ADC.

VI. Conclusion

We have presented a silicon validation of an In-the-Loop Sampling Amplifier (ILSA), as the core analog interface circuit of a Hall sensor front-end. It provides a high one-step gain, low noise, low offset and inherent anti-aliasing. It is found that the concept of a synchronously operated RRL blends well with the core ILSA structure. As an additional feature, this RRL is implemented in the digital domain combined with a low-resolution DAC and corresponding quantization noise cancellation logic. This way, the area overhead of the RRL could be kept low. The resulting Hall readout system is very compact and has a bandwidth close to the chopping frequency with a state-of-the-art noise level of $55\,\mathrm{nT}/\sqrt{\mathrm{Hz}}$ at a low current consumption of 5.1 mA. Moreover this low noise level is maintained over a bandwidth of more than 400 kHz, demonstrating that the ILSA provides a versatile, compact and low-noise solution.

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