Design Methodology for Industrial Internet-of-Things Wireless Systems

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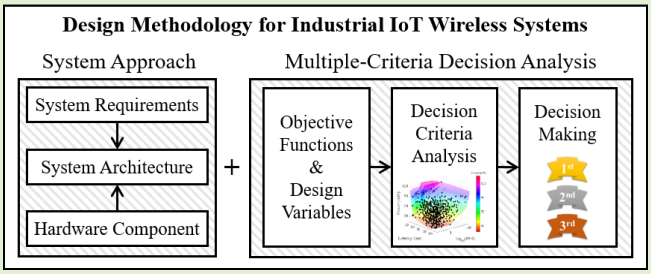
***Abstract*—The ubiquity foreseen by the Internet-of-Things (IoT) and powered by the 5G advancements has motivated research on wireless solutions for critical applications, in particular, Industrial IoT (IIoT). Nevertheless, there is little or no research on a unified design methodology for IIoT that tackles the conflicting wireless system performances of Power, Latency, and Reliability (PLR). Obtaining such a framework is vital for empowering further development and fair comparison in future IIoT designs. Thereby, this paper presents a novel design methodology to tackle PLR trade-off in IIoT Wireless Systems (IIoT-WS). This new methodology uses a meet-in-the-middle system approach to design an entire PLR RF system, and a custom Multiple-Criteria Decision Analysis (MCDA) to help decide the best design variables that are both resource-efficient and PLR-balanced for a given application. Finally, to quantify the methodology for critical wireless systems, a lab-demonstrator for automotive application is designed and its performance compared to other wireless systems standards.**



***Index Terms*—Industrial IoT, WSN, URLCC, IIoT-WS, MCDA, system design, Pareto front, multi-objective optimization, reliable communications, low power, low latency.**

I. Introduction

UNTIL early 2000s, research on wireless systems had been mainly focused on two extremes of Shannon's Law [44]. On one end, the increasing demand for high data-rate under a bandwidth-limited regime has fostered spectrum efficiency and information theory techniques [6], [16], [22]. On the other end, the rise of monitoring applications under a power-limited regime (e.g., Wireless Sensor Networks - WSN) has boosted low-power techniques such as adaptive protocols and power-efficient networks [5], [27], [37]. Even though both ends provided good ground for non-critical users, low-latency and highly reliable applications, such as industrial and automotive, have been left with inflexible, expensive to install and maintain wired solutions.

Recently, the ubiquity foreseen by the Internet-of-Things (IoT) and powered by 5G advances has led to more research on wireless technologies for critical applications. In particular, Industrial IoT (IIoT) [38] has drawn significant attention when applied to industrial process control [51] and monitoring [50], [52], [53], and intelligent automotive systems [12], [13]. Nonetheless, unlike the loose requirements found in traditional IoT applications, such as health-care systems [11] and agricultural monitoring [29], IIoT sets stricter requirements for wireless reliability and low latency with limited power consumption, Fig. 1a. In addition, the conflicting nature of these requirements set an extra level of design challenge for IIoT wireless systems. Also known as a trade-off, the design conflict between Power, Latency, and Reliability means that usually one cannot be made better off without making at least one worse off. In practice, this translates into a concern on how to properly choose the design parameters such that the PLR requirements are met in the best and most efficient way.

The term IIoT Wireless Systems (IIoT-WS) is used in this paper in the broadest context possible and it includes all wireless systems that face, at some extend, the PLR trade-off, such as Industrial WSN (IWSN [28]), Ultra-Reliable Low-Latency Communication (URLLC [45]), and industrial wireless Time-Sensitive Network (TSN [10]). Recent works have addressed this trade-off from many different perspectives. On the system side, new or modified standards have been presented, e.g., IEEE 802.11AH, MTC based on LTE, WirelessHART™, and 6TiSCH [3], [4], [24], [39]. The software side has been approached by creating wireless protocols with multi-antenna base stations, priority access in Wi-Fi MAC layer, constructive flooding, resource allocation, deep learning, or even hybrid architectures [19], [21], [31], [43], [46], [47].

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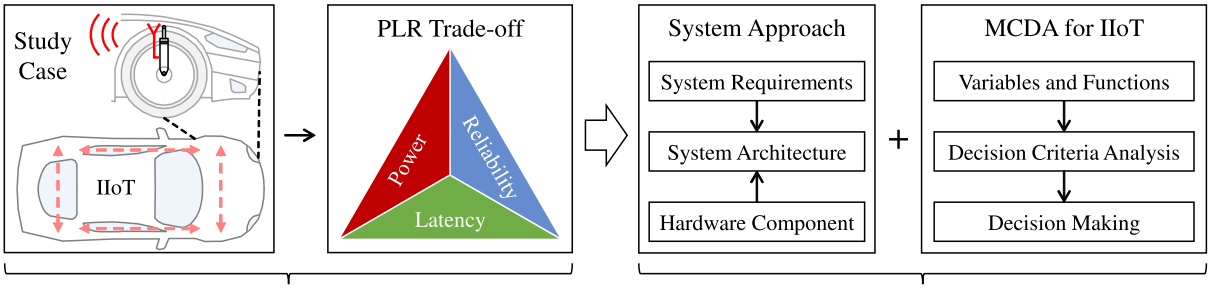


(a) Problem Definition – IIoT Wireless Systems (b) Proposed Solution – Design Methodology

Fig. 1. Design methodology for IIoT wireless systems.

Finally, on a hardware perspective, researchers have addressed IIoT-WS with communication models, packet error models, coding schemes, innovative hardware design, and promising bottom-up design approach [14], [26], [33], [40], [45].

Amid so many design approaches, this work differentiates by presenting a novel design methodology that brings together an extensive range of design layers (e.g., system, architecture, software and hardware perspectives) to provide the best application-oriented and resource-efficient PLR trade-off. This design methodology tackles the PLR trade-off in two steps, as depicted in Fig. 1b: (1) a Meet-In-The-Middle (MITM) system approach is first implemented to design the global wireless system, and (2) a Multiple-Criteria Decision Analysis (MCDA) is performed to help choose the appropriate values for the system's design variables. The methodology offers a broad view of the system-to-implementation concept, while leading to a solution that is both the best fit for a given application requirements and the closest to the theoretical optimum boundary. In the end, the methodology is verified with an example based on an automotive application.

This paper has been divided in the following sections. First, a study case is introduced in Section II. Then, Section III explains the System Requirements of an IIoT wireless system, and Section IV describes its the Hardware Components. Afterwards, the wireless System Architecture is described in Section V, and in Section VI the application example is further developed. Next, the MCDA is presented in Section VII, and in Section VIII the measurements results are discussed.

II. Study Case

At a high level of abstraction, consider a suspension system of an ordinary vehicle. In simple terms, this system limits the vertical motion of the vehicle by damping its vertical velocity [9]. The passive suspension can only have either a soft or stiff characteristic, which brings a compromise between driving comfort or handling capability. To minimize such compromise the passive suspension can be replaced by an easy-to-install Autonomous Semi-Active Suspension system (ASAS) [12], [13]. The ASAS is envisioned to be a self-contained suspension system formed by a network of nodes that harvest energy from the environment and use it to decide, communicate, and deliver the best damping ratio according to the road profile, Fig. 1a. Therefore, the ASAS needs to not only cope with the strict design challenges of any automotive system, i.e., to be reliable and to respond fast, but it also has deal with a limited energy source.

The strict ASAS requirements have a strong impact on the design of its wireless communication system (prerequisite for a plug-and-play capability). For instance, the reliability requirement translates into low Bit-Error-Rate (BER); the fast response translates into low latency communication, and the limited available energy into power-constrained circuits. These are conflicting requirements (a.k.a. the PLR trade-off) and cannot be simultaneously met, which makes the design of the wireless system non-trivial. In fact, this trade-off may be found in many other similar industrial wireless applications and high performance WSN.

Having defined the problem from the study case, the next sections will focus on presenting a solution for the PLR trade-off encountered in IIoT-WS, Fig. 1. The methodology presented in this paper is generic and can be used in a variety of applications, however the described study case will be used through out the text as an application example.

III. System Requirements

In this section we introduce the PLR system requirements from the perspective of time, amplitude and the combined time & amplitude domains.

A. Time

The impact of time (or frequency) related requirements in a PLR system link can be quantified as follows.

1) Coherence Bandwidth (Delay Spread): The majority of wireless links present a non-line-of-sight environment, where the transmitted signal only achieves the receiver via multipath, e.g., cellphone communication in a dense urban environment. Even for point-to-point wireless communication, e.g., satellite links, the receiver still gets multiple times the same signal due to atmospheric effects. Either way, the presence of multipath generates a time dispersion in the received signal that might lead to Inter-Symbol-Interference (ISI). This delay spread (T_m) is a statistical measure of the delay between the first and the last multipath signal components [23]. According to [34] the delay spread is related to the Coherence Bandwidth (B_C), a measurement of the frequency channel flatness, given by Eq. 1. This relationship shows that an ISI-free system may be equivalently achieved by either having a signal bandwidth (B_S)

lower than B_C, or a symbol duration longer than the delay spread.

$$B_C = 1/T_m \tag{1}$$

In IIoT-WS design, these two parameters are used to characterize the fading profile of a channel, and consequently define the minimum uncorrelated channel spacing and the channel allocation of a wireless link.

(i) Minimum Uncorrelated Channel Spacing
In practice, B_C can be found by transmitting a pair of sinusoids over a given channel and cross-correlating the resulting transfer function for different values of frequency separation, Δf. The value in which the cross-correlation function falls below 0.7 is then the coherence bandwidth of a given channel [25]. This value limits the maximum bandwidth of a channel and dictates the frequency channel separation.

(ii) Channel Allocation
Usually, the system's bandwidth accommodates many individual signal channels. For instance, the ZigBee protocol allocates sixteen channels within the 2.4 GHz ISM band. It practically means that the system can use a signal quality measurement tool, such as the RSSI, to identify and avoid a deep fade channel. Thus, improving the chances of successful communication. Alternatively, adaptive frequency-hopping schemes allow systems to continuously hop between healthy channels in order to dynamically avoid interferences or selective fading.

2) Coherence Time (Doppler Spread): The Doppler effect is a frequency shift seen due to a non-zero relative velocity of two bodies. It is commonly relevant for fast-moving targets, like in satellite applications, and may not have a significant impact in daily-life applications, even if we consider strict IIoT-WS. For example, using Eq. 2, a signal transmitted from a car traveling at a relative speed of 120 km/h ($v = 33\,m/s$) faces a frequency shift (also called Doppler spread - B_d) of only 0.1 ppm. For reference, many current systems work with a crystal oscillator with $\pm$ 40 ppm of frequency shift [20].

$$B_d(ppm) = v/c \times 10^6, \tag{2a}$$

$$B_d(Hz) = v/c \times f_c, \tag{2b}$$

where f_c is the signal's center frequency and c is the speed-of-light.

Nevertheless, for those applications where the Doppler is relevant, e.g., [36], the Doppler spread of a channel can indicate a measure of frequency dispersion. Additionally, Eq. 3 shows the relation between Doppler spread and Coherence Time (T_C), which can be seen as the statistical measurement of the fading correlation over time.

$$T_C = 1/B_d \tag{3}$$

In IIoT-WS design, these parameters are used to characterize duration of fading effects in a channel. Consequently, it can be used to determine the minimum uncorrelated time frame in which the system can have two uncorrelated transmissions.

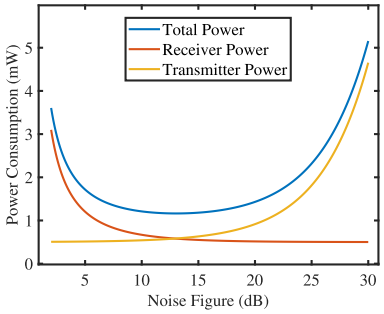


Fig. 2. Example of receiver and transmitter power trade-off based on [17].

(i) Minimum Uncorrelated Time Frame
In practice, if a system retransmits the same data with a time interval $T_{TX} > T_C$, then the more the system retransmits, the better are the chances of successful communication in a given channel. Therefore, one could define T_C as the minimum uncorrelated time frame in which the uncorrelated consecutive transmissions shall happen in order to improve system's reliability. The interval T_{TX} is often translated into an auto-retry delay parameter, and the number of retransmissions into a auto-retry counter, both found in auto-retry functions.

3) Data Rate: The rate (R) at which the data is sent throughout the channel is of paramount importance for wireless system design. Its analysis and choice are not always straightforward.

For instance, contrary to what one might think, a smaller data rate does not necessarily lead to lower power consumption. This only occurs for a 100% duty-cycled radio systems. Otherwise, there is an optimum combination of R and duty-cycle (DC) that provides the minimum receiver's power consumption [18]. Likewise, for a given R in a DC transceiver, the overall power consumption is impacted differently by the receiver (RX) and the transmitter (TX). For instance, while a large R can lead to shorter transmission time, it also requires the receiver to couple with a larger in-band noise because of the higher bandwidth, meaning higher power consumption for the transmitter to ensure an increased SNR at the receiver. Similarly, others approach this issue from a Noise Figure (NF) perspective [17], thus providing an optimum NF that minimizes power consumption in a transceiver, such as depicted in Fig. 2.

B. Amplitude

The impact of amplitude requirements in a IIoT-WS link can be quantified as follows.

1) Path Loss: Path loss measures how much of a signal, at a given frequency, is attenuated when traveling through a certain channel. The free-space path loss (FSPL) can be found by

$$FSPL = (\lambda/4\pi d)^2, \tag{4}$$

where λ is the wavelength and d is the distance between transmitter and receiver.

However, this is oversimplified and does not represent the reality of most wireless applications. Instead, statistical tools

can be used to help model Multipath Rich Environments (MRE). In a static environment, such as indoor, on-field measurements lead to curve fitted log-distance models that accurately represent the situation [54]. Conversely, in dynamic environments, like intra-vehicular WSN, extensive on-field measurements should be used to derive a worst-case PL (PL_W) [12], [13], [32]. As shown in Eq. 5, the PL_W is formed by an average PL (PL_A) added to a level of uncertainty (α), e.g., 2σ for 95.4% confidence. Obviously, it may be a system over-design for non-critical applications, but essential for critical ones.

$$PL_W = PL_A + \alpha \times \sigma. \tag{5}$$

2) Sensitivity: The sensitivity is the minimum received level, for a fixed noise floor, at which the receiver can properly demodulate an incoming signal. This is strictly related to the minimum Signal-to-Noise Ratio (SNR) a receiver must have to achieve a maximum number of bit errors per time, defined as Bit-Error-Rate (BER). The relationship between SNR and BER is further discussed in the next subsection. Once the SNR of a receiver has been defined, the sensitivity (P_{IN}) can be used to estimate the minimum required transmitted power (P_{OUT}) so that the signal can at least overcome the path loss discussed earlier:

$$P_{OUT} = P_{IN} + PL. \tag{6}$$

C. Time & Amplitude

Shannon's law defines the upper bound of information transfer capacity (C) in a white-Gaussian noisy channel for a given SNR (Eq. 7a). This practically means that no combination of time (i.e., frequency) and amplitude parameters allow a wireless system to achieve that upper limit, provided a flat fading channel and a signal with no Doppler effect.

$$C = BW \times log_2 (S/N + 1), \tag{7a}$$

$$N = BW \cdot N_0, \tag{7b}$$

where S is the signal power (W) and N_0 is noise spectral density (W/Hz).

Interestingly, an indefinite increase in the signal bandwidth does not provide unlimited improvement of C. However, next subsections will show that this number can be improved by using different techniques to improve signal-to-noise ratio at the cost of introducing a power, latency, and reliability trade-off.

1) Power, Latency and Reliability Trade-Off: At the cost of power consumption and latency, Error-Correction Codes (ECC) can improve SNR such that the channel capacity approaches Shannon's bound, e.g., Turbo Code [8]. This introduces a fundamental performance trade-off between power, latency, and reliability (PLR) in wireless systems [41]. There must always be one or more parameters to be sacrificed so that a third can improve. Nevertheless, we must highlight the fact that ECC solutions only work on the digital domain. Thus, ECC relies on the fact that Analog-to-Digital Converters (ADC) work under all conditions, e.g., powerful interferences, frequency shifts, etc. Thereby, in order to tackle the PLR trade-off within the rise of IIoT, the methodology presented in this paper aims at combining hardware and software parameter evaluation with multi-dimensional transceivers (e.g., time, frequency, space and polarization diversity schemes). Multi-dimensionality allows for uncorrelated channels, thus providing multiple alternative paths for the signal to successfully arrive at its destination.

TABLE I
MODULATION SCHEMES AVAILABLE IN THE MOST COMMON TRANSCEIVER MODULES

Module	Modulation
ZigBee	BPSK or OQPSK
Bluetooth	GFSK, π/4-DQPSK or 8-DPSK
Wi-Fi	BPSK, QPSK or 16/64-QAM
WirelessHART®	OQPSK

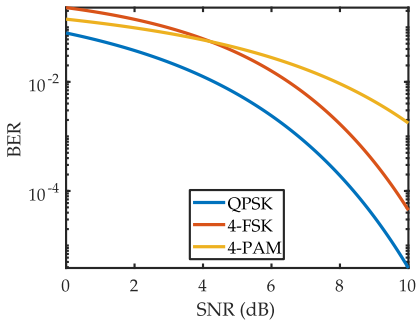


Fig. 3. Theoretical BER versus normalized SNR for different modulation schemes.

It is worth noticing that diversity scheme is fundamentally different from channel access methods. The latter mainly focuses on sharing the channel capacity among different users, while the former aims at improving reliability by use of redundancy.

2) Bit-Error-Rate and Modulation Schemes: Many different factors can dictate the signal modulation choices. It can be limited by regulation requirements (e.g., spectrum emission mask), by channel limitations (e.g., amount of PL, or presence of multipath), or by system reliability requirement (BER). Although not ideal, industrial IoT may want to continue using ISM bands for compatibility and spectrum price issues, which automatically limit the options for modulation schemes. That said, there are basically two ways to choose the proper modulation schemes, and it depends on the system integration level (to be further discussed in Section IV).

(i) When the system is designed from scratch in a fully integrated solution, it is possible to pick a modulation scheme that best fits the channel characteristics and the BER requirement. For instance, Fig. 3 shows the BER vs. SNR performance of some of the most common modulation schemes. One may think, however, that QPSK is the best among the displayed options, but implementation complexity should also be taken into account.

(ii) The second and most common way to decide upon the modulation scheme of a communication system is by

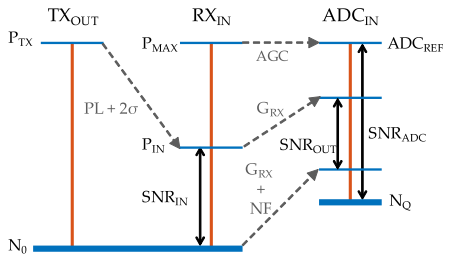


Fig. 4. Complete signal path summary from transmission to reception.

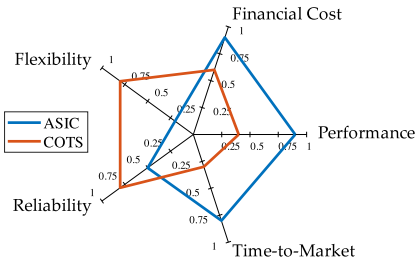


Fig. 5. Qualitative comparison between ASIC and COTS. In average the COTS is better, but may not provide the necessary performance required by some applications.

choosing the adequate wireless transceiver module, often embedded in commercial IoTs. Table I gathers the most commonly used transceiver modules and their respective modulation schemes, frequently dictated by proprietary or standardized protocols.

D. Complete Signal Path

The signal has a long way from transmission until reception and proper demodulation. Fig. 4 summarizes the most important steps seen until now. The signal that comes out of the transmitter (TX) is attenuated by the channel until it reaches the receiver (RX) with a certain input power (P_{IN}). The ratio between the P_{IN} and the white thermal noise is defined by SNR_{IN}, as shown in Eq. 8a. Next, the signal is conditioned by RX such that a particular SNR, for a given BER, is achieved at the ADC's input (SNR_{OUT}), Eq. 8b. The noise floor at the ADC is usually dominated by its quantization noise (N_Q). Finally, the expected receiver's Noise Figure (NF) and Gain (G_{RX}) can be extracted from the required system performance, as expressed in Eq. 8c.

$$SNR_{IN} = P_{IN} - 10\log_{10}\left(\frac{KTB}{1\,mW}\right), \tag{8a}$$

$$SNR_{OUT} = 10\log_{10}\left(\frac{E_b}{N_0}\right) + 10\log_{10}\left(\frac{R}{B}\right), \tag{8b}$$

$$NF = SNR_{IN} - SNR_{OUT}. \tag{8c}$$

IV. Hardware Component

There are many levels of integration. Systems may be designed from scratch extending from protocol to an integrated transceiver and microcontroller solution, they may be implemented over existing platforms, e.g., ZigBee, or yet with a combination of both. This section focus on which are the options available to implement a IIoT-WS system.

Based on the system requirements explained in the previous section, a wireless system can be implemented by either an Application-Specific Integrated Circuit (ASIC) or by a Commercial Off-The-Shelf module (COTS). Fig. 5 evaluates the drawbacks and advantages of each approach qualitatively. On the one hand, high performance, low power and monolithic solutions with total control over design parameters can be fulfilled by ASICs. On the other hand, COTS are cheaper, present a faster time-to-market, are more reliable, but deliver less performance and control.

As a result, an ASIC solution would bring the best possible performance with limited re-use flexibility, at the cost of time and financial resources. In contrast, most of the available COTS shown in Table I are more generic platforms that focus on range and low power performance with a wide degree of re-use. Therefore, the present work chooses to focus on the development of a generic and comprehensive design methodology that delivers the best COTS configuration for the widest variety of IIoT-WS.

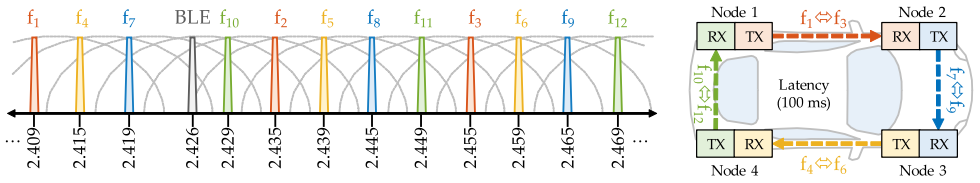
V. System Architecture

Now we meet in the middle from system to implementation to describe the system architecture. Here we discuss the roles of the three lowest tiers of the OSI model, i.e., physical, data link, and network layers [48], while highlighting the importance of diversity schemes for PLR applications.

A. Physical

The Physical layer's (PHY) primary focus is to transmit and receive bits over a communication medium. It is strictly related to the hardware discussed in Section IV and deals with all the topics presented in Section III. After gathering the bits at a particular data rate, the PHY layer translates them into a physical signal (voltage or current) through line codes, e.g., Non-Return-to-Zero, Manchester, etc. The coded stream may be then multiplexed (in frequency, time, space, etc.) to allow the sharing of the channel's capacity among different users. The multiplexing can be eventually extended into a multiple access method controlled by the Data Link layer. The physical network topology, in which the nodes exchange data, is also defined by the PHY layers. The most common options are point-to-point, bus, ring, mesh, and star, all of which can either be fixed or dynamic.

1) Diversity Scheme: It is worth noticing that the channel sharing methods do not intrinsically improve reliability nor latency; to do so, Diversity Schemes (DS) need to be implemented into the network topology instead. The fundamental idea for using DS to achieve reliable and low latency wireless communication is redundancy, i.e., the signal can be spread across multiple, partially-uncorrelated dimensions, namely, time, frequency, space, polarization, code and type of energy (mechanical or electromagnetic). For instance, DS could be implemented by: (1) transmitting the same signal in different frequencies at the same time (frequency diversity acts against multipath); (2) exchanging the same signal at different time instants (time diversity works against time-variant fading



(a) (b)

Fig. 6. Autonoumous Semi-Active Suspension System: (a) Channel allocation; (b) Frequency diversity, each color represents a TX/RX frequency set; and Space diversity, nodes arrangement improve P2P communication.

effects); (3) directing the signal towards a particular angle in space (space diversity give spatial selective against interference signals); or (4) transmitting complementary parts of the signal at the same time but in different frequencies so to reduce latency.

B. Data Link

The Data Link layer (DAT) handles packaging - and unpackaging - of bits originated from the Physical layer into frames. Additionally, DAT layer includes error detection mechanisms, such as parity check, checksums, Cyclic Redundancy Checks (CRC), and error correction codings, such as Hamming, binary convolution, and Reed-Solomon. In turn, these mechanisms may enable acknowledgment of correctly received package, or auto-retransmissions requests. These mechanisms are all essential to increase reliability in a wireless system, but at the cost of power consumption and latency. At the bottom of this layer, a Medium Access Control (MAC) sublayer is responsible for controlling the Physical layer's access to the channel. This essentially controls the dynamic access of users to the channel by multiplexing them in time, frequency, space, or coding (TDMA, FDMA, SDMA, CDMA). In practice, this layer can also be implemented in a μC; however, most of the current COTS transceivers already integrates a full or partial DAT protocol.

C. Network

The Network layer (NET) is responsible for defining the best route to deliver a package from the sender to its destination. There are, however, different ways to determine the best route. For the Internet, the best route might be the fasts while for WSN, it might be that consumes the least energy from the nodes. Moreover, based on a pre-knowledge of the network topology, the NET layer has to handle congestion by re-routing packages. Due to its primary responsibility, the NET layer usually provides quality of service performance, such as delay, transit time, etc. Practically, this layer is implemented by an algorithm (state-machine like) running in a control unit, e.g., computer, microcontroller (μC), or Digital Signal Processor (DSP).

VI. Application Example

This section brings all the concepts developed previously into perspective by methodically translating them into an application.

TABLE II
nRF24L01+ Transceiver Specifications (Recalculated for $V_{DD} = 3.3V$) [2]. P_{DC} Refers to the DC Power Consumption

Transmitter		Receiver		
P_{OUT} (dBm)	P_{DC} (mW)	R $(kbps)$	P_{IN} (dBm)	P_{DC} (mW)
0	33.9	2000	-82	40.5
-6	27.0	1000	-85	39.3
-12	22.5	250	-94	37.8
-18	21.0	-	-	-

A. Introduction

The previously introduced ASAS system can be applied to a car by installing one node in each wheel, as depicted in Fig. 6(b). Each node is composed by: (1) an actuator to change the damping settings, (2) an energy harvesting block that transforms road excitation into energy for the system, (3) an energy storage unit, (4) an independent electronic control unit (ECU) for autonomous operation, and (5) a wireless communication system to share sensor and system data within the vehicle. The latter will have its aspects of system requirements, hardware, and system architecture developed in this section. Afterwards, in Section VII, a multiple-criteria decision analysis will make use of these developments to help decide the best combination of design variables that delivers the most resource-efficient and PLR-balanced performance.

B. Hardware Choice

As discussed earlier in Section IV, ASIC offers the best performance solution for an IWSN application. However, it is costly, time-consuming, and delivers a rigid platform. Therefore, to meet the PLR requirements for vehicular application, we opt to create and evaluate a re-usable, COTS-based node platform composed by 2 microcontrollers (Atmel® ATmega328P microcontroller [1]) and 2 transceivers (Nordic nRF24L01+ transceiver [2]). The nRF24L01P transceiver (nTRX) presents a simple protocol and many adjustable hardware parameters (both to be discussed further in this Section), thus giving a certain degree of design freedom. Table II summarizes the nRF24L01P transceiver specifications extract from its datasheet.

C. System Requirements

System requirements are application-specific and, thus, require prior knowledge of the channel characteristics.

Consequently, we use the in-between-shock-absorbers channel characterization performed in [12] as the basis for this subsection.

1) Time:

(i) *Coherence Bandwidth:* Based on the measured coherence bandwidth, we define the minimum uncorrelated channel spacing to be larger than 5.25 MHz so to avoid correlated fading among multiple channels. As the aim is to use the ISM 2.4 GHz band for the transmission, channel allocation is design to avoid Wi-Fi center frequency channels and BLE advertising channels (respectively dashed and gray line in Fig. 6(a)). The channel spacing is chosen to be 26 MHz.

(ii) *Coherence Time:* There was no measurement regarding the coherence time, but that can be easily estimated by following the example given in Subsection III-A.2. For instance, consider the average speed seen from the perspective of a radio wave leaving the shock absorber to be N times the car's average speed (120 km/h), where N is the number of spokes in the wheel. If we estimate 4 spokes in a wheel and use Eqs. 2 and 3, we arrive at a minimum uncorrelated time frame of 940 μs.

(iii) *Data Rate:* Since we are not using an ASIC solution, our data rate range is limited by the chosen hardware. Therefore, according to Table II, we can choose between 250, 1000 and 2000 kbps. While, on the one hand, the impact of a higher or lower R on the system's power consumption depends on the duty-cycle, on the other hand, as discussed earlier, it also influences latency and reliability. In fact, because of its importance, the data rate is one of the designed variables used in the next section's method.

2) Amplitude:

(i) *Path Loss:* The dynamic environment of a vehicle produced a worst case path loss of 90 dB. For reference, a signal at 2.4 GHz across 315m in FSPL also faces 90 dB of attenuation (Eq. 4)

(ii) *Sensitivity:* As previously discussed in Subsection III-A.3, the data rate impacts on the amount of noise that enters the receiver, which directly affect its sensitivity. Nonetheless, whether the incoming signal is above or below the RX's sensitivity depends on the path loss and output power. Therefore, we can verify from Table II that the nTRX is able cope with the required PL through different combinations of POUT and R, e.g., an POUT of 0 dBm, a R of 250 kpbs and the PL of 90 lead to a signal that is -90 dBm, or 4 dB large the the minimum sensitivity of -94 dBm. In practice, higher than sensitivity SNR means better Eb/No, which translates to a better BER, or a more reliable communication link.

3) Time & Amplitude: The sensitivity values discussed previously refereed to a hardware BER of 10^{-3}, however, based on internal discussions with a shock absorber company [49], the ASAS would require a system BER of at least 5×10^{-5}. Therefore, on top of the fact that hardware Eb/No ($(Eb/No)_H$) can be improved by increasing the output power of the transmitter, the system Eb/No ($(Eb/No)_S$) can be improved by diversity schemes, e.g., time diversity techniques of automatically retransmit the same signal at a lack of acknowledgment signal. nTRX uses auto-retry count software parameter for retransmitting ARC times $(0-15)$, and auto-retry delay software parameter for waiting ARD $(125-4000\mu s)$ seconds before retransmit. As shown in Eq. 9, in practice, the ARC improves the hardware Eb/No by $10log_{10}(ARC+1)dB$.

$$(Eb/No)_S = (Eb/No)_H \times (ARC+1). \tag{9}$$

The nTRX uses a GFSK modulation scheme. Consequently, the hardware Eb/No for a BER of 10^{-3} can be calculated as 10.94 dB and the system Eb/No for a BER of $5 \times 10^{-}5$ as 12.65 dB. Thus, according to Eq. 9, we can extract that a minimum ARC of 1 would meet the reliability requirement. However, it is worth noticing that the larger the ARC, the longer the system latency. Hence, Eb/No is set as an objective function to be assessed in the next section.

D. System Architecture

As explained throughout this paper, while digital techniques, e.g., ECC, do improve the system reliability, they also introduce a trade-off between power, latency, and reliability. Our proposed solution is to explore orthogonal redundant communication links provided by diversity schemes and implemented in all system architecture levels. Therefore, this subsection focus on explaining the architectural and implementations choices that tackle PLR trade-off in an IWSN. It is worth noting that differently from some works [30], latency is defined here as the entire time duration of a cycle, which includes standby and awake periods.

1) Physical: Internal discussion with a shock absorber company [49] led to an ASAS latency requirement of 100 ms (a.k.a., cycle period T_C), i.e., all the data from the 4 nodes has to be exchanged 10 times per second. To deal with that, the physical network structure, depicted in Fig. 6(b), employs space diversity by adopting 4 independent and parallel point-to-point (P2P) links arranged in a ring format. Thus, the system latency can be relaxed down to 100 ms per node, instead of 25 ms. To improve reliability, frequency diversity is implemented by using different sets of frequency channels for each RX/TX pair. At last, it is important to note that the vehicular environment present intrinsic time diversity due to the vehicle's movement. This topology is implemented in practice by allocating one nTRX and one μC for each RX and TX, so that all the communication control can be processed in independent state machines.

2) Data Link and Network: The nRF2401L+ provides a basic data link protocol. It is able to automatically assembly (and disassembly) data packets with destination address, preamble, and payload info, besides validating the data through CRC [2]. Upon request, it controls all receiver and transmitter parameters, such as R, POUT, ARC, ARD.

The two μCs host independent state machines (one for the RX and one for the TX) responsible for the actual control of the communication network. They handle duty-cycle, frequency hopping scheme and set all the transceiver parameters.

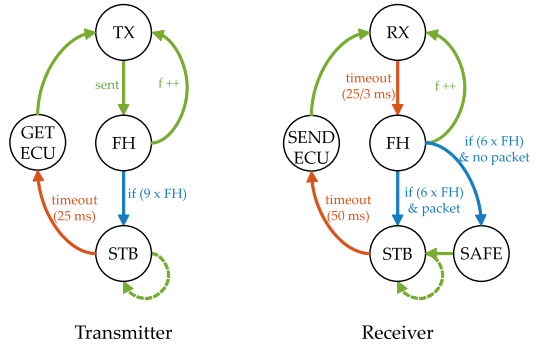


Fig. 7. Two state machines control separately the TX and RX. Green: non-timed transition; Blue: conditioned transition; Red: timed transition. As an example, the duty-cycle is set to 50% DC.

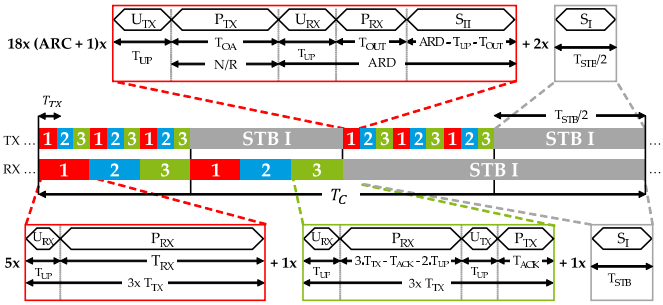


Fig. 8. Non-synced frequency hopping scheme with duty-cycled auto-retransmission arrangement. As an example, the duty-cycle is set to 50% DC.

The state machines presented in Fig. 7 implement a non-synced frequency hopping scheme with duty-cycled auto-retransmission arrangement. This establishes boundaries for latency, while reducing power consumption by duty-cycling and improving reliability by adding frequency and time diversity. As depicted in Fig. 8, the same data is sent 3 times in different channels (pre-defined for an specific TX/RX pair) and each time may be repeated due to auto-retransmission (depending on ARC and ARD), then it is repeated all over again another 2 times. The maximum amount of time the transmitted is on is TX_{ON}, and it has to be more than a quarter cycle ($T_C/4 = 25\ ms$) and less than a half a cycle ($T_C/2 = 50\ ms$) in order to allow for RX and TX overlap. The TX_{ON} period is followed by a stand-by period (TX_{STB}), which defines the duty-cycle as $(1 - TX_{STB})/(T_C/2)$. These two periods are repeated twice every cycle, such that

$$2 \times TX_{ON} + 2 \times TX_{STB} \leq 100\ ms. \tag{10}$$

The receiver is then turned on once every cycle for $2 \times TX_{ON}$ seconds. For each time, the receiver tunes and listens twice the medium at 3 different frequency channel, each time during $TX_{ON}/3$ seconds.

Therefore, the longer the TX and RX are turned on, the higher is the power consumption, the lower is the reliability, and the longer is the latency. The best point for a given application, where all these objectives are met at the same time, depends on the right choice of the data-rate, output power, ARC, ARD, and duty-cycle.

VII. PLR Multiple-Criteria Decision Analysis

With so many different combinations of design variables, each having a different impact on the Objective Functions (OF), properly choosing a unique combination that results in the best fit for the system requirements is not a trivial task. Therefore, in order to cope with that, this section presents the final step of the design methodology for IIoT wireless systems, an implementation of a Multiple-Criteria Decision Analysis (MCDA) based on Pareto optimal front and application-oriented cost-function ranking. The methodology can be used to design any PLR system, in ASIC or COTS, with any system requirements or architecture. Here, to simplify the analysis and understanding, the described ASAS system is used as the target application.

As initially described in Fig. 1, the MCDA methodology is developed in three steps described below.

A. Variables and Functions Definitions

Based on the system requirements, network structure, chosen hardware and discussions with a shock absorber manufacturer [49], the design variables, system goals, and objective functions are first defined.

1) Design Variables:

Any controllable parameter, from hardware or software, can be used as a DV. A full ASIC solution provides more design freedom, and thus more parameters would be available. While COTS have only a limited number of DV values, here called the feasible set. Either way, choosing the best combination of design variables values among all options is not an easy task. Especially if the DVs have a trade-off relation, where one cannot be made better off without making another worse off. Consequently, analytical solutions may become extremely difficult or even impossible for most of the applications; therefore, multi-objective optimization tools should be applied instead. The proposed method based on COTS adopts five design variables, which provides good control over the system performance. They are: (1) auto-retry count (ARC: 0:1:15), (2) auto-retry delay (ARD: 250:250:4000 us), (3) data rate (R: 250, 1000 and 2000 kbps), (4) output power (P_{OUT}: -18, -12, -6 and 0 dBm), and (5) standby time (T_{STB}: 0:1:100 ms), a.k.a. duty-cycle. The maximum and minimum values of these variables also sets the upper and lower boundaries for the optimization tool.

2) System Goals: Additionally to the on-field measurements performed to characterize the damper-to-damper channel in a car environment [12], [13], many discussions with a shock absorber company [49] led to a set of system goals.

(i) *The latency goal* is dominated by the proposed non-synced frequency hopping scheme with duty-cycled auto-retransmission arrangement. The maximum number of retransmission, the delay between them and the stand-by time dictate the worst-case latency. As discussed earlier, the latency should be shorter than 100 ms, with a duty-cycle of at least 50%.

(ii) *The reliability goal* is measured in terms of BER and it should be better than 5×10^{-5}. That is equivalent to a Packet-Error-Rate of 13×10^{-3} (given 32 bytes

of payload). The BER is dictated by the output power, ARC and data-rate.

(iii) *The power consumption goal* is set to be less than 90 mW per node, which is only 1.8% the total available power from the energy harvesting system. For a reference, that is equivalent to a node continuously working for 40 hours with a standalone 3600 mAh battery, which sounds very conservative for a car application. This goal is dictated by all the design variables.

3) Objective Functions:

The system performance is evaluated mathematically by objective functions. They are based on models of how the system works in reality, and they are mostly drawn from the transceiver's datasheet and the theory developed in Section III. Since, the resulting optimum solutions are as good as the models, we try to define these thoroughly.

(i) *Latency*, also called cycle time (T_C), is defined in this paper as the time the transmitter attempts to properly send the data to the receiver. As shown in Fig. 8, T_C is the equal for both RX and TX, although they are implemented differently. In practice, the transmitter profile dictates the latency depending upon the ARC, ARD, R, and T_{STB} while the receiver only changes listening time accordingly. As shown in Eq 11a, the TX profile is formed by ARC times 18 frequency hops and two standby times ($T_{STB}/2$ each). During each TX time, described in Eq. 11b, large values of ARC and ARD can lead to improved link quality due to increased time diversity.

$$T_C = 18 \cdot (ARC + 1) \cdot (T_{TX} + T_{STB}), \quad (11a)$$

$$T_{TX} = T_{UP} + T_{OA} + ARD, \quad (11b)$$

where T_{UP} is the time for startup (130 μs), T_{OA} is the time of data on air (number of bits over data rate - N/R). While in ARD, the transmitter listens for acknowledgment for a timeout period (T_{OUT}) before entering standby mode II.

(ii) *The overall power consumption* depends on the contribution from the power spent and the time elapsed in each transmission and reception event. Thus, the averaged total power consumption, described in Eqs. 12, is calculated by the sum of the events shown in Eqs. 11 multiplied by their respective power consumption (summarized in Table III) over a cycle time.

$$P_T = (E_{TX} + E_{RX})/T_C, \quad (12a)$$

$$E_{TX} = 18 \times (ARC + 1) \times (E_{UTX} + E_{OA} + E_{URX} + E_{OUT} + E_{SII}) + E_{SI}; \quad (12b)$$

$$E_{RX} = 5 \times (E_{URX} + E_{TRX}) + E_{URX} + E_{TRX2} + E_{UTX} + E_{ACK}; \quad (12c)$$

where the energy spent during 130 μs for TX start up is E_{UTX} and for RX start up is E_{URX}; the energy spent for transmission during the time-on-air (E_{OA}) and acknowledgment (E_{ACK}) events is composed of an independent term and an output power dependent term; the energy spent while receiving data during receive mode (E_{TRX} and E_{TRX2}) and timeout event (T_{OUT}) is composed of an independent term and a data-rate dependent term. Those dependent and independent terms were extracted and curve fitted from II into Table III.

TABLE III
POWER CONSUMPTION DERIVED PARAMETERS FOR THE nRF24L01+ TRANSCEIVER ($V_{DD} = 3.3V$). THE TX AND RX POWER CONSUMPTION HAVE INDEPENDENT AND DEPENDENT TERMS, WHICH WERE CURVE FITTED FROM TABLE II

P_{RX}		U_{RX}	P_{TX}		U_{TX}	S_I	S_{II}
(mW)	(nW/bps)	(mW)	(mW)	(W/W)	(mW)	(uW)	(mW)
41.25	1.65	29.37	24.09	13.58	26.4	85.8	1.06

(iii) *The reliability* of a communication system is usually measured in terms of BER, which is a function of E_b/N_o. Therefore, if the Eqs. 8 are rearranged, it is possible to express E_b/N_o in terms of R and P_{OUT}, as shown in Eq. 13.

$$Eb/No = \frac{(P_{OUT} \cdot (ARC + 1)}{R \cdot F \cdot k \cdot T \cdot (10^{PL/10})}. \quad (13)$$

where K is the Boltzmann constant, T is the temperature and PL is the path loss defined earlier.

The more the TX tries to retransmit data, the larger is the chance of the data being properly received. Thus, the ARC parameter can be incorporated into Eq. 13 to account for that. To enable a more accurate modeling of the reality, the noise factor (F) can be extracted from Eq. 8 by using an E_b/N_o for a GFSK system with a BER of 10^{-3} (value considered for the sensitivity given by the nTRX datasheet). Additionally, a new hardware sensitivity for a BER of 5×10^{-5} was also calculated and used as a constraint for the algorithm.

B. Decision Criteria Analysis

In order to help decide the values of the DV that are most suitable for a given application, a criteria analysis has to be performed. It quantifies all the possible solutions with respect to certain criteria: how far the feasible set of DV is from the optimal (usually non-feasible) set; and how the feasible set performs w.r.t an application-oriented cost-function.

1) The Pareto Front:

The Pareto optimality provides the optimal boundary from which conflicting objective functions can not surpass. It delivers the most optimal performance set for a multi-objective system such that one objective cannot be made better off without making another one worse off [15]. Nevertheless, this optimum boundary, called Pareto Front (PF), belongs to $\mathbb{R}$, and thus cannot be directly used for COTS, which present a discrete set of DV values. On the other hand, an ASIC system can potentially make use of any candidate of the PF.

Using the variables, goals and functions defined for the ASAS system in Subsection VII-A, a optimization problem is proposed to minimize both overall power consumption and latency, and to maximum reliability, given the constraints shown in Table IV. The Pareto front obtained from such optimization can be seen in a 3D view, Fig. 10, or in section views,

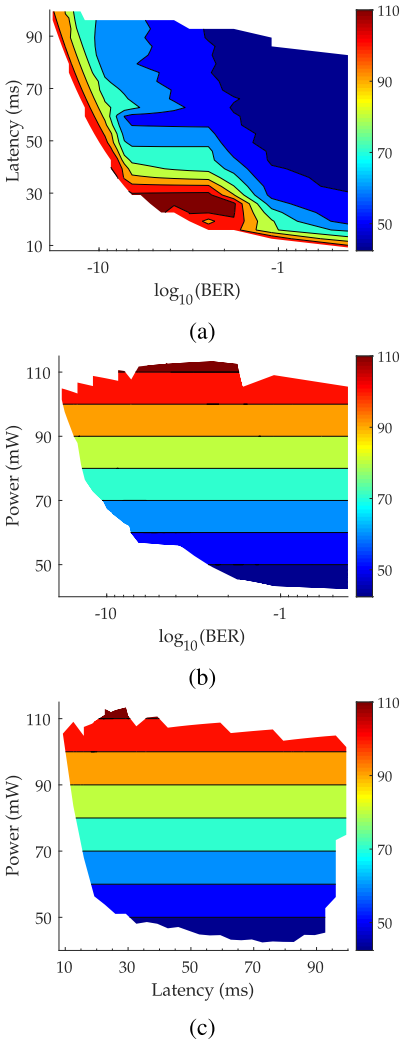


Fig. 9. Pareto front highlights the trade-off between Power, Latency and Reliability: (a) Reliability x Latency; (b) Reliability x Power; (c) Latency x Power. All colorbars present power information. Reduced number of points was used to improve visualization.

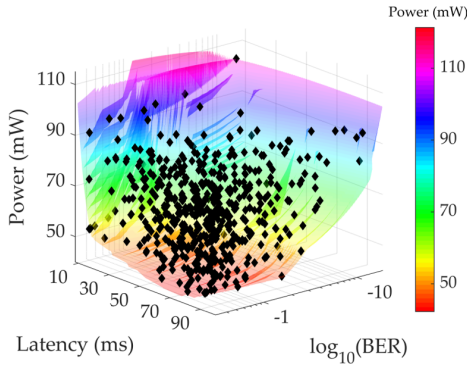


Fig. 10. Pareto front (in colored scale) represents the optimum theoretical boundary for a specific PLR system. The DDS is formed by the black dots, which represent the achievable hardware performance. Reduced number of points was used to improve visualization.

TABLE IV
OPTIMIZATION PROBLEM FORMULATION

Min. $P_T\,(ARC, ARD, R, P_{OUT}, T_{STB})$
Min. $T_C\,(ARC, ARD, R, T_{STB})$
Max. $BER\,(ARC, R, P_{OUT})$
s.t.
$P_T \leq 90\ mW$
$T_C \leq 100\ ms$
$BER \leq 5 \times 10^{-5}$
$0 \leq ARC \leq 15$
$250\ us \leq ARD \leq 4000\ us$
$250\ kbps \leq R \leq 2000\ kbps$
$-18\ dBm \leq P_OUT \leq 0\ dBm$
$0\ ms \leq T_{STB} \leq 100\ ms$

Fig. 9. By inspection, one can recognize the Power x Latency x Reliability trade-off expected for an IIoT. For instance, it is evident from Fig. 9a that low latency and low BER can only or restrictively be achieved at the cost of power consumption, where the power peak shown in dark red presents the overall lowest latency and BER. Similarly, Figs. 9b and 9c show that the link quality and system latency can only be achieved by increasing power consumption. Moreover, it is interesting to note that the latter two cases show a gradient effect over power consumption. In practice, this means that equal values of power can lead to a wide range of BER and Latency.

2) Distance to Optimality and Cost-Function: As discussed earlier, the PF solutions can only be fully met by using a costly ASIC design. Nevertheless, the methodology developed in this paper shows that a good compromise between cost and performance can be achieved even when COTS hardware is used. Thus, in order to decide the best solution within the feasible set of design variables, the following criteria can be applied.

After the PF is obtained, the feasible set can be evaluated into the objective functions and a discrete design space (DDS) created, shown as black dots in Fig. 10. These points represent the discrete feasible performances of the COTS-based system and most of them are clearly far from the optimum boundary of the Pareto front. In order to measure the optimality distance of these DDS points, a vector d_j, shown in Eq. 14a, is created. Each element of this vector contains the minimum distance between the respective DDS point to the PF, thus giving quantitative measure of optimality for the discrete points. This means that small distances will lead to the most resource-efficient solutions (w.r.t. power, latency, and reliability). Finally, in order to evaluate the fitness of each DDS point to the system requirements, a Cost-Function vector (CF_j) can be derived as shown in Eq. 14b.

$$d_j = \left[\min \left(\sqrt{\sum_{i=1}^{Q} \left(DDS_j - PF_i \right)^2} \right) \right]_{j=1}^{P}, \quad (14a)$$

$$CF_j = \left[\frac{abs(log_{10}(BER_j))}{Latency_j \cdot Power_j} \right]_{j=1}^{P}, \quad (14b)$$

where $i \in [1\ Q]$, Q is the number of points that form the PF, $j \in [1\ P]$, and P is the number of points that form the DDS.

TABLE V
THE HIGHEST RANKED DECISION OF THE METHODOLOGY

Latency	Reliability	Power	R	ARC	ARD	P_{OUT}	T_{STB}
(ms)	(BER)	(mW)	(kbps)	(-)	(μs)	(dBm)	(ms)
51	10^{-7}	66	250	0	500	0	21

Latency and Power vectors are normalized by ms and mW, respectively.

C. Decision Making

Making use of the vectors defined in Eqs. 14a and 14b, a decision making vector, called Optimum-Cost-Function (OCF_j), can be created. It divides element-by-element of the CF_j vector sorted in a descending order with the d_j vector sorted in a ascending order. The resulting vector can then be sorted in a descending order and corresponding DV values can be mapped back. Table V shows the best candidate (out of 307200), which scored highest in OCF_j. In practice, this candidate delivers the best application-oriented and resource-efficient solution, i.e., it delivers the best cost-function that is the closest to the optimal boundary.

Additionally, the cost-function presented in Eq. 14b can be modified to emphasize one of the objective function at the expense of another by raising it to a non-unitary exponent. The Weighted-Product-Cost-Function ($WPCF$) is formulated in Eq. 15, where w_1, w_2, and w_3 are the relative weight of importance for reliability, latency, and power, respectively. For instance, a case where the user would like to focus on reliability could apply a $w_1 = 2$, while maintaining $w_2 = w_3 = 1$.

$$CF_j = \left[\frac{abs(log_{10}(BER_j))^{w_1}}{Latency_j^{w_2} \cdot Power_j^{w_3}} \right]_{j=1}^{P}, \tag{15}$$

VIII. METHODOLOGY VERIFICATION

This section verifies the design methodology for critical wireless applications by employing the candidate of Table V into a laboratory demonstrator. The measured and expected performances are then compared to similar industrial wireless systems.

A. Experimental Scenario

Fig. 11 shows the experimental setup. The measurement is performed inside a Faraday cage laboratory, where the radio-frequency spectrum is well under control. The setup is composed of a TX-RX pair sharing data through a 90 dB attenuation medium for approximately 30 minutes. The transmitter is located inside a metal box, and it is powered by a 9 V battery so that it is completely isolated from the receiver, except for the 90 dB attenuation path. The receiver is also placed inside another metal box to ensure isolation. During the standby period of each cycle, the RX forwards the received data to a computer (PC) that validates and compares it to the expected packet. The PC can then calculate the system performance based on when and how many packets are received correctly.

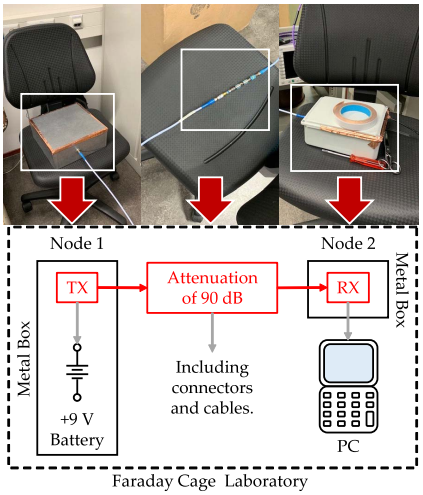


Fig. 11. Measurement setup inside the Farady cage laboratory.

B. Reliability

The system reliability is measured in terms of Packet-Error-Rate (PER), i.e., the number of wrong packets received per the total number of cycles measured. The relation between PER and BER depends on the number of bits (N), and it is described in Eq. 16. The measured PER matches the required one with a value of 13×10^{-3}. Nevertheless, there is a practical difference between the measured and simulated (22×10^{-6}), which is due to the non-ideal and time-constrained measurement setup. For instance, even in an ideal measurement setup, the exact matching between theoretical and measured values would only be achieved at an infinitely long time.

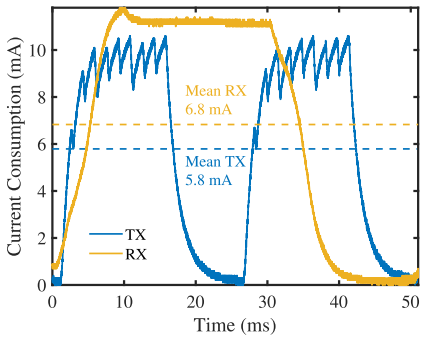
$$PER = 1 - (1 - BER)^N. \tag{16}$$

C. Power Consumption

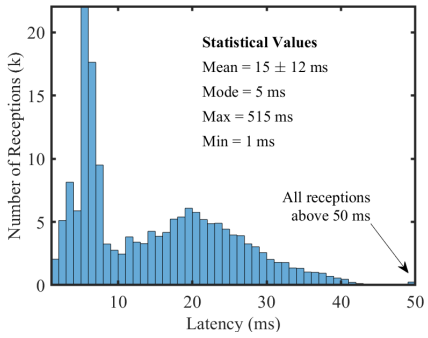
Fig. 12a shows the transmitter and receiver current consumption over time when no data is exchanged, i.e. worst case power consumption. The global mean current consumption is 12.6 mA, i.e., 41.6 mW of mean power consumption. The divergence between measurement and simulation (66 mW) is due to the onboard decoupling capacitors that smooth the rise and fall transitions. Moreover, it is worth noticing that the ASAS results do not have the minimum power consumption possible, but it is the best trade-off between power, latency and reliability. It is obvious that one could achieve a lower power consumption, however latency and reliability would not be nearly as good.

D. Latency

According to the expected values shown in Table V, the cycle latency should be 51 ms, which correspond to about 20 cycles per second. To measure that, a PC monitored the time between received packages. The resulting measurement and its statistical analysis are shown in the histogram of Fig. 12b. It can be seen a maximum delay of 515 ms, and a minimum one of 1 ms. The most frequent delay being only 5 ms, and an average delay of 15 ms with 12 ms of standard



(a)



(b)

Fig. 12. Experimental performance: (a) transmitter and receiver current consumption profile; (b) number of receptions per latency.

deviation. For performance comparison purposes, a confidence interval of two standard deviation (24 ms) is used, which means that 95% of all receptions were within 39 ms.

E. Extrapolation

The performance achieved by the described methodology is the best possible for a given application and a single link, however it can still be further improved. At a cost of size and bandwidth occupation, the same system would only require parallel links (pairs of TX/RX), making use of vacant frequency channels of Fig. 6, to send data concurrently in time, thus reducing the latency by the same factor of added links. For instance, 3 parallel links, sending data split in 3 set of channels, would reduce the latency by a factor of 3, while keeping the BER and power consumption the same. The overhead sync bits, and the added startup time and power from the local oscillators can be neglected since the TX/RX on-time, which is much more power hungry, would not change with the parallelization of data. Therefore, to show the full potential of this methodology, and the use of multi-dimensionality for IIoT-WS, the measured performance can be extrapolated to a 3 parallel link system, as shown in Table VI.

Ultimately, a multi-link system could be optimized to provide a performance superior to the extrapolated one. In fact, it would be even more beneficial and efficient, if the multi-link system was implemented in an instantaneous wideband system, rather than many parallel narrowband ones.

F. Performance Comparison

Consistent practical data that can be used for a comparison with the latest technology is not abundant in literature.

TABLE VI
PERFORMANCE COMPARISON

Technology	Reference	Power (mW)	Latency (ms)	BER ($\lvert \log_{10} \rvert$)	FoM
Simulation	**This Work**	**66**	**51**$^{(I)}$	**7**	**2080**
Measurement		**42**$^{(III)}$	**39**$^{(II)}$	**4.3**	**2651**
Extrapolation		**42**$^{(III)}$	**13**	**4.3**	**7953**
Bluetooth	[7], [42]	100	50	9	1800
WLAN	[28], [42]	500	500	9	36
ZigBee	[35], [42]	50	500	9	360

(I) Worst case value.
(II) Value for 95% of the cases.
(III) Average of the decoupling-capacitor-smoothed power consumption.

Nevertheless, the comparison of the simulated, measured, and extrapolated results of the lab demonstrator is done with technology contemporary to the hardware used ([42] and nRF24L01+ are both from late 2000's). The comparison is shown in Table VI. While the results of this paper performs among the absolute best on power and latency, it delivers the worst BER among all references. That is, however, due to the very own nature of the PLR trade-off that improves one objective at the expense of another. Therefore, to properly and quantitatively compare different system performances, a Figure-of-Merit (FoM) that takes into account the impact of the PLR trade-off should be used, Eq. 17. According to the FoM, the 3 implementations of this work outperform their best counterpart by up to a factor of 4 times. This shows that the PLR design methodology presented in this paper, not only brings valuable design insights, but also delivers a PLR performance that is the best balance in a resource-efficient solution for a given application.

$$FoM = \frac{|\log_{10}(BER)|}{(Power_{(mW)} \cdot Latency_{(ms)})}. \tag{17}$$

IX. CONCLUSION

This paper has presented a detailed and comprehensive design methodology based on multiple-criteria decision analysis for industrial IoT wireless systems. The methodology can be used to help decide which is the best combination of design variables for a given application that delivers the most resource-efficient and PLR-balanced performance. Furthermore, the paper has also highlighted the main aspects of system requirements, hardware, and system architecture that are required for a low power, low latency, and reliable wireless system design. The proposed design methodology was successfully tested and validated through measurements. A lab-demonstrator was built using the PLR methodology and its results have outperformed well-known wireless standards. Future research will include an ASIC implementation fully designed with the presented methodology.

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