Compact Source-Gated Transistor Analog Circuits for Ubiquitous Sensors

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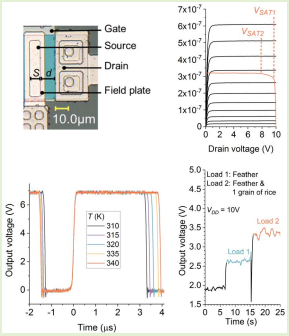
***Abstract*—Silicon-based digital electronics have evolved over decades through an aggressive scaling process following Moore's law with increasingly complex device structures. Simultaneously, large-area electronics have continued to rely on the same field-effect transistor structure with minimal evolution. This limitation has resulted in less than ideal circuit designs, with increased complexity to account for shortcomings in material properties and process control. At present, this situation is holding back the development of novel systems required for printed and flexible electronic applications beyond the Internet of Things. In this work we demonstrate the opportunity offered by the source-gated transistor's unique properties for low-cost, highly functional large-area applications in two extremely compact circuit blocks. Polysilicon common-source amplifiers show 49 dB gain, the highest reported for a two-transistor unipolar circuit. Current mirrors fabricated in polysilicon and InGaZnO have, in addition to excellent current copying performance, the ability to control the temperature dependence (degrees of positive, neutral or negative) of output current solely by choice of relative transistor geometry, giving further flexibility to the design engineer. Application examples are proposed, including local amplification of sensor output for improved signal integrity, as well as temperature-regulated delay stages and timing circuits for homeostatic operation in future wearables. Numerous applications will benefit from these highly competitive compact circuit designs with robust performance, improved energy efficiency and tolerance to geometrical variations: sensor front-ends, temperature sensors, pixel drivers, bias analog blocks and high-gain amplifiers.**



***Index Terms*— Analog electronics, contact barriers, Schottky barrier, source-gated transistors, thin-film transistors.**

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I. Introduction

FLEXIBLE and printed electronics are now maturing from a promising future technology [1]–[5], to be regarded as emerging [6]–[10], with potential areas of use conceived at a rate faster than progress in production-ready applications. Design constraints imposed by the use of conventional thin-film transistor (TFT) structures is holding back many extraordinary opportunities [5], [11], [12]. While there is no limitation on imagining valuable applications, such as electronics on paper, textiles, etc., their realization requires fabrication yield with low-cost, high-throughput manufacturing, which at present is highly challenging [6], [13], [14]. Realizing advanced large area electronics (LAE) requires device architectures that have a high degree of uniformity, reliability and robustness [12], and circuits with a minimal number of components to reduce yield loss due to variability.

Currently, the core element of a vast majority of LAE, is the TFT, which is based on conventional field effect transistor (FET) principles. The net conductivity of its semiconductor channel, including variations in source-drain gap [7], short channel effects, threshold voltage V_{th} variations during manufacturing and under bias stress [15], have an adverse impact

on analog circuit performance and operating frequencies [16]. Recent advancements in device design, aimed at mitigating these limitations [17], [18], may provide a solution only for small circuits, as the necessity for device-by-device tuning drastically reduces its applicability to circuits with more complex functionality. Techniques for reducing the impact of TFT non-idealities include the use of compensation circuits, ranging from rudimentary cascoding or additional gain stages, to feedback, bootstrapping and complex timing and preloading circuits. Other techniques involve the use of combined material systems, which complicate fabrication processes, while still requiring support circuitry [19]. Undesirably, with the increase of circuit complexity, circuit area naturally increases and device variations become more critical, drastically impacting fabrication yield and robustness [7], [20]. A current stop-gap solution involves mounting conventional silicon chips onto flexible substrates (hybrid integration) [13], [21], but this approach is not particularly suited for single-use applications, such as medical or ecological agritech bio-sensors. For high throughput fabrication methods to be economical, thin-film circuits would ideally be highly functional yet compact (comprising few components, which themselves can tolerate stress and variability).

The source-gated transistor (SGT) is a TFT structure with operating mechanisms considerably different from conventional FETs [22]. The SGT has shown remarkable benefits: lower saturation voltages, high gain, low power consumption and, notably, superior uniformity and electrical robustness [23]–[26]. There are, however, drawbacks arising from the reduced current density (due to charge injection over an energy barrier purposely introduced at the source) and increased capacitance (as a result of the staggered source and gate electrodes): relatively low transconductance g_m and operating frequency f_T [27], [28], respectively. However, the energy barrier Φ_B at the source and source-gate overlap are two out of the three requirements for a TFT to operate as an SGT [22], with $\Phi_B = \Phi_M - \chi$, where Φ_M is the metal work function and χ is the semiconductor's electron affinity. The third requirement is that the semiconductor needs to be capable of being fully depleted in the source region when the source barrier is reverse biased by the applied drain potential. Fig. 1a and 1b show cross-sections of two SGTs with source-gate overlap S and source-drain separation, d. (SGTs ordinarily do not use the more general notation L for source-drain gap, as their effective channel length varies with applied bias in a manner additional to channel length shortening in FETs, hence the distinct terminology). SGTs have been explored in a variety of materials including amorphous [29] and polysilicon [23], [25], [28], [30], ZnO [31], InGaZnO (IGZO) [26], [32], organics [33], MoS_2 [34] and semimetals [26], with several means of engineering an energy barrier at the source, including Schottky contacts (Fig. 1a), bulk unipolar contacts [35], [36], or incorporating a tunnel barrier [32] (Fig. 1b). Fig. 1a shows the depletion region that forms in the semiconductor. The drain voltage at which the accumulation layer pinches-off at the source represents the saturation voltage, and is determined by the product of overdrive voltage and series specific capacitance between gate and source in the pinch-off region, $V_{SAT1} = (V_{GS} - V_{th})(C_i/(C_i + C_s)) + K$, where C_i and C_s are the insulator and depleted semiconductor capacitances per unit area, respectively, and K is a constant representing the drain voltage required to deplete the semiconductor [29]. For suitably chosen C_i and C_s, abrupt saturation can be achieved. This saturation behavior is in contrast with conventional TFT operation, in which the accumulation layer pinches off at the drain at a voltage which can be, in the first order, described as $V_{SAT2} = V_{GS} - V_{th}$. Drain current results via the transport of charge injected at the source contact through two distinct mechanisms, significantly, the net behavior depends on source-gate overlap, S [37]. For short S, Mode I injection dominates with charges injected by thermionic-field emission over the barrier, however the majority of SGT benefits arise from Mode II current, where charge injection occurs under a low electric field and is ohmic in nature [38]. The source-gate overlap (also denoted "source length"), S is therefore a key design parameter. The quality of saturation improves with longer S, but there is an inevitable trade-off with operating frequency due to the increased overlap capacitance [28]. Still, for many applications of interest to TFT circuits (e.g. bio-sensing), the frequency of the signal is typically much slower than the device bandwidth. A further consideration for S is the temperature coefficient of the drain current. As thermionic-field emission is highly sensitive to changes in temperature, short S is associated with a more positive temperature dependence (TD) than longer S [37], [39]. Yet with appropriate device design, SGTs do not suffer from deleterious effects such as thermal runaway [30].

SGTs are versatile devices and possess many advantages for circuit designers. Particularly relevant to this communication is the resilience to material and geometrical variability [23]–[26], [31], which allow SGT circuits to operate without requiring complex compensation or support elements. Since the fabrication process is largely identical to that of many staggered TFTs, SGTs can be incorporated alongside conventional technology with only minor changes [24].

Here, we demonstrate the benefits of implementing well-known highly compact two transistor (2T) circuits, the common source amplifier and the current mirror, using SGTs (Fig. 1). By realizing these circuits with SGTs, their functionality is substantially improved. The extremely high output impedance leads to behavior close to ideal in both circuits, and the SGT's inherent temperature sensitivity is exploited for superior circuit functionality.

II. Experimental Section

A. Device and Circuit Fabrication

Low temperature polysilicon SGTs were fabricated in a top contact, bottom gate self-aligned process (see Fig. 1a and Tables S1 and S3 in the Supplementary Material) as per [11] with active layer thickness $t_s = 40$ nm and gate insulator thickness $t_i = 400$ nm (200 nm SiO_2 and 200 nm SiN_x). The Schottky source contact was realized with Cr and included a shallow P or BF_2 barrier modification implant for tailoring energy barrier height (~0.4 eV). Bulk doping was used for threshold engineering, creating devices that operate in depletion mode (normally-on) [28]. Both the Schottky source and Ohmic drain contacts included a field plate structure of 4 μm

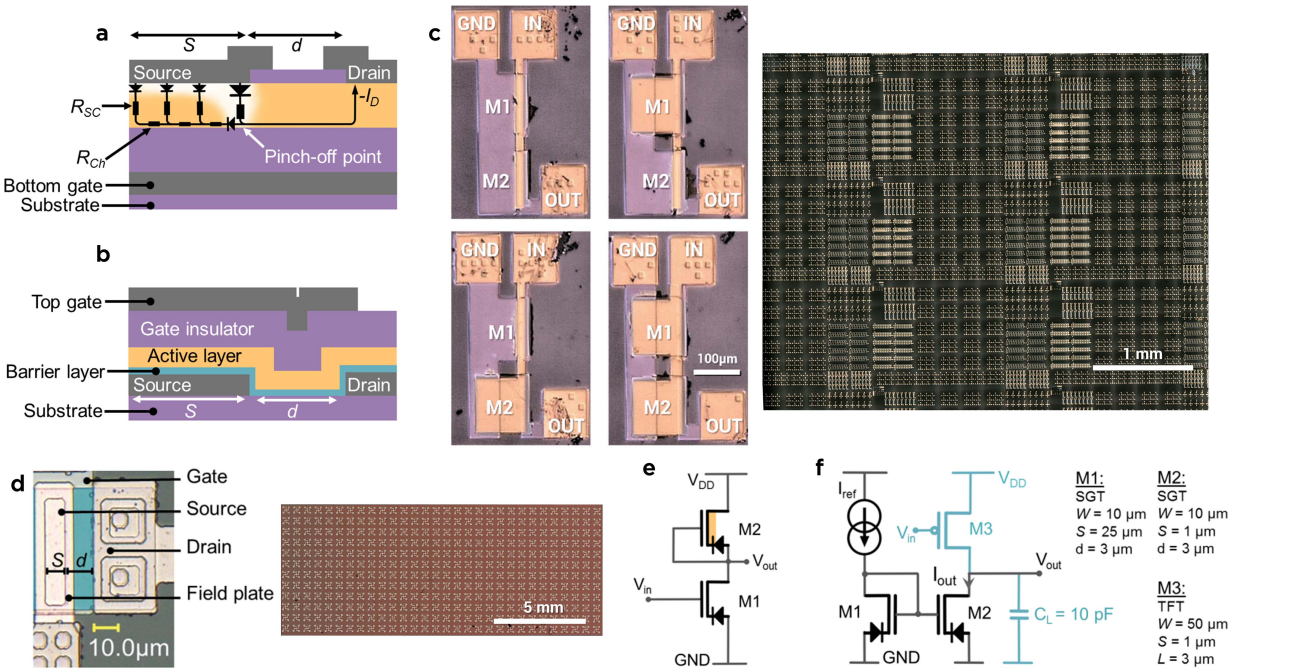

Fig. 1. Source-gate transistor devices and circuits. Schematic cross-sections of source-gated transistors (SGTs) in a) polysilicon with Schottky source and b) IGZO with thin insulating barrier layers at the contacts, showing the layer structure, source-drain gap (*d*), source-gate overlap (also called source length, *S*), and the charge injection paths from the edge and bulk of the source. c) Photomicrograph of current mirrors using IGZO tunnel contact SGTs fabricated as per Ref. [32] with various combinations of *S* and general view of the substrate. d) Photomicrograph of a typical polysilicon SGT fabricated as per Ref. [23] and general view of the substrate. e) Circuit diagram of an SGT common source amplifier with enhancement mode drive device (M1) and depletion mode ($0V_{GS}$) load (M2). f) Current mirror using *n*-type SGTs and a constant current source (in black) for the current copying performance and temperature behavior experiments. The full circuit is used when studying temperature-dependent delay in a common-source amplifier with M3 as the driver, M2 as the temperature-dependent active load, C_L as the capacitive load, and sizes as shown.

extension and 120 nm height in SiO_2, designed to provide relief from the drain induced electric field, thereby inhibiting bipolar amplification [47]. Additional device dimensions of the polysilicon amplifier circuits included a driver SGT with width, $W = 50\ \mu$m and source-gate overlap, $S = 8\ \mu$m, and load SGT with $W = 4\ \mu$m and $S = 4\ \mu$m. Both SGTs included source-drain gap $d = 10\ \mu$m. For the polysilicon current mirrors circuits, the device dimensions were $S = 2\ \mu$m with $d = 6\ \mu$m and $d = 10\ \mu$m, and $S = 8\ \mu$m with $d = 10\ \mu$m. These S values ensure that Mode II charge injection determines the drain current and the d values were chosen to highlight that the source-drain separation or channel plays no role in current modulation [38].

Top gate, bottom contact SGTs (Fig. 1b) and circuits (Fig. 1c) were fabricated in IGZO (additional data in Supplementary Tables S1 and S3), with the full process flow available as per Ref. [32]. The tunnel contacts were formed by ALD deposition of 3 nm Al_2O_3 on top of Ni source and drain. Active layer thickness $t_s = 35$ nm and gate insulator thickness $t_i = 98$ nm (ALD Al_2O_3). For device measurements $S = 45\ \mu$m and $S = 9\ \mu$m, with circuit dimensions $S = 1\ \mu$m, $S = 45\ \mu$m and $d = 6.5\ \mu$m, $d = 50\ \mu$m, respectively. Device widths $W = 110\ \mu$m.

Electrical characterization was conducted on a Wentworth probe station with a six-probe manual setup. An additional Weir 413D voltage source was used as the supply rail for the amplifier circuits. Measurements were performed with a Keysight B2902A source/measure unit (SMU) connected to the probe station.

For the pressure pad weight measurements, the sensor was connected in a potential divider with the SMU acting as a power rail. The pressure pad was calibrated using a plastic weigh boat by performing a voltage transfer characteristic sweep to obtain the operating point of the amplifier circuit. Input current was measured during sensing of low mass objects over time and used to convert to input voltage, while output voltage was measured directly with the SMU (See video in Supplementary Material).

The same method was used for the pulse measurement system. A white LED with a current limiting resistor in series and a phototransistor with another current limiting resistor were mounted on each side of a laser-cut acrylic finger-clip. Both the LED and phototransistor subsystems where biased directly from the SMU. The user's finger was positioned between the two parts of the finger-clip and the amplified signal was measured directly with the SMU (See video in Supplementary Material).

For the temperature-controlled ring oscillator demonstrator, the external system was realized on a breadboard using off-the-shelf components and connected to the SGT current mirror ($S_1 = 2\ \mu$m, $S_2 = 8\ \mu$m) via the probe station. CMOS inverters (TI CD4049UBE) were used to create a 3-stage ring oscillator with current-controlled positive supply though p-channel MOSFETs (ZVP4424A). 10 nF ceramic capacitors where used to load each oscillator stage to induce operation in the desired frequency range. The ring oscillator was buffered by a CD4049UBE inverter. At the start of the measurement, the temperature of the stage was stabilized at 35 °C

(Wentworth Hot Chuck Controller HC250) and the buffered output of the oscillator was measured using a Tektronix DSOX1102A oscilloscope at various temperatures. A video was recorded starting at 35 °C and with the HC250 programmed to increase rapidly to 70 °C. It should be noted that, while the video shows the qualitative effect of increasing oscillating period, it should not be compared with the plotted data, due to the thermal inertia of the substrate.

B. Device and Circuit Simulation

Electrical and thermal co-simulations of polysilicon devices were performed using Silvaco Atlas v. 5.24.1.R. Simulated and fabricated devices differ deliberately, in order to investigate more aggressively scaled geometries, while continuing exploration from previous TCAD studies. A typical device structure is shown in Supplementary Fig. S1 and geometrical and material parameters are summarized in Supplementary Tables S1 – S3.

For both simulation studies, devices shared the same width, materials and layer thicknesses, including a gate (work function, $WF = 4.7$ eV) that overlapped both source and drain, separated by 60 nm SiO_2 gate dielectric. A 30 nm active layer was defined with polysilicon material parameters that have consistently verified SGT behavior, including defects, impact ionization and Klaasen's band-to-band tunneling [46]. Both source and drain contacts included field plate extensions of 500 nm with 20 nm height, separated by SiO_2 from the semiconductor. A full list of simulation parameters has been included in Tables I, II and III of the Supplementary Material.

For the amplifier study, SGT device dimensions included $S = 5$ μm and 5 μm drain contact length [46]. As low source barriers reduce the intrinsic gain in SGTs [23], Schottky source contacts were simulated with three different work functions, $WF = 4.45$ eV, 4.5 eV and 4.57 eV. Source-drain separation was set at $d = 3$ μm to prevent the channel from restricting the current even for low source barrier heights. For TFTs, gain is determined by channel length [55], therefore devices with $L = 3$ μm, 10 μm and 30 μm were simulated using $WF = 4.17$ eV for ideal Ohmic contacts at both source and drain. Depletion mode devices were simulated by including uniform $4 \cdot 10^{17}\text{cm}^{-3}n$-type doping.

SGT device dimensions in the current mirror study included $S = 1$ μm, 5 μm and 25 μm with $d = 3$ μm and a drain contact length of 1 μm.

Amplifier and current mirror circuits were simulated with Mixed-Mode Atlas, in which a SPICE circuit is described and simulated using both SPICE (i.e. capacitors) and Atlas (physically-modeled) devices. Voltage transfer characteristic sweeps of common source amplifiers were studied in d.c, as was the temperature dependence of output current for the current mirrors. An a.c. analysis was performed on amplifiers with sufficient gain and output swing, while transient simulations were performed for the time-response of the current mirror-based temperature-sensitive delay circuit.

D.c. simulations of common source amplifier circuits with 0V_{GS} and diode loads provided the value of the switching point, V_m, and an estimation of gain from the slope of the transfer curve. Simulations were performed on circuits formed with SGTs with $WF = 4.5$ eV and/or TFTs with different L in all driver-load combinations. Load width was kept $W = 10$ μm, while driver width varied. An a.c. analysis on practical circuit configurations was performed using a 1 mV amplitude a.c. input voltage for obtaining the gain-bandwidth plot and cut-off frequency, f_T.

III. Common Source Amplifiers With Depletion-Mode Active Loads

In addition to the low-cost, high throughput processes stated above, it is generally preferred to design unipolar circuits (i.e. all transistors operating as either electron or hole devices) for convenient, facile fabrication, cost reduction [12], [40] and improved manufacturing yield [41]. Pseudo-CMOS inverter circuits are often implemented as high-gain analog amplifiers due to their comparatively large gain [42], but the increased circuit complexity (4T per stage) and additional biasing signal presents additional challenges. Depletion load (0V_{GS}) amplifiers (Fig. 1e) are generally the most compact [18], [43], however their achievable gain is limited by the intrinsic behavior of the transistors. In order to increase amplification, designers resort to either cascading gain stages (which reduces the gain-bandwidth product and increases the number of transistors), or protecting the gain device with another transistor placed in series in a cascode configuration [44] (which requires higher supply voltages and potentially additional bias circuitry). Intrinsic transistor gain, $A_v = g_m/g_d$, plays a crucial role in the overall gain of the amplifier circuit. While the g_m of SGTs is lower than conventional TFTs with Ohmic contacts, the output conductance g_d can be many orders of magnitude lower, and as such the SGT is far more capable of achieving higher A_V values [23]. The low temperature polysilicon (LTPS) devices, fabricated as per the process in Ref. [23] have demonstrated values as high as $A_v = 10^5$, remarkably high for polysilicon, a material which is typically affected by the kink effect [45] and grain boundaries [25]. In IGZO SGTs, $A_v = 2.9 \cdot 10^5$ has been recently reported [26] and these device performance characteristics have been newly confirmed in unipolar circuits [46]. Here, we concentrate on unipolar SGT common source amplifiers. We provide examples of pressure/weight and bio-sensing systems with minimal complexity to confirm the reduced design restrictions of this easily scalable device architecture.

The transfer and output characteristics of Fig. 2a and 2b provide the results from measurements taken of polysilicon SGTs similar to the device in Fig. 1d (details of device geometry as per Supplementary Table S1). Common-source amplifier circuits (Fig. 1e) have been constructed using two devices of suitable width. Traditionally the drive transistor M1 is wider (here $W_1 = 50$ μm) for increased g_m and load transistor M2 is narrower for increased a.c. impedance (here $W_2 = 4$ μm). The barrier modification implant of M1 was chosen to be low to provide a high g_m, while a high effective barrier (for low drain current and low g_d) was chosen for M2. Here, both devices operate in depletion mode, however M1 could be either an enhancement or depletion mode device. The shorter source of M2 ($S_2 = 4$ μm) demonstrates a slight

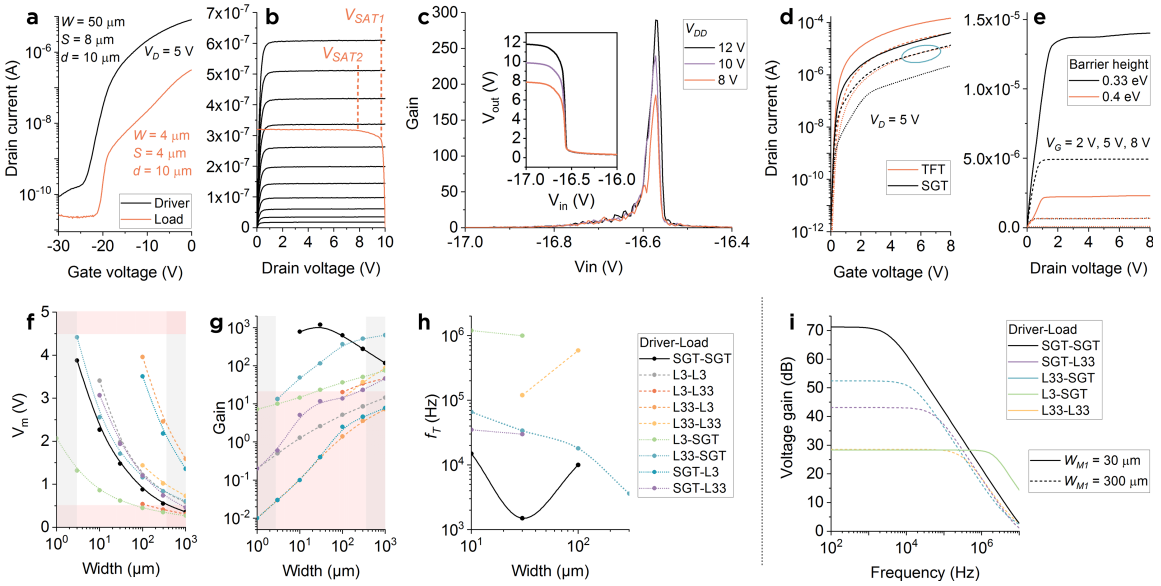

Fig. 2. SGT characteristics enable exceptional gain in common source amplifiers. a) Measured transfer characteristics of polysilicon SGTs, M1 driver and M2 load. b) Driver M1 output characteristics (black curves, $V_{\mathrm{Gmax}} = -15$ V, step 0.5 V) and superimposed M2 load line (orange, $V_G = 0$ V). V_{SAT1} occurs as a result from pinch-off at the source and V_{SAT2} represents channel pinch-off of the parasitic FET. c) Gain for various V_{DD} with an inset of a voltage transfer characteristic of the SGT $0\mathrm{V_{GS}}$ amplifier showing reduced gain when the voltage of the load is between V_{SAT1} and V_{SAT2}. d) Transfer characteristics from the simulation study where $V_D = 5$ V for conventional TFTs with different channel lengths, $L = 3$ μm (solid), $L = 10$ μm (dashed), $L = 33$ μm (dotted) and SGTs with $d = 3$ μm and different source metal work function, $WF = 4.45$ eV (solid), $WF = 4.5$ eV (dashed), $WF = 4.57$ eV (dotted). For the SGT with $WF = 4.5$ eV, the current achieves comparable levels as a conventional TFT with $L = 33$ μm (circled in blue). e) SGT output characteristics from simulations ($V_G = 2$ V, 5 V and 8 V) showing typical low saturation and high output impedance. While the $WF = 4.5$ eV SGT demonstrates a small increase in V_{SAT} and gain loss at higher V_G. f) Simulation results for device width versus switching point V_M of the $0\mathrm{V_{GS}}$ load amplifiers for various M1-M2 device combinations with constant load width, $W = 10$ μm. Channel length L is identified for TFTs. Grey shaded areas indicate impractical widths, while red shaded areas indicate regions of insufficient output swing. g) Simulated gain for various device combinations, again, the grey shaded areas represent impractical widths, while the red shaded area indicates insufficient gain. SGT combinations provide high gain, as expected, peaking with M1 $W = 30$ μm, indicating a suitable driver to load width ratio. h) Operating frequency f_T as a function of M1 width for practical device combinations from (f) and (g). Combinations using an SGT load (M2) offer the best trade-off for gain and frequency. i) Simulation results for the a.c. analysis for feasible combinations, highlighting the benefits of SGTs for high gain amplification or as a load device for improved bandwidth in hybrid SGT-TFT amplifiers.

loss in gain, as observed in the superimposed load curve of Fig. 2b when compared with the superior output characteristics of M1 $S_1 = 8$ μm (black curves), which exemplifies the low saturation voltage and high output impedance normally associated with SGTs. The M2 load curve further indicates two saturation points [24], V_{SAT1} where the SGT pinches-off due to the capacitor divider, and V_{SAT2} where the parasitic FET of the channel pinches off at the drain $V_{SAT2} = V_{GS} - V_{th}$. Improvements in field plate design [47] and/or longer S would improve the quality of saturation. However, in the present use case of a $0\mathrm{V_{GS}}$ amplifier, only the headroom of the output swing in the voltage transfer characteristics (Fig. 2c inset) is affected. The circuit gain was estimated from the slope of the voltage transfer characteristics (dV_{out}/dV_{in}) for several supply voltages, V_{DD}, with gain increasing for higher V_{DD} (see Supplementary Fig. S2). The circuit function is as expected, when a sine wave is presented at the input, an amplified sinewave of opposite phase is produced at the output (Supplementary Fig. S3). The gain achieved for this M1-M2 combination (Fig. 2c) was measured at ~290 (V/V) (49.5dB). With improvements in device geometry of M2, the sharp curves of the M1 transition (inset of Fig. 2c) could be realized, as well as operation at lower V_{DD} could be enabled. The results of the unipolar polysilicon $0\mathrm{V_{GS}}$ amplifier are extremely promising, particularly in light of the facile approach to circuit implementation when compared to recent achievements of 264 (V/V) in advanced, complementary dual-material (polysilicon, IGZO) processes [48] of significantly more complexity and cost.

SGT design is versatile, with many parameters to take into account [28], [37], depending on the application. In order to explore some of the design features for common source amplifiers, simulations of devices were performed with Silvaco Atlas. Moreover, using the package's mixed-mode capability, circuits comprising the physically-simulated SGTs are embedded in SPICE code and co-simulated (see Section II B). Polysilicon was selected as the active material for several reasons: the material is well understood and in common use; intrinsic gain in polysilicon transistors is usually low due to the kink effect; the parameters have consistently been verified with the SGTs; simulations complement the measurement results, to further understand SGT design for amplifiers in a "worst case" scenario (see Table S2 in the Supplementary Material for simulation geometries and parameters).

The simulated transfer characteristics of SGTs with three barrier heights and FETs with three channel lengths (Fig. 2d) indicate that for an SGT with moderate barrier height $\Phi_B = 0.33$ eV, the drain current produced is comparable to that of a TFT with channel length $L = 33$ μm when operating around $V_G = 5$ V. Considering the source contact

length for both devices was 5 μm, the SGT delivers similar current at approximately a third of the device size, which is important when layout area poses a constraint. Additionally, the saturation voltage of the SGT is lower for the same drain current. As gain is moderated by barrier height in SGTs [23], higher barriers typically result in higher gain with lower saturation voltages, demonstrated by the curve drawn for $\Phi_B = 0.4$ eV of Fig. 2e, but for the purposes of this study $\Phi_B = 0.33$ eV offers suitable g_m while maintaining the signature flat output characteristics associated with SGTs. However, it is important to note that at high V_G, the effective barrier becomes low and the voltage drop in the channel cannot be ignored. Consequently, the transistor gradually transitions toward behaving akin to a TFT [49], with an increase in g_d which would lead to gain loss (Fig. 2e).

Common source amplifier circuits with $0V_{GS}$ load have been simulated. M1 and M2 were chosen from all combinations of the SGT with $\Phi_B = 0.33$ eV and TFTs with $L = 3$, 10, 33 μm. M1 width varied while M2 width was a constant 10 μm. Switching voltage and gain are shown in Figs. 2f and 2g. Some permutations are unsuitable for implementation. The grey shaded areas of the switching point V_m in Fig. 2f as well as gain in Fig. 2g indicate unsuitable M1 width, as the smaller values are difficult to realize with large-area fabrication techniques, and for large values, device sizes become both impractical to fabricate and susceptible to self-heating effects, particularly in flexible circuits [50]. The red shaded areas of Fig. 2g indicate insufficient head/legroom of the output swing, while in Fig. 2f, the red shaded area indicates insufficient gain (below 2). As expected, g_m and gain increases with W in TFTs, but the amplification is modest and comes at the price of area. The gain of the entirely SGT-based combination was the highest, peaking above 1000 (60 dB) for $W = 30$ μm, indicating a suitable driver-to-load W ratio of 3, which allows for a compact layout. For lower W of M1, there is insufficient drive current produced to match the current of M2 and therefore higher V_G is required. However, at high V_G the SGT with $\Phi_B = 0.33$ eV leads to gain loss as well as increased V_{SAT1}, evident in the output characteristics of Fig. 2e. For large W, lower V_G on M1 is required, however, the SGT then starts to operate closer to the threshold, where the channel controls the current instead of the source contact area. The investigation also included common source amplifiers with diode-connected active loads. However, since in this connection the load transistor's operating point is $V_D = V_G$, no benefits can be derived from the saturation behavior of an SGT over TFTs, as the SGT is permanently operated above V_{SAT2} (see Supplementary Fig. S4).

The results from the a.c. analysis in Fig. 2h and 2i confirm the predictable trade-off between gain and bandwidth, particularly with SGT-exclusive circuits. (See also Supplementary Figs. S5 and S6 for a gain-bandwidth plot containing more circuit combinations and a Bode plot including the phase evolution and phase margin). Importantly, for many applications involving biosignals, there is rarely need for high bandwidth due to the comparatively low-frequency nature of the measured quantities. Therefore SGT-only circuits, with $f_T = 20$ kHz and gain values over 700 (57 dB), provide appropriate design space for bio-sensing applications. For the majority of hybrid SGT-TFT and TFT-SGT M1-M2 combinations, there would be little need to alter any process steps to realize both devices, as the benefits of these combinations can be achieved with SGT exclusive circuits, where gain can be sacrificed for improved bandwidth. However, the M1 TFT with $L = 3$ μm driver and M2 SGT hybrid amplifier indicates there can be advantages for adapting fabrication processes with gain around 20 (26 dB) at $f_T \sim 1$ MHz. Due to the high g_m of M1 combined with the high output impedance of M2, these high bandwidths can be achieved over any exclusive TFT combination, taking into account that neither device has been fully optimized. For example, when using the SGT as a load device, the output conductance can be reduced by improving the quality of saturation by using a higher source barrier, as well as increasing S. Applications such as low power wireless communications for IoT or embedded power management could benefit from this hybrid TFT-SGT combination.

In order to demonstrate circuit applications using SGT common source amplifiers with $0V_{GS}$ load, two experiments were conducted: pressure sensing of relatively light masses for extreme sensitivity and pulse detection. Fig. 3a and 3b show a block diagram of the pressure sensing experimental setup and circuit schematic, respectively (see Section II A) and Fig. 3c provides an example of a typical sensing setup for this experiment (see Supplementary Material for video). The results in Fig. 3d highlight the ability of 2T SGT amplifiers to detect objects with very low mass (feather $m = 40.9$ mg, grain of rice $m = 20$ mg). Fig. 3e and 3f show the block diagram of the pulse detector and circuit schematic, respectively, with Fig. 3g showing finger placement in the sensor. The results in Fig. 3h indicate that SGT gain is sufficient to detect a human pulse with significant signal-to-noise ratio using a simple 2T circuit. Here, the rate detected is 96 bpm (see Supplementary Material for video). These results were obtained in an electrically noisy environment using a rudimentary setup. While far from optimum, they indicate the potential of SGT circuits for sensors with minimal component count operating in real-life settings, and with the potential for facile and low-cost manufacturing using printed or roll-to-roll (R2R) processes.

IV. Current Mirrors With Geometrically Tuneable Temperature Dependence of Output Current

Current mirrors (CMs) are essential circuit blocks for analog circuit biasing and active loads in a multitude of signal processing, amplification and conversion applications. Device non-idealities usually limit current copying performance [51] with the numerous improvements proposed thus far generally coming at the expense of operating voltage, speed or complexity [52]. As previously noted, in emerging printed and flexible LAE circuits, minimizing components reduces area, thereby increasing reliability and ultimately yield [7].

Here, we present measurements on current mirrors using polysilicon SGTs [24] and the first report tunnel-barrier SGT circuits in IGZO [32]. Uniquely, we exploit the temperature dependence of SGT drain current on S [39] to

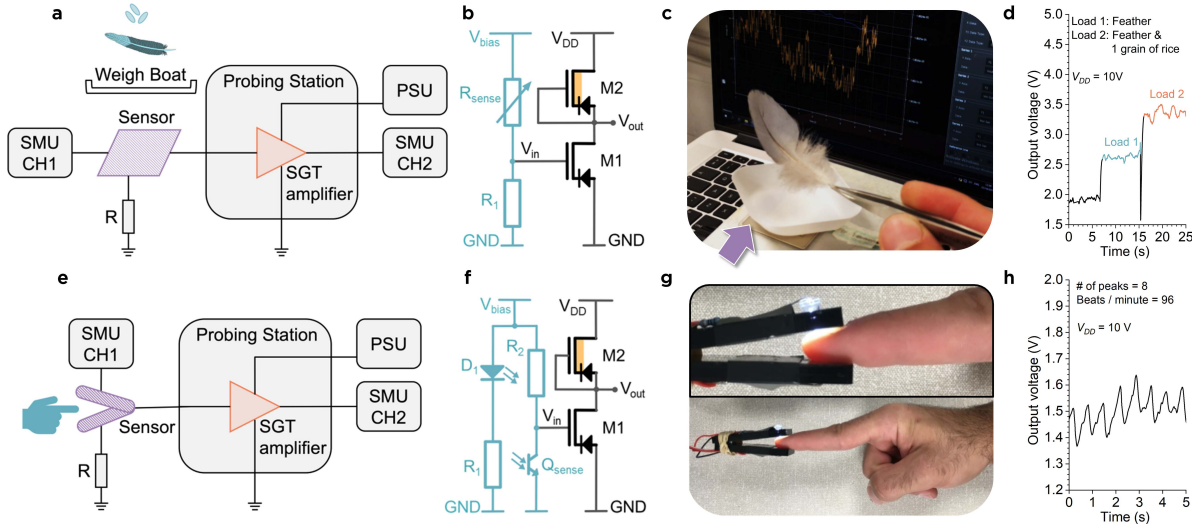

Fig. 3. Applications of two-transistor high-gain amplifiers. a) Block diagram of the weight measurement system with source measurement unit, power supply, pressure sensor and SGT amplifier circuit. b) Circuit diagram of an SGT amplifier with $0V_{GS}$ load including variable resistance pressure pad. c) Photograph of a typical experiment showing the pressure pad (arrow), weigh boat and feather. d) Output voltage of the SGT amplifier showing significant step changes when a feather is placed on the weigh boat (blue) and when a single grain of rice is subsequently added (orange). e) Block diagram of the pulse detection system. f) Circuit diagram of the depletion-load ($0V_{GS}$) SGT amplifier with optical sensing circuit. g) Finger placement during measurement. The light emitting diode (D_1) of (f) is seen on top of the sensor and the phototransistor (Q_{sense}) of (f) is located on the opposite side of the setup. h) The system tracks the user's pulse as detectable changes in output voltage.

demonstrate minimal, 2T CMs capable of producing output current with temperature dependence, which is either positive (PTD) or negative (NTD) controlled via the transistor design geometry. Current injected from the drain-side edge of the source has a high PTD, whereas the PTD reduces when increasing S, as injection from the bulk of the source begins to dominate [39]. Distinct temperature behavior can be obtained by varying S in otherwise identical devices. These minimal circuits generating currents with PTD and NTD prove useful in temperature sensing and self-regulating wearable electronics or sensor systems. We propose a current-starved ring oscillator [53], which adapts its operating frequency according to chip temperature through a negative feedback mechanism, for wide-ranging applications in emerging printed and flexible electronics: thermal safety of the circuit; user comfort and safety; homeostasis.

The SGTs were made according to Ref. [23] for polysilicon and Ref. [32] for IGZO with tunnel contacts. Simulations and the mixed-mode circuit capability were once again used to complement measurements and produce design recommendations for temperature dependent CM circuits.

Electrical data for the polysilicon SGTs are presented in Fig. 4a and 4b. The devices operate in depletion due to bulk doping and show typical low-voltage saturation and independence of drain current on d. Furthermore, saturated drain current is practically independent of drain voltage. Due to the 2-D charge injection process [39], drain current temperature dependence is marginally higher for the device with a shorter source. This behavior is exploited later for generating NTD and PTD currents using SGT current mirrors.

Simulated polysilicon enhancement-mode devices (Fig. 4c and 4d) show similar features. The SGT with $S = 1$ μm has reduced drain current, due to the small source area, and this current has a large PTD, as injection from the source edge dominates. Devices with $S = 5$ μm and 25 μm behave very similarly, indicating that, here, injection from the bulk of the source not only dominates, but saturates with increasing S as low as 5 μm [39].

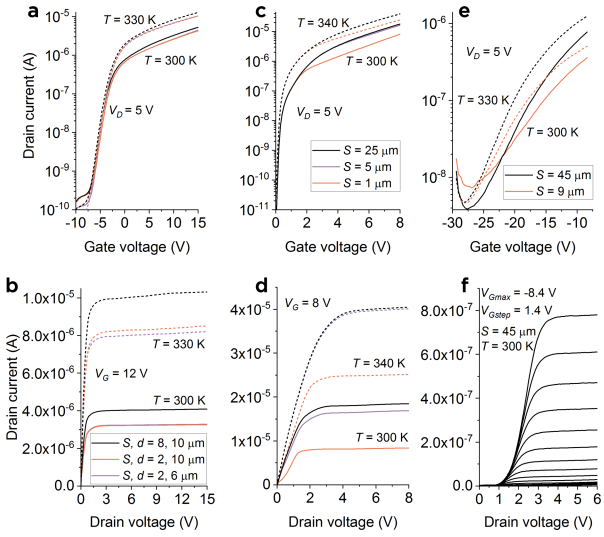

Fig. 4. The temperature dependence of SGT drain current varies with source geometry and can be exploited in compact temperature-sensing circuits. a) Transfer and b) output characteristics for the fabricated poly-Si SGTs. Early saturation and flat characteristics typical of SGTs are seen. Current is largely insensitive to d, changing more with temperature for the devices with greater S [39]. c) Transfer and d) output characteristics for the simulated polysilicon SGTs. More extreme values of S compared to the fabricated devices lead to stronger dominance of their respective operation [39]. A larger dependence of drain current on temperature is observed for the device with a smaller S, and the discrepancy between curves for $S = 5$ μm and $S = 25$ μm is minimal. e) Transfer and f) output characteristics for the fabricated IGZO SGTs with $d = 50$ μm. Injection and conduction processes are not fully understood, and appear to be complex, as the device with lower S demonstrates a lower dependence of drain current on temperature. Output curves are super-linear at low drain voltage [32], but the devices show low saturation voltage and flat saturated curves, typical of SGTs.

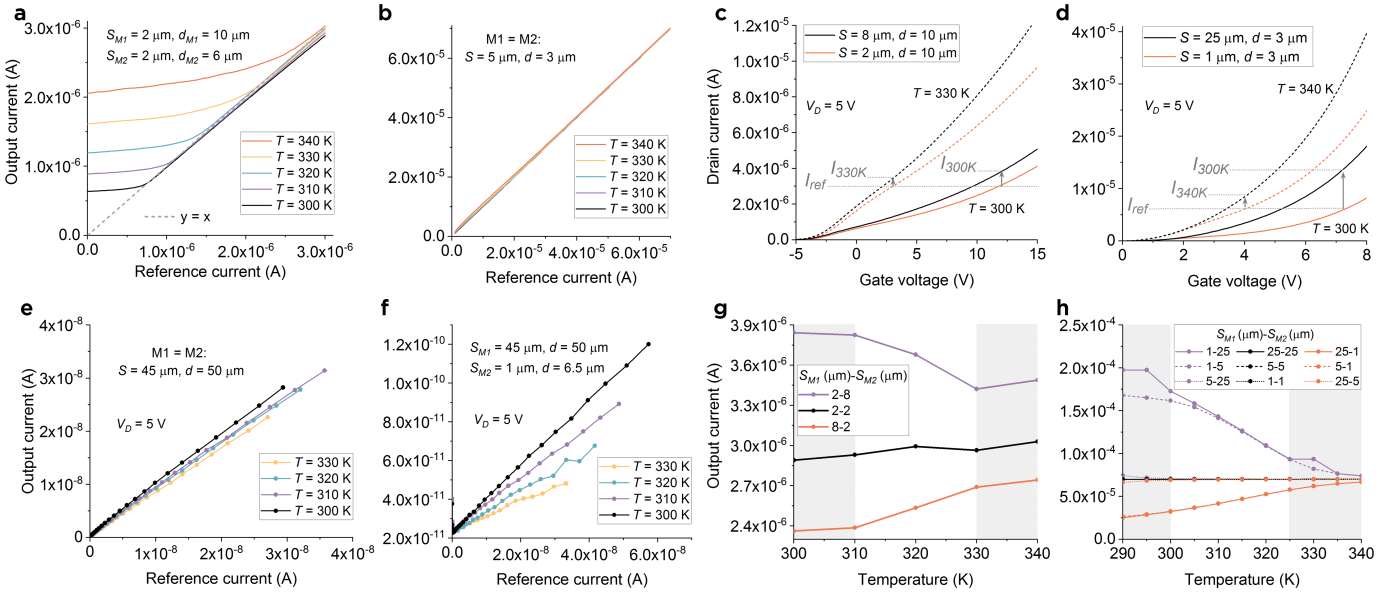

Fig. 5. SGT current mirror performance and temperature effects. a) The polysilicon current mirror copies current well with minimal dependence on temperature when M1 and M2 have equal S. As M1 operates in depletion (Fig. 4a), low currents cannot be copied correctly. b) Identical SGTs in the simulated polysilicon current mirror circuit achieve good current copying with negligible temperature dependence. c) Measured transfer curves (linear plot) for the polysilicon SGTs illustrating the mechanism for achieving a negative temperature dependence of output current using two devices with positive temperature dependence. d) As in (c), for simulated polysilicon devices, transfer curves for devices with extreme sizes of S. Obtaining e) small negative and f) larger negative temperature dependence of output current from CM circuits with IGZO SGTs in which devices are identical, or the device with the higher temperature sensitivity is at the input, respectively. It has been shown previously that d is unlikely to play a role in current control in such devices [32]. g) Negative, negligible or positive temperature dependence can be obtained by varying the relative S of the two transistors. h) A negative temperature dependence of output current is observed in current mirrors in which $S_{M1} < S_{M2}$. Minimal differences are observed for $S = 5$ and 25 μm, indicating that injection from the bulk of the source dominates even at $S = 5$ μm [39].

IGZO SGTs with thin insulating tunnel barriers have only recently been introduced [32] and while their operation is still under investigation, the electrical characteristics in Fig. 4e and 4f show that in this case drain current PTD is larger for the device with the longer source. Early saturation and flat saturated curves are observed. Low-voltage behavior is super-linear, as explained in [32], without impeding functionality in CM circuits, where transistors operate in saturation.

The CM in Fig. 1f (devices in black, output to V_{DD}) is formed by input transistor M1 and output transistor M2. The flat output curves of SGTs predict good current copying, notably without cascoding. Fig. 5a shows the current copying performance of the measured polysilicon circuit with devices of equal S. A linear relationship between output and input current is established, independent of d and temperature, showing the robustness of the minimal 2T CM using SGTs. Copying performance is lost at low current and higher temperature, as in the depletion-mode devices, V_G of M1 and M2 cannot reduce below 0 V due to the diode connection across M1. Even as circuit implementations would optimize these parameters for the desired application, the present design maintains its functionality in the temperature range of interest for bio-sensing and wearable applications. Supporting the measurement data, the simulated CM using identical enhancement-mode polysilicon SGTs shows excellent, temperature-independent copying (Fig. 5b).

SGT-based current mirrors can exploit the variable TD of drain current with S to generate output currents with negligible TD, PTD or NTD. Fig. 5c shows the principle behind obtaining NTD: M1 and M2 are chosen so that the PTD of M1's drain current is higher than that of M2's (i.e. relatively shorter S for M1 for Schottky-contact SGTs). When M1 is driven with a constant current, I_{ref}, an increase in global temperature will result in a reduction of gate voltage for M1 and M2, but since M2 has a lower PTD than M1, its current (i.e. CM output current) reduces with temperature. A -0.53 %/K temperature sensitivity output current (TSOC) is measured in Fig. 5g for this setup. Conversely, PTD output current is obtained by choosing M2 to have the shorter S, yielding a TSOC of $+0.64$ %/K. For identical transistors, TSOC is minor, at $+0.06$ %/K.

TCAD simulations (parameters in Supplementary Table S3) show similar behavior (Fig. 5d) but a larger TSOC due to the larger discrepancy in S between devices (1 μm and 25 μm): -1.83 and $+3.15$ %/K, respectively, and a negligible $+0.002$ %/K TSOC for identical transistors (Fig. 5h).

IGZO circuits achieve the same net effect. The -0.5 %/K TSOC obtained at $I_{ref} = 20$ nA when using identical devices (Fig. 5e) may be attributed to differential threshold shifts and self-heating in M1 and M2 at the fairly high gate voltage, relative to their threshold voltage. When M1's drain current has a higher PTD than M2's (Fig. 5f), a -1.17 %/K TSOC is obtained. The small S of M2 produces a low output current.

An example of an application that could benefit from this unique circuit functionality is a current-starved oscillator [53], [54] throttled with NTD currents. The proof of principle

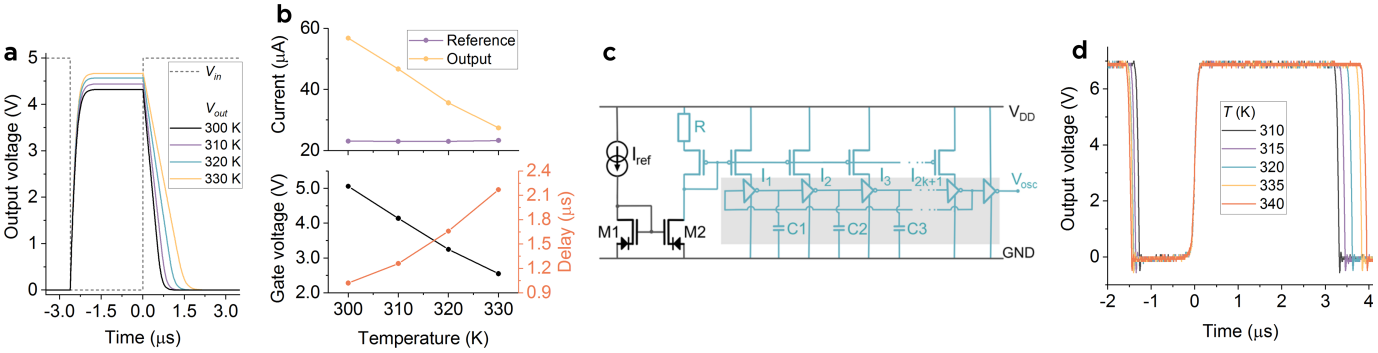

Fig. 6. Applications of the negative temperature dependence of output current in SGT current mirrors. a) Inverter stage delay dependence on temperature as per the setup in Fig. 1f. b) Evolution with temperature of the switching delay, output current, and gate voltage of transistors M1 and M2 in Fig. 1f. c) The oscillating frequency of a ring oscillator circuit with an odd number of inverters (I_{2k+1}) and a buffer stage (shaded) can be throttled by limiting the current using the transistors shown in blue [53]. For example, a throttle current which reduces with temperature is generated by M2 and is mirrored in all branches, resulting in a reduction of the operating frequency with increasing temperature. All *p*-type devices are identical, respectively, and may be TFTs or SGTs. d) Measurements of the output waveform of the circuit in (c) with increasing temperature resulting in a reduction of operating frequency (see Supplementary Material for video).

result is illustrated in Fig. 6a. The common-source amplifier in Fig. 1f uses the CM as active load and is driven with a square wave. As temperature rises (Fig. 6b), the CM output current reduces, increasing the time for load capacitor ($C_L = 10$ pF) discharge. Fig. 6b shows the evolution of the delay, CM output current and CM gate bias voltage with temperature for a constant reference current. The CM and ring oscillator in Fig. 6c demonstrates a practical implementation of the current-starved oscillator concept. The output waveforms in Fig. 6d shows the time period increasing with temperature, resulting in reduced operating frequency (see Supplementary Material for video). The circuit in Fig. 6c, and similar implementations [54], would self-regulate the operating speed and power dissipation of the circuit it drives, with many applications in low-cost LAE. If necessary, a precise clock may be generated separately.

Stability and aging are essential considerations for large-area electronic circuits. Well-designed SGTs operating above threshold (e.g. [31]) inherently shield against bias stress and material non-uniformity effects, as the semiconductor channel does not control the magnitude of drain current, making them robust candidates for prolonged operation in low-cost circuits such as those described above.

V. Conclusion

In thin-film technologies, minimizing the component count is highly desirable, as it leads to reduced circuit area and improved yield. We have demonstrated common source amplifiers and current mirrors with minimal, two-transistor (2T) designs in polysilicon, supported by Silvaco Atlas simulations, as well as current mirrors in IGZO. These circuits use the SGT's high output impedance for high gain amplification and accurate current copying without additional circuit components (e.g. cascode) and demonstrate a major step in LAE circuit design not seen for over half a century.

Depletion-load amplifiers show 49dB gain in a single stage, the highest reported, and enabled by the greatly reduced kink effect in polysilicon SGTs. Essentially, SGT current mirrors are shown to exploit the source-gate overlap (S) as a design parameter, which changes the temperature dependence of drain current. This results in the ability to generate output currents with either negligible, positive, or negative temperature dependence, starting from a temperature-independent reference current and using only two SGTs. As with all current mirrors, rigorous layout design is required to reduce the temperature difference between the essential transistors, thus minimizing non-ideal behavior. In principle, SGTs and TFTs can be used in the same circuit, such as in increased bandwidth amplification and the proposed application to a temperature-self-regulating oscillator. The high output impedance and quality of saturation in an SGT can be improved with increased barrier height and longer S, both of which would lower g_d and hence further improve A_v when the transistor is used as a load.

The wide applicability of such circuit blocks to ubiquitous sensors, wearables, signal conditioning, data processing and conversion, etc. is complemented by the material-agnostic nature of SGT operation. We expect that these blocks will complement the traditional design tool-box for the engineers conceiving the next generation of ubiquitous, energy-efficient electronics.

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