Highly Sensitive Nanotesla Quantum-Well Hall-Effect Integrated Circuit Using GaAs–InGaAs–AlGaAs 2DEG

Mohammadreza Sadeghi, James Sexton, Chen-Wei Liang, and Mohamed Missous, *Senior Member, IEEE*

***Abstract*— This paper reports on the first low power (10.4 mW) and ultrasensitive linear Hall-effect integrated circuits (LHEICs) using GaAs–InGaAs–AlGaAs 2D electron gas technology. These LHEICs have a state-of-the-art sensitivity of 533 μV/μT and are capable of detecting magnetic fields as low as 177 nT (in a 10-Hz bandwidth), at frequencies from 500 Hz to 200 kHz. This provides at least an order of magnitude improvement in sensitivity and a factor of four improvements in detectability of small fields, compared with commercial Si linear Hall ICs.**

***Index Terms*— Linear Hall effect integrated circuit, LHEIC, 2DEG, GaAs-InGaAs-AlGaAs, pHEMT.**

I. Introduction

HALL Effect integrated circuits are widely used in such diverse applications as automation, medical, electronic and electrical industries [1]. AC linear integrated circuits are most commonly employed in these applications and are used to detect AC magnetic fields and produce an output which is proportional to the strength of the detected magnetic field. Commercially available Hall Effect linear ICs are all based on silicon CMOS technology mainly due to their small dimension and low cost [2]–[5]. However, shortcomings of these ICs include low magnetic field sensitivity, limited operating frequency and temperature ranges and high power consumption. Due to the inherently poor silicon Hall sensor material properties, devices made of III–V semiconductors have attracted a great deal of interest by virtue of their high electron mobility combined with moderate sheet carrier densities, low temperature dependences of the output Hall voltage and large signal-to-noise ratios (S/N) [6]–[10]. However, the majority of this work to date has been concerned with single Hall elements with no reports of fully integrated Hall Effect circuit using the III–V semiconductors apart from [11]–[13] describing a hybrid circuit using ion implanted GaAs for which the performances were less than ideal due to the difficulties of the technologies used at the time. At present, the most sensitive commercial linear Hall integrated circuits (based on silicon) are made by Allegro (A1324), Melexis (MLX90242) and Honeywell (SS39ET). These have sensitivities of 50 mV/mT, 39 mV/mT and 14 mV/mT respectively and are capable of detecting magnetic fields as low as 864 nT, 6500 nT and 652 nT respectively in a 10 Hz bandwidth. These ICs also have a maximum cut off frequency of 10 kHz and a minimum power consumption of 12.5 mW from a 5 V supply [14]–[16] largely as a result of the on-board offset cancellation circuitry. In order to provide a higher sensitivity, lower field detectability and wider operating frequency range, a new type of linear integrated circuit has been developed in this work and which utilises a two Dimensional Electron Gas (2DEG) system. The high electron mobility and the moderate sheet carrier densities permit both magnetic and circuit functionalities [17]. This integrated Hall IC is based on the GaAs-InGaAs-AlGaAs system, which is a relatively mature technology enabling accurate modelling and simulation of transistors for the development of Process Development Kits (PDK). All circuit elements required for successful integration, have been developed in this work culminating in the design and fabrication of low power linear integrated Hall ICs with unprecedented sensitivities.

Manuscript received September 21, 2014; revised November 2, 2014; accepted November 2, 2014. Date of publication November 5, 2014; date of current version January 15, 2015. This work was supported by the Science and Technology Facilities Council under IPS Grant Proposal ST/L000040/1. The associate editor coordinating the review of this paper and approving it for publication was Dr. Kailash Thakur.

The authors are with the School of Electrical and Electronic Engineering, University of Manchester, Manchester M13 9PL, U.K. (e-mail: mohammadreza.sadeghi@manchester.ac.uk; james.sexton@manchester.ac.uk; chen-wei.liang@postgrad.manchester.ac.uk; m.missous@manchester.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSEN.2014.2368074

TABLE I
STRUCTURE OF EPITAXIAL WAFER XMBE303

Layer	Composition	Thickness (Å)
Cap	GaAs	50
Supply	$Al_{0.35}Ga_{0.65}As$	200
Δ-doping		
Spacer	$Al_{0.35}Ga_{0.65}As$	50
Channel	$In_{0.15}Ga_{0.85}As$	120
Buffer	GaAs	6000

II. Material Growth and Fabrication

All wafers used in these studies were grown in-house using a solid-source RIBER V100 Molecular Beam Epitaxy (MBE) system. The epitaxial profile of a typical 4" wafer (XMBE303) grown on a (100) GaAs semi-insulating substrate is shown in Table 1.

The pseudomorphic high electron mobility transistor structure consists of a GaAs buffer layer, a channel/active layer of strained $In_{0.15}Ga_{0.85}As$ cladded by an $Al_{0.35}Ga_{0.65}As$ spacer and supply layers, a Si delta doped layer and finally

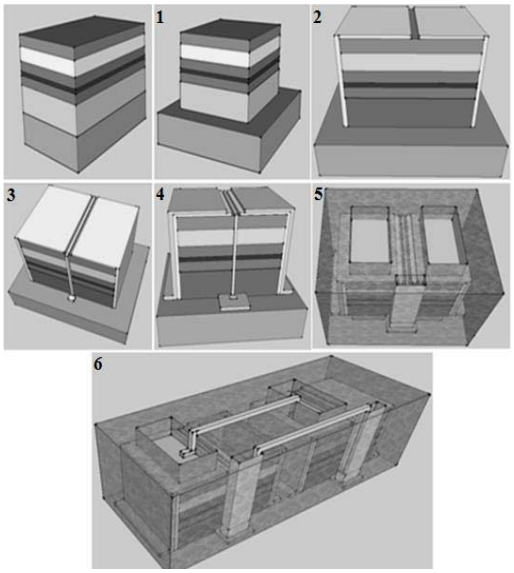

Fig. 1. Fabrication steps of pHEMTs, sensors and integrated circuits. 1. Mesa, 2. Ohmic, 3. Gate, 4. Bond pad, 5. Via (openings) and 6. Bridge.

a GaAs cap layer. The as-grown sheet carrier density and mobility values were obtained using Hall Effect measurements at room temperature and determined to be 1.57×10^{12} cm^{-2} and 6447 cm^2/V.s respectively.

The thicknesses of the spacer layer and the magnitude of the delta doped layer control the amount of charge trapped in the Quantum Well, n_s and therefore, the current sensitivity of the Hall sensing element. As the sensitivity of the Hall element is inversely proportional to n_s, and a very low n_s would have an impact on noise performance (due to the resulting high resistance), a careful design was made to achieve both high sensitivity and low noise operation. The entire linear Hall Effect integrated circuit was fabricated using the six steps illustrated in Figure 1.

The fabrication process was performed using traditional optical i-line lithography and metal lift-off. Hence, the device active layer or Mesa isolation was defined first by wet-etching using the non-selective etchant Orthophosphoric acid (H_3PO_4:H_2O:H_2O_2) with a ratio 3:1:50. Thereafter, the Ohmic contacts were formed by the thermal evaporation of AuGe, Ni, followed by Au, which were then annealed at 420 °C in a furnace, resulting in specific contact resistances (R_C) of $< 1.6 \times 10^{-5}$ Ω.mm^2. Ti/Au was then deposited using thermal evaporation onto the pre-defined gate and bond pad regions. A 200 nm Si_3N_4 dielectric layer was then deposited and vias opened using CF_4 gas. Finally, the bridge metals were deposited using the same process as the Gate and Bond pads.

III. Hall Effect Sensor Characterization

The design of the pHEMT structure can easily be adapted to form Hall plates. Using this pHEMT-like structure, two Greek cross Hall structures, denoted as P2A and P15A, using AlGaAs/InGaAs/GaAs materials and having resolutions of 1 μT at DC and 100 nT at higher frequencies have been reported previously [17]. The design of the XMBE303 Hall sensors relied on the same principles as the designs of the P2A and P15A sensors, however with slightly different epilayers to also optimise the characteristics of the depletion mode PHEMT transistors when used in the integrated high gain amplifier circuits. Figure 2 illustrates the top view of the Hall Greek cross sensor used in the final linear integrated circuit.

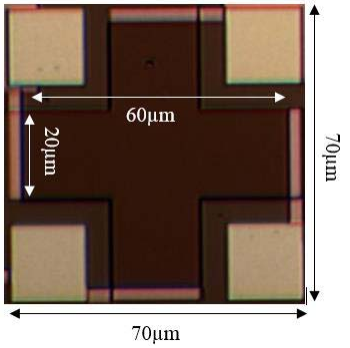

Fig. 2. Top view of the XMBE303 Greek cross Hall sensor.

TABLE II
XMBE303 Hall Sensor Characteristics

Parameters	XMBE303 Hall Sensor	Units
Dimension (L/W)	60/20	µm
Input resistance	1750	Ω
Output resistance	1750	Ω
Current sensitivity	0.4	mV/mA.mT
Operating temperature range	-180 to 200	°C
Linearity error (B = 0 to 50 mT)	0.05	%
Current sensitivity drift over temperature	-0.08	%/°C
Resistance drift over temperature	0.3	%/°C
Power consumption at V_{in} = 1 V	0.57	mW
Maximum DC offset at V_{in} = 1 V	0.35	mT

The fabricated device was fully symmetrical and thus input and output resistances were the same (∼1750 Ω). The fabricated sensor had an (L/W) ratio of 3 with L = 60 μm and a sensitivity of 0.4 mV/mA.mT and was capable of detecting magnetic fields as low as 10 nT (with amplification of 40,000 using off-chip components). The characteristics of the Hall sensors are shown in Table 2.

As shown in Figure 3, a temperature coefficient of the Hall voltage (T_C) of approximately −0.08 %/°C was achieved from −40 °C to approximately 200 °C. The Hall sensor was shown to have a maximum DC offset of 0.35 mT at 1 V of input bias (measurements were conducted on 50 sensors over 28 runs), a value that is at least 20 times smaller compared with silicon Hall plates. However, since the integrated circuit is used in AC applications, this offset can easily be removed from the output signal using capacitor filtering.

IV. Transistor Characterization and Modeling

To realise the integrated circuit, pseudomorphic High Electron Mobility Transistors (pHEMTs) using the same epitaxial layer profile as the Hall elements were fabricated and characterised. On Wafer DC and RF measurements were conducted

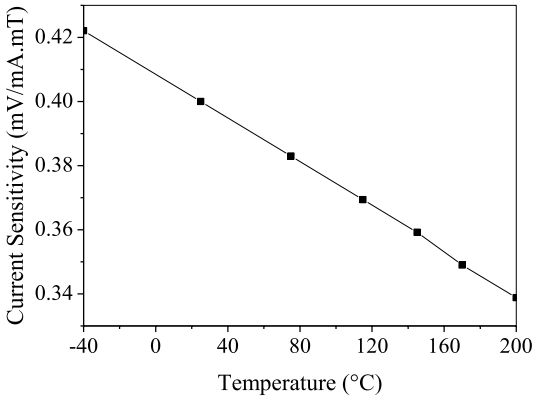

Fig. 3. Current sensitivity drift of XMBE303 Hall sensor over temperature from −40 °C to 200 °C.

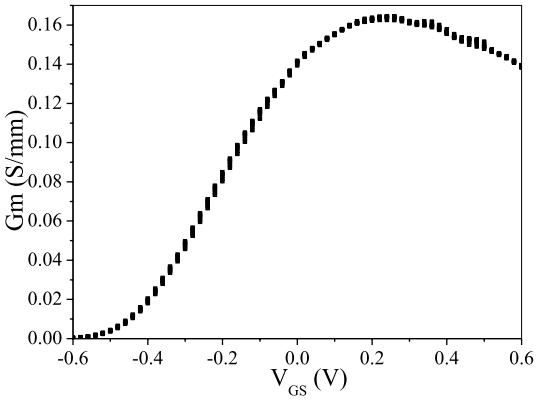

Fig. 4. Transconductance (Gm) of a 2 × 50 μm (2 finger 50 μm) width device at V_{DS} sweep from 1 V to 2 V (in 3 steps) and V_{GS} sweep from −0.6 V to 0.6 V.

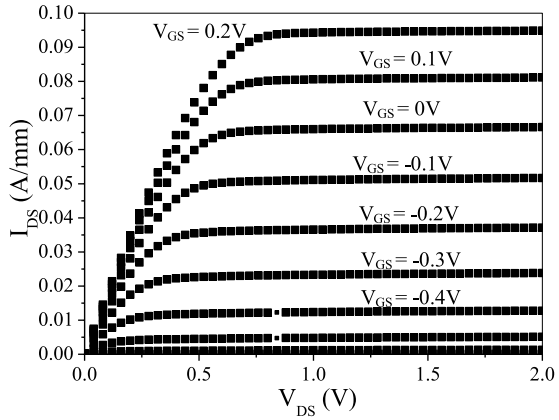

Fig. 5. DC I_{DS} versus V_{DS} characteristic of a 2 × 50 μm device where V_{GS} is swept from −0.8 V to 0.2 V in steps of 0.1 V.

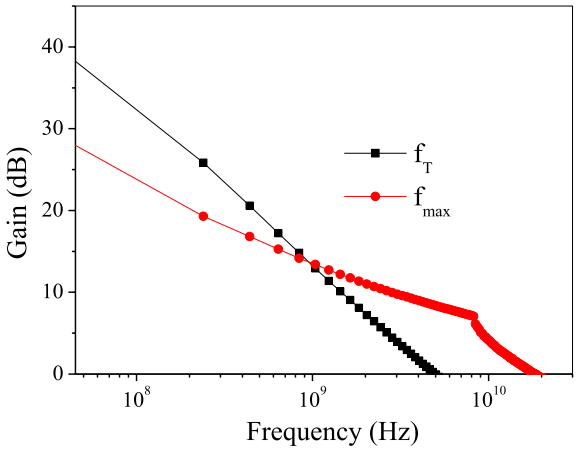

Fig. 6. Cut off frequency and maximum frequency at Gm maximum and V_{DS} = 1 V.

on several devices with 2 μm gate length and various gate widths (10 μm to 400 μm). The 2 μm gate length allowed a simple, very high yielding fabrication process. A turn on and breakdown voltage of 0.8 V and −21 V, respectively, at a gate current of ±100 μA/mm were achieved. The high breakdown is the result of the high band gap of the supply layer, which leads to a high schottky barrier. This characteristic is excellent for designing circuits with minimal protection. The threshold voltage was determined to be −0.4 V from an extrapolation of the square root of I_{DS} versus V_{GS} curve. This latter value is ideal for the design of integrated circuits as the threshold voltage is negative and close to zero, which eliminates the need for a negative rail in the circuit design. The normalised maximum transconductance was 162 mS/mm at a Drain-Source voltage of 1 V, as shown in Figure 4.

The high transconductance is useful in designing high gain amplifiers, and can specifically assist in achieving high overall sensitivities in the Hall integrated circuit. The maximum Drain-Source current corresponding to the maximum transconductance and Drain-source voltage of 1 V was as high as 95 mA/mm, as depicted in Figure 5.

The output conductance corresponding to the range of 1 V to 2 V Drain-Source voltage and 0.3 V Gate-Source voltage was only 0.4 mS/mm. A low output conductance is vital when pHEMTs are used in circuits as all the transistors operate in their saturation regions. Due to the extremely low output conductance, the overall intrinsic gain was as high as 405.

Microwave S-parameters were measured on an Anritsu 37369A network analyser using on-wafer probing over the frequency range of 40 MHz to 40 GHz. The current-gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) at the maximum transconductance and Drain-Source voltage of 1 V were 4.8 GHz and 18.2 GHz, respectively, (Figure 6). Note that these values are comparable to 0.5 μm gate length NMOS in Silicon.

High cut off and maximum frequencies would allow designing integrated circuits with ample bandwidths. This specifically aids in enhancing current commercial Hall linear IC technology whose frequency bandwidth are at most a few 10 kHz.

The transistor parameters were extracted from non-linear modelling in Agilent's ICCAP and Advanced Design System (ADS) software. This software includes the EEHEMT model for the HEMTs [18]. Figures 7 and 8 illustrate the excellent fit between the simulated and measured current-voltage (I-V) and RF characteristics of a single finger 50 μm pHEMT, respectively.

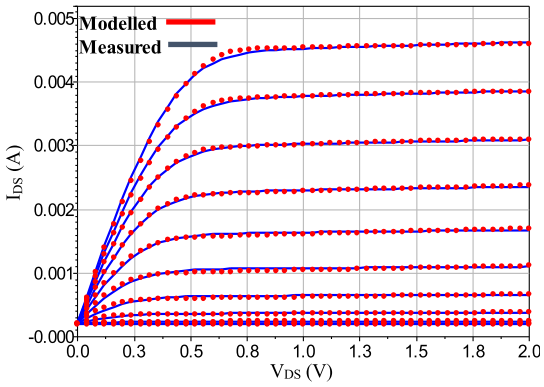

Fig. 7. DC modeling (IV curve) for a 2μm length, 1×50 μm width device as V_{GS} is swept from -0.8 V to 0.2 V.

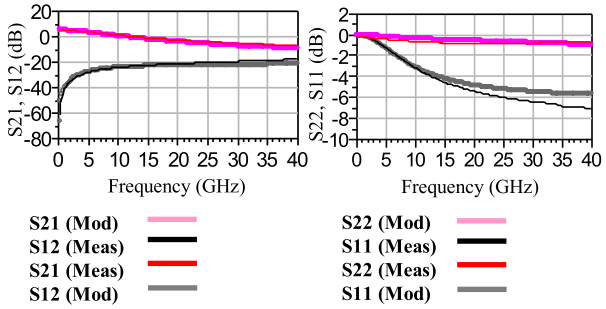

Fig. 8. RF modelling (S parameters) in the frequency range from 40 MHz to 40 GHz.

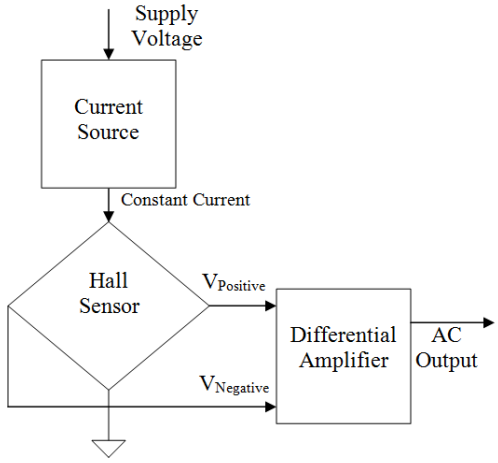

Fig. 9. The top level design of the AC linear Hall Effect integrated circuit.

V. AC Linear Hall Effect Integrated Circuit Design

The linear Hall IC design was divided into 3 sub-circuits comprising the Hall Effect sensor, a current source and a differential amplifier. The top-level configuration of this IC is illustrated in Figure 9. Each of these sub-circuits was designed and simulated individually, and they were then combined to form the complete GaAs-InGaAs-AlGaAs 2DEG linear Hall IC.

The current source circuit consisted of a single saturated pHEMT whose gate is connected to its source and two diodes

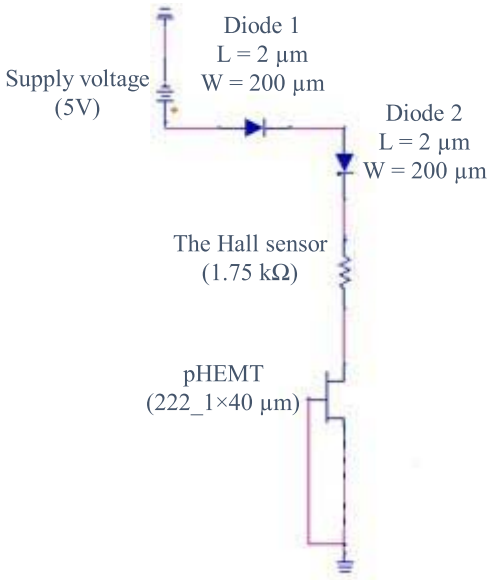

Fig. 10. Current source circuit configuration.

(pHEMTs consisting of one schottky and one ohmic terminal). A transistor with a gate width of 40 μm and two diodes with width of 200 μm provided the 1 mA constant current to the Hall sensor. Figure 10 illustrates the circuit layout of the current source circuit. A resistor value of 1.75 kΩ (R_{in} of the XMBE303 Hall sensor) was used in order to represent the XMBE303 Hall sensor in the simulation.

As discussed previously, the fabricated pHEMTs drain-source current has shown excellent stability for the drain-source voltage range of 1 V to 3 V since the pHEMT output conductance for this range is very low ($g_0 = 0.4$ mS/mm). For this reason, two diodes with width of 200 μm (2 μm gate length) were used to decrease the supply voltage of 5 V down to about $\sim$2.3 V. This would provide 0.7 V of margin to ensure that process variations during lithography have the least possible effect on the generated current by the current source circuit. Over the number of runs this circuit was fabricated and tested, it showed excellent stability and reproducibility, with variations less than $\pm 5\%$ from circuit to circuit and run to run.

An open-loop differential amplifier was designed to amplify the output of the Hall sensor, so that ultra-low magnetic fields could be easily detected. The aim was to achieve the maximum gain possible from single stage amplification so that the overall IC power consumption and size could be reduced. The following points were considered as the objectives when designing this circuit:

1. A circuit with a gain of at least 1000
2. Operating frequencies larger than 10 kHz (the limit of silicon commercial Hall ICs due to offset cancellation spinning technique)
3. Power consumption below 10 mW

Prior to the design of the differential amplifier circuit, there were two limitations (compared to CMOS technology) which had to be taken into account.

1. The major limitation in designing a differential amplifier using GaAs technology is the absence of

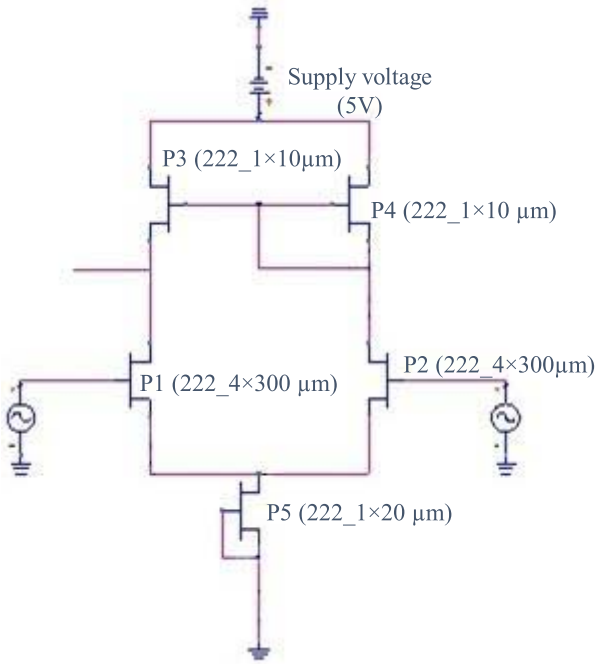

Fig. 11. The differential amplifier circuit configuration.

complementary devices. Although it is possible to produce p-channel GaAs transistors, and use them in the same manner as PMOS transistors, this is not very practical in GaAs. This is mainly because the hole mobility of GaAs is poor [19] and the resulting cut-off frequency would be lower than silicon devices.

2. The second limitation is the absence of negative rail in the design. This was mainly to reduce one pin from the final packaged IC to make it compliant with Hall IC practice. Taking into account the points above and as shown in Figure 11, the differential amplifier circuit consisted of a differential pair (P_1 and P_2), a saturated pair (P_3 and P_4) and a saturated (active load) transistor (P_5).

The amplifier's power consumption at 5 V of supply was 5.4 mW (1.08 mA × 5 V). In the final IC, the Hall sensor's outputs would be connected to the differential pair P_1 and P_2, with the four gate finger widths of 300 μm (1.2 mm width in total). The amplifier's output was taken from the drain of P_1. If there was no AC magnetic field applied to the sensor, the Hall sensor's outputs is a DC value (as the supplied current to the sensor is DC) and would equally be:

$$V^+ = V^- = (0.5 \times R_{in}) + V_{CS} \tag{1}$$

where V_{CS} is the voltage dropped across the transistor in the current source circuit. If an AC magnetic field was applied to the sensor, proportional to the strength of the magnetic field, an AC output would appear at the sensor's outputs. This signal would be amplified by the gain of the circuit and would appear at the amplifier's output. The gain of this circuit is determined by Equation 2 below.

$$A_V = \frac{Gm_1 \times R_O}{2} \tag{2}$$

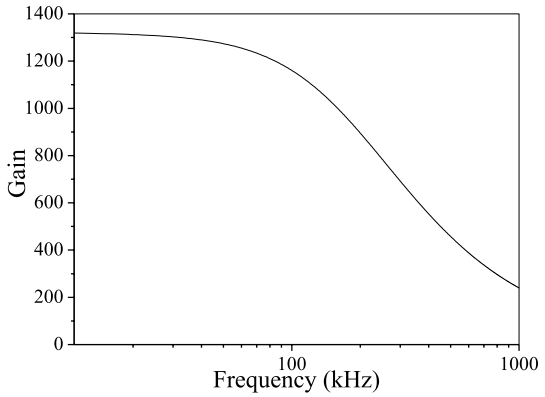

Fig. 12. Differential amplifier Bode plot (simulation).

Where, Gm_1 is the transconductance of P_1, R_O is the parallel drain-source resistance of P_1 and P_3 ($R_{DS1} \parallel R_{DS3}$). As shown above, the overall gain of the amplifier is directly proportional to the transconductance of P_1. For this reason transistors with large width ($4 \times 300\ \mu m = 1.2$ mm) were chosen for P_1 and P_2 in order to achieve a gain of over 1000. In addition, in order to achieve high R_O, devices with a single finger of width 10 μm were selected for P_3 and P_4.

This circuit was simulated in ADS and showed to have an AC gain of 1333 (62.5 dB) and a bandwidth of around 200 kHz. Figure 12 illustrates the Bode plot of the amplifier circuit obtained in simulation.

Note that this amplifier has a DC offset of 2.75 V as no negative rail has been used. This offset can easily be removed using an external capacitor.

VI. Fabrication of Linear Hall Effect Integrated Circuit

The fabricated IC had overall dimensions of 0.65 mm × 0.9 mm. The final processed IC is shown in Figure 13.

The overall integrated circuit's sensitivity was 533 mV/mT and was determined by the Hall Effect sensor's sensitivity (0.4 mV/mT biased at 1 mA) and the amplifier's gain of 1333. This is a factor of 10, 13 and 37 higher compared with the Allegro (A1324), Melexis (MLX90242) and Honeywell (SS39ET) [14]–[16] devices. In addition to providing very high sensitivity, this IC had a power consumption of only 10.4 mW. Despite being the most sensitive amongst all commercial silicon ICs investigated in this study, the power consumption of the Honeywell SS39ET IC is 30 mW (at 5 V supply), which is almost 3 times higher than the GaAs Hall IC reported here. The power consumption for the Allegro A1324 and Melexis MLX90242 ICs are 34.5 mW and 12.5 mW at 5 V supply, respectively. The reason for high power consumption of these silicon ICs is probably due to the use of complex circuitries for spinning current technique, circuit protection, signal buffering, offset and 1/f noise cancellation.

VII. Linear Hall Effect Integrated Circuit Testing and Characterization

In order to test the sensitivity of the IC, and especially its low field detectability, known small AC fields were generated using a Helmholtz coil. The Helmholtz coil consist of a pair

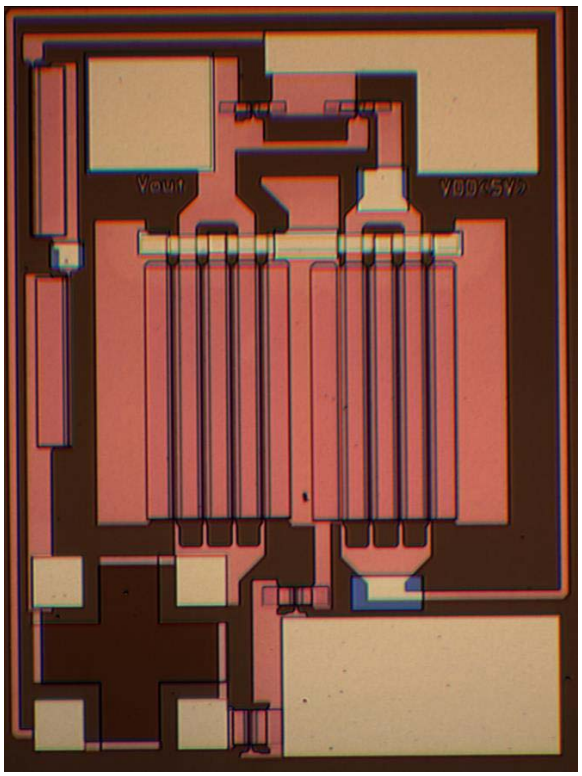

Fig. 13. Linear Hall integrated circuit layout.

of similar coils where the magnetic field is extremely uniform in the mid-plane between these two coils. The value of the generated field in a Helmholtz coil can be calculated as shown in Equation 3.

$$B = \frac{8\mu oNI}{\sqrt{125}R} \tag{3}$$

where N is the number of turns of each coil, I is the driving current in the coil, μ_o is the permeability of free space and R is the coil radius. In this work, a function generator was used to generate a constant AC current to a Helmholtz coil with 10 turns on each coil and 55 mm coil radius. From Equation 3, the magnetic field that is created in this coil is given by: $B = I \times 1.6 \times 10^{-7}$ T.

As the generated magnetic field can be accurately determined and the overall sensitivity of the circuit is known (0.4 × amplifier's gain (at a specific frequency) nV/nT), the expected output of the integrated circuit, at a specific field, can be calculated. Measurements were carried out at a magnetic field of 250 nT over the frequency range of 1 to 200 kHz. Figure 14 illustrates the measurement versus the expected (calculated) results. Note that in all the measurements performed here, an external capacitor was used to remove the IC's output DC offset.

As can be seen, the measured output from the IC closely followed the calculated results verifying the experimental setup. This verifies that the generated current to the Hall sensor and the obtained gain from the amplifier are close to what was expected and achieved in the simulation. The increase in the measured signal after ~100 kHz is due to the Faraday induced voltages picked up by the PCB in which the IC was mounted.

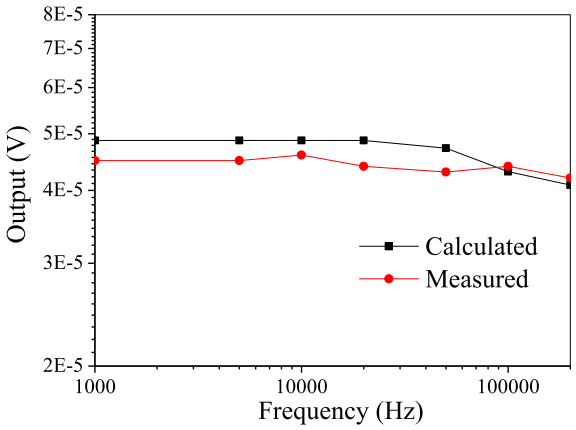

Fig. 14. Measured and calculated output at B = 250 nT.

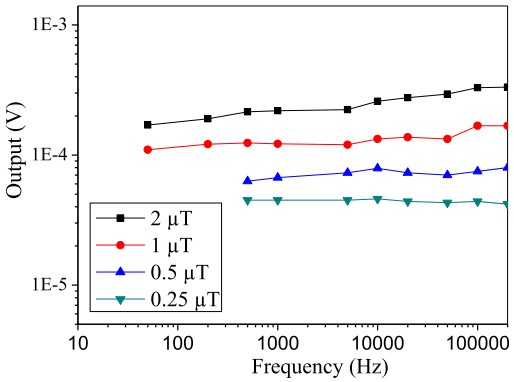

Fig. 15. Linear Hall IC Output at magnetic fields of 2 μT, 1 μT, 0.5 μT and 0.25 μT for the frequency range of 50 Hz to 200 kHz.

According to Faraday's law, induced voltage is proportional to the rate of change of flux lines cutting the conductor, so it increases at higher frequencies. The base PCB was designed with such layout to reduce this pick-up, however, it is very difficult to fully remove such pick-ups, especially at higher frequencies.

Further measurements were then performed on this IC at magnetic fields of 2 μT, 1 μT, 0.5 μT and 0.25 μT (until the noise floor level of the circuit was reached) for the frequency range from 50 Hz to 200 kHz. The results from these measurements are depicted in Figure 15. For magnetic fields less than 1 μT at frequencies below 500 Hz, the output could not be detected, due to the presence of 1/f noise.

The circuit was thus capable of detecting magnetic fields as low as 177 nT in the frequency range of 1 kHz to 200 kHz (at S/N = 2). This was determined in a measurement bandwidth of 10 Hz. Figure 16 shows the minimum detectable magnetic field at frequencies from 50 Hz to 200 kHz. The smallest detectable magnetic field is seen to increase at frequencies below 1 kHz due to 1/f noise and reaches 700 nT at 50 Hz.

Table 3 summarises the key properties of the linear Hall IC.

Figure 17 shows the results of field measurements on the commercial linear Hall ICs as compared to the GaAs Hall IC. All the measurements here were performed in a 10 Hz bandwidth. The performances at low frequencies become comparable in part due to the on-board noise cancellation circuitry

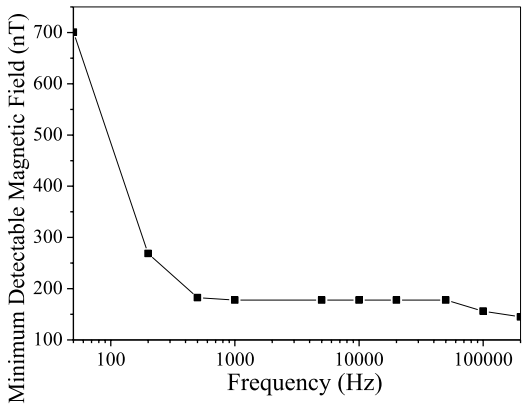

Fig. 16. Minimum detectable field by the Linear Hall Effect IC in the frequency range of 50 Hz to 200 kHz (at S/N = 2) and 10 Hz measurement bandwidth.

TABLE III
SUMMARY OF THE GaAs-InGaAs-AlGaAs LINEAR HALL IC CHARACTERISTICS

GaAs-InGaAs-AlGaAs 2DEG linear Hall Effect IC Characteristics	
Circuit sensitivity	533 μV/μT
Supply bias current at 5 V	2.08 mA
Minimum detectable field (10 Hz bandwidth)	177 nT
Maximum field at 5 V supply	~ 9 mT
Frequency range of operation	500 Hz to 200 kHz
Dimension	0.65 mm × 0.9 mm

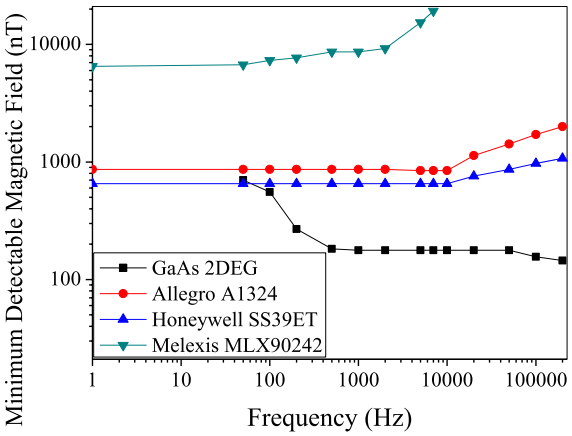

Fig. 17. Comparison of the GaAs 2DEG linear Hall IC with linear Hall ICs made by Allegro, Honeywell and Melexis in terms of Minimum detectable field as a function of frequency, at S/N of 2 in measurement bandwidth of 10 Hz.

that the silicon based sensors have in comparison to the InGaAs-GaAs-AlGaAs IC fabricated here. This technique was not employed as this would have made the circuitry complex and more power hungry. However, considerable improvements are expected if such circuit techniques were used. At high frequencies, the superiority of the III-V based circuit is seen in both resolution and bandwidth.

The minimum detectability in Figure 17 is defined as the point where the amplitude of the signal is twice the noise (S/N = 2). The Honeywell SS39ET IC showed a lowest minimum field detectability at 652 nT. This detectability, in comparison with the GaAs IC, is higher by a factor of four. Furthermore, the high frequency performance of these silicon

TABLE IV
LINEAR SILICON HALL EFFECT ICs (HONEYWELL, ALLEGRO AND MELEXIS) AND COMPARISON WITH THE GaAs 2DEG HALL IC

Supplier (Product)	Min Detectable Field	Operating Frequency Range	Power Consumption at 5 V Supply
Honeywell (SS39ET)	652 nT	DC to 10 kHz	30 mW
Allegro (A1324)	864 nT	DC to 10 kHz	34.5 mW
Melexis (MLX90242)	6500 nT	DC to 2 kHz	12.5 mW
GaAs 2DEG IC	177 nT	500 Hz to 200 kHz	10.4 mW

ICs are limited to 10 kHz (in the case of Honeywell and Allegro), whereas the reported GaAs 2DEG IC is capable of operating up to 200 kHz. The limitation of the operating frequency on these commercial ICs is largely a result of the on-board current spinning technique used to reduce the Hall element offset and 1/f noise. Such a technique limits the operating frequency range typically to 10 kHz because of the use of typical 100 kHz spinning frequency [2], [20], [21]. In addition, another limitation for Silicon Hall bandwidth is the output stage, which is required to work on 100 nF filter caps thereby limiting the maximum frequency. One also has to note that the advantage of high frequency operation can sometime be lost by eddy currents in the lead frame of conventional low cost packages.

Table 4 compares the performances of the various Hall Effect linear ICs.

The GaAs 2DEG Hall IC is not only capable of detecting lower magnetic fields but also enhances the current technology in terms of operating frequency range and power consumption.

Whereas integrated Hall sensors based on ion implanted GaAs MESFET were reported earlier [13], the 2DEG IC demonstrated here with their more complex epitaxial structure permit much higher mobilities than ion implanted GaAs (because of the pseudomorphic InGaAs channel layer) leading to higher sensitivities and lower offsets. Furthermore, the large band gap barrier material (AlGaAs) helps in ensuring operations at higher temperatures too. The pHEMT transistors based on the structures also lead to very high gain transistors because of the much reduced output conductance compared with the ion implanted GaAs MESFETS [13]. The combination of all these properties resulted in a Hall IC that looks promising for a range of applications.

However, in order to have a product which is ready to enter the market, the IC will still need to be fully characterised in terms of thermal stability, operating temperature range and linearity.

VIII. CONCLUSION

In this work, the performance of a new GaAs-InGaAs-AlGaAs 2DEG fully integrated linear Hall Effect integrated circuit was presented. This IC provides a sensitivity of 533 μV/μT which is an order of magnitude larger than that of the most sensitive available linear Hall IC, Allegro A1324 (S = 50 mV/mT). The GaAs IC is capable of detecting

AC magnetic fields as low as 177 nT (in a 10 Hz bandwidth), which is almost a factor of 4 lower than the best commercially available Si Hall IC. Furthermore, the GaAs 2DEG IC has operating bandwidths greater than 200 kHz compared with bandwidths around 10 kHz for the commercially available silicon ICs. The GaAs IC has a total power consumption of 10.4 mW (at 5 V), which is less than silicon ICs [14]–[16]. The GaAs-InGaAs-AlGaAs 2DEG linear Hall IC could therefore be employed in applications such as Non Destructive Testing (NDT), linear and rotary position sensing, contactless current sensing, detection of overcurrent from power lines and for use in harsh environments.

REFERENCES

[1] G. Bosch, "A Hall device in an integrated circuit," *Solid-State Electron.*, vol. 11, no. 7, pp. 712–714, 1968.

[2] S. Bellekom, "CMOS versus bipolar Hall plates regarding offset correction," *Sens. Actuators A, Phys.*, vol. 76, nos. 1–3, pp. 178–182, 1999.

[3] R. S. Popovic, Z. Randjelovic, and D. Manic, "Integrated Hall-effect magnetic sensors," *Sens. Actuators A, Phys.*, vol. 91, nos. 1–2, pp. 46–50, 2001.

[4] Z. B. Randjelovic, M. Kayal, R. Popovic, and H. Blanchard, "Highly sensitive Hall magnetic sensor microsystem in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 151–158, Feb. 2002.

[5] H. Blanchard, M. F. De, B. J. Hu, and R. S. Popovic, "Highly sensitive Hall sensor in CMOS technology," *Sens. Actuators A, Phys.*, vol. 82, nos. 1–3, pp. 144–148, 2000.

[6] V. Mosser *et al.*, "High sensitivity Hall sensors with low thermal drift using AlGaAs/InGaAs/GaAs heterostructures," *Sens. Actuators A, Phys.*, vol. 43, nos. 1–3, pp. 135–140, 1994.

[7] V. Mosser *et al.*, "High-performance Hall sensors based on III–V heterostructures," *Sens. Actuators A, Phys.*, vol. 42, nos. 1–3, pp. 450–454, 1994.

[8] J.-S. Lee, K.-H. Ahn, Y.-H. Jeong, and D. M. Kim, "Highly sensitive $Al_{0.25}Ga_{0.75}As/In_{0.25}Ga_{0.75}As/GaAs$ quantum-well Hall devices with Si-delta-doped GaAs layer grown by LP-MOCVD," *Sens. Actuators A, Phys.*, vol. 57, no. 3, pp. 183–185, 1996.

[9] J.-S. Lee, K.-H. Ahn, Y.-H. Jeong, and D. M. Kim, "Quantum-well Hall devices in Si-delta-doped $Al_{0.25}Ga_{0.75}As/GaAs$ and pseudomorphic $Al_{0.25}$ $Ga_{0.75}As/In_{0.25}Ga_{0.75}As/GaAs$ heterostructures grown by LP-MOCVD: Performance comparisons," *IEEE Trans. Electron Devices*, vol. 43, no. 10, pp. 1665–1670, Oct. 1996.

[10] V. Mosser *et al.*, "Low-cost 2DEG magnetic sensor with meteorological performances for magnetic field and current sensing," in *Proc. Int. Conf. Solid-State Sens. Actuators*, Chicago, IL, USA, 1997, pp. 401–404.

[11] T. R. Lepkowski *et al.*, "A GaAs integrated Hall sensor/amplifier," *IEEE Electron. Device Lett.*, vol. EDL-7, no. 4, pp. 222–224, Apr. 1986.

[12] K. Fricke, G. Schweeger, J. Wurfl, and H. L. Hartnagel, "Integrated circuits on GaAs for the temperature range from room temperature up to 300 °C," in *Proc. Gallium Arsenide Appl. Symp.*, Apr. 1990, pp. 284–289.

[13] K. Itakura, D. Ueda, M. Hagio, and M. Kazumura, "GaAs integrated Hall sensor with temperature-stabilised characteristics up to 300 °C," *Electron. Lett.*, vol. 25, no. 22, pp. 1493–1495, Oct. 1989.

[14] *SS39ET/SS49E/SS59ET Linear Hall-Effect Sensor IC*, Honeywell, Morristown, NJ, USA, Mar. 2013.

[15] *A1324, A1325, and A1326 Low Noise, Linear Hall Effect Sensor ICs with Analog Output*, Allegro, Poznań, Poland, Sep. 2013.

[16] *MLX90242 Linear Hall Effect Sensor*, Melexis, Bevaix, Switzerland, Feb. 2012.

[17] N. Haned and M. Missous, "Nano-tesla magnetic field magnetometry using an InGaAs–AlGaAs–GaAs 2DEG Hall sensor," *Sens. Actuators A, Phys.*, vol. 102, no. 3, pp. 216–222, 2003.

[18] Agilent's EEHEMT. *HEMT Modeling*. [Online]. Available: http://edocs.soco.agilent.com/display/iccap2009U1/Using+the+EEFET3-EEHEMT1+Example+Model+Files, accessed Nov. 4, 2013.

[19] R. Zuleeg, J. K. Notthoff, and G. L. Troeger, "Double-implanted GaAs complementary JFET's," *IEEE Electron Device Lett.*, vol. EDL-5, no. 1, pp. 21–23, Jan. 1984.

[20] R. Steiner, C. Maier, A. Hàberli, F.-P. Steiner, and H. Baltes, "Offset reduction in Hall devices by continuous spinning current method," *Sens. Actuators A, Phys.*, vol. 66, nos. 1–3, pp. 167–172, 1998.

[21] S. Bellekom and P. M. Sarro, "Offset reduction of Hall plates in three different crystal planes," *Sens. Actuators A, Phys.*, vol. 66, nos. 1–3, pp. 23–28, 1998.

Mohammadreza Sadeghi received the B.Eng. (Hons.) degree in electronics and computer engineering from the University of Bolton, Bolton, U.K., in 2009. He is currently pursuing the Ph.D. degree at the School of Electrical and Electronic Engineering, University of Manchester, Manchester, U.K., where he is working on advanced nanotesla III–V 2DEG quantum well Hall effect integrated circuits. His research interests include pseudomorphic high-electron mobility transistors, analogue circuits, and Hall effect sensors.

James Sexton received the bachelor's degree in electronic engineering from the University of Manchester Institute of Science and Technology, Manchester, U.K., in 2001, and the Ph.D. degree from the University of Manchester (UOM), Manchester, in 2005, with a focus on InP-based single and double heterojunction bipolar transistors for high-speed low-power digital applications. He became a Research Associate at UOM developing digital front-end technology for the next-generation radio telescope square kilometre array. In 2009, his research was directed on transistor development specifically designed for the Electromagnetic Remote Sensing Defence Technology Centre. Since 2010, he has been the Experimental Officer managing the III–V Compound Semiconductor Fabrication Facility at UOM. His current research interests include magnetic Hall effect sensors, resonant tunnelling diodes, asymmetric spacer-layer tunnel diodes, and low-noise pseudomorphic high-electron mobility transistors.

Chen-Wei Liang received the bachelor's degree in applied physics and chemistry from the Department of Natural Science, Taipei Municipal University of Education, Taipei, Taiwan, in 2012. He was with National Marines for the obligations of a citizen in Taiwan in 2012. He received the M.Phil. degree in electrical and electronic engineering from the University of Manchester (UOM), Manchester, U.K., in 2014, with a focus on high-frequency magnetometers and linear array magnetometers using ultrasensitive quantum well Hall effect sensors, where he is currently pursuing the Ph.D. degree, investigating Hall effect sensor noise and minimum B-field measurement and developing linear Hall array magnetometer. His current research interests include 2D Hall effect sensors, offset cancellation techniques, circuit design of Hall effect linear array magnetometer, microcontrolled Hall array magnetometer architecture, and low-noise pseudomorphic high-electron mobility transistors.

Mohamed Missous (SM'05) is a Fellow of the Royal Academy of Engineering, the Institute of Physics, the Institution of Engineering and Technology, and a Chartered Engineer, U.K. He is currently a Professor of Semiconductor Materials and Devices with the School of Electrical and Electronic Engineering, University of Manchester, Manchester, U.K. His research activities are centred on the growth of complex multilayer semiconductor films by the technique of molecular beam epitaxy (MBE). He has established a large MBE and Compound Semiconductor Laboratory for materials growth, assessment equipment, compound semiconductor processing facility, and device testing. Over the years, he has concentrated, with considerable success, on establishing practical approaches and techniques required to meet stringent doping and thickness control, to submonolayer accuracy, for a variety of advanced quantum devices, from room temperature operating midinfrared quantum-well infrared photodetectors, nanotesla magnetic imaging using ultrasensitive 2DEG for nondestructive testing, 77-GHz car radars to terahertz materials for 1.55-μm imaging. He has also been involved in developing advanced low-noise amplifiers and high-speed ADCs for the Square Kilometre Array project. His involvement in the above research topics has led to the publication of over 200 papers in the open international literature.