Planar On-Silicon Inductor Design for Electromagnetic Tracking

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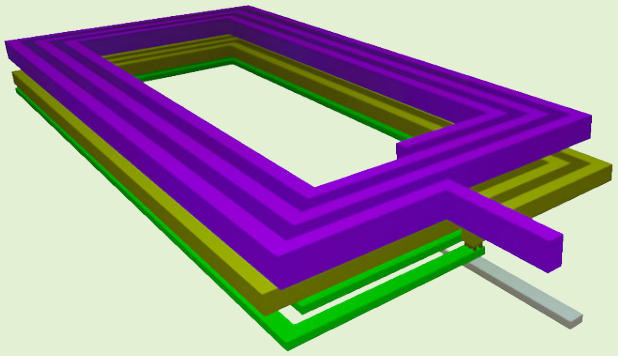
***Abstract*—In this article, a planar on-silicon inductor design for electromagnetic tracking (EMT) is presented. The design process has been demonstrated for a planar sensing coil in a 65-nm on-silicon process. The designed multilayer planar inductor configuration achieves SNR of 23.6 dB and sensitivity of 202 μV/T/Hz. The designed inductor satisfies system requirements for clinical use in EMT applications. The current design has been verified on the Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm process and exhibits a close correlation with simulation results. Measured SNR of 22.1 dB and sensitivity of 198 μV/T/Hz at a frequency of 20 kHz and magnetic flux density of 150 nT is achieved. An improved lumped element model to account for multilayer planar inductor designs is also proposed.**



***Index Terms*— CMOS, electromagnetic sensing, electromagnetic tracking (EMT), inductor, parameterized cell (PCELL), SKILL programming language, virtual bronchoscopy.**

I. Introduction

ELECTROMAGNETIC tracking (EMT) is a critical technology for tracking and navigation in image-guided interventions, when there is no line of sight to the target [1]. Clinical applications which currently exploit EMT for virtual navigation include bronchoscopy [2], [3], neurosurgery, and ear, nose, and throat surgery [4], [5]. In general, an EMT system relies on two main components: a field generator, which generates a spatially dependent magnetic field, and a magnetic sensor, which, by field measurement, can determine its relative position and orientation with respect to the field generator. One of the two components is fixed, while the other is tracked. Prior work [2] described the open-hardware EMT system called Anser EMT which allows for virtual navigation without using a real-time X-ray. This is possible by combining a preoperative CT scan with the EMT data. One clinical example of EMT is airway navigation [6]. When the diameter of the bronchoscope exceeds the diameter of the airways, navigation can be continued with EMT, where tracked medical instruments are advanced further into the lung under virtual navigation. The basic overview of this system is the basis of most commercial EMT systems as shown in Fig. 1.

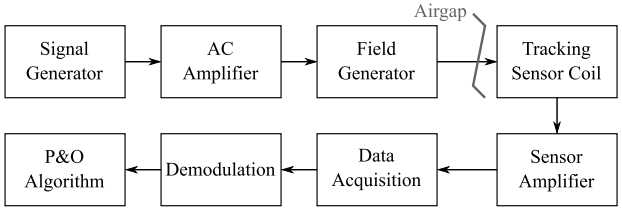


Fig. 1. Block diagram of the Anser EMT system.

A signal generator circuit provides a reference sine wave for each emitter coil channel. The signal is amplified and transmitted through the field generator coil array on a printed circuit board (PCB). A tracking sensor coil produces an induced alternating voltage due to the field generator. The sensed signal is amplified and sampled. The resulting samples are demodulated and processed through the position and

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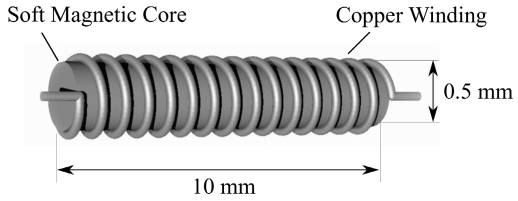

Fig. 2. Typical electromagnetic inductive sensor.

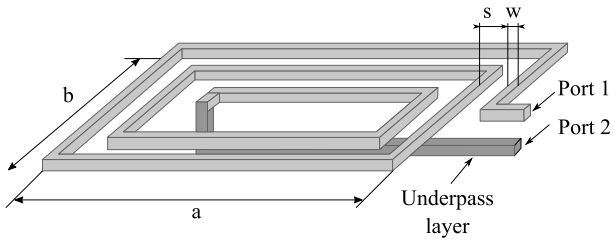

Fig. 3. Basic planar inductor structure.

orientation algorithm to yield a position and orientation vector for the tracking coil [2], [7]. The dimensions of existing discrete inductive sensor coils place a constraint on the mechanical design of the instrument and the spatial resolution of the sensor. The instrument must be typically rigid (nonflexible) for 10 mm and the sensor coil should consist of several hundred turns to achieve the required sensitivity (see Fig. 2). Otherwise, there is a risk of sensor lead breakage due to the instrument bending [8].

Moreover, the induced voltage from the sensor transmitted through the long cable introduces additional noise and decreases the accuracy of the system. These shortcomings with existing discrete inductive coil-based sensors make an integrated on-silicon solution very attractive. While this article specifically describes the optimization of the magnetic sensor coil, the overall goal of this work is to implement the tracking sensor coil, sensor amplifier, filter, and ADC on a single die [9]. This solution provides the following benefits.

1) Significant physical constraint reduction (decreasing sensor size from 5.5 × 0.5 to 1.5 × 0.5 mm).
2) Reduced sensor noise and losses in the cable resulting in accuracy improvement due to the single-die implementation.
3) Accuracy improvement, as the magnetic flux density point approximation is better achieved with a small die than with a 10-mm long coil.

II. Planar Inductor Basics

A. Basic Planar Inductor Structure

The planar inductor is a two-port device in the shape of a rectangular spiral that winds from the edge to the center and passes outside through the underpass layer, as depicted in Fig. 3. The main geometric parameters of the inductor indicated in Fig. 3 are as follows.

1) Number of turns N.
2) Width of trace w.
3) Spacing between traces s.
4) Outer dimensions of the coil (width a and length b).

In the present application, the planar inductor is an inductive sensor of the electromagnetic field that uses the principle of electromagnetic induction. According to Faraday's law of induction, a voltage is induced across an inductor when the magnetic field linking it changes. The temporal variations of the magnetic flux $\Phi(t)$ through the N turn inductor will induce a voltage which follows

$$e(t) = -N\frac{d\Phi(t)}{dt} \tag{1}$$

where $\Phi = \oint_s \overline{B} \cdot d\overline{S}$ is the magnetic field B linked by one turn, assuming they all have the same area S hereby

$$e(t) = -N\frac{d}{dt}\oint_s \overline{B} \cdot d\overline{S}. \tag{2}$$

The surface integral can be replaced by the discrete term summation for numerical evaluation

$$e(t) = -\frac{d}{dt}\sum_{i=1}^{N} B \cdot A_i \tag{3}$$

where N is the number of turns, A_i is the area of the ith turn, and B is the flux density at the center of the coil. For the sensors that are small relative to the spatial variation of the magnetic flux density, the variation in flux density across the sensor cross section is usually linear, so (3) may be simplified

$$e(t) = -\frac{dB(x, y, z, t)}{dt}\sum_{i=1}^{N} A_i. \tag{4}$$

Assume the magnetic field detected by the sensor is sinusoidal (as is the case for the Anser EMT system) with amplitude B_0

$$B(x, y, z, t) = B_0(x, y, z)\sin(\omega t) \tag{5}$$

where $\omega = 2\pi f_0$ is the received field angular frequency in radians per second. Then (4) can be represented as

$$e(t) = -\omega B_0(x, y, z)\cos(\omega t)\sum_{i=1}^{N} A_i. \tag{6}$$

The resulting magnitude of the induced voltage V_s for the nominal magnetic flux B_0 may be made explicit

$$V_s = 2\pi f_0 B_0 \sum_{i=1}^{N} A_i = k_s B_0 f_0 \tag{7}$$

where f_0 is the received signal frequency in Hz and k_s is the sensitivity of the sensor in volts per tesla per hertz (V/T/Hz)

$$k_s = 2\pi \sum_{i=1}^{N} A_i. \tag{8}$$

Considering input signal to be sinusoidal, the root-mean-square (rms) value of the signal is

$$\sqrt{\overline{V_s^2}} = \frac{V_s}{\sqrt{2}} = \frac{k_s B_0 f_0}{\sqrt{2}}. \tag{9}$$

Since the inductor is not ideal, the performance of the coil will be limited by the thermal noise contributed by

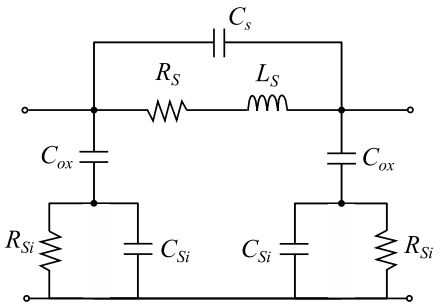

Fig. 4. Lumped physical model of a spiral inductor.

the parasitic resistance of the coil trace R_s. According to the Johnson–Nyquist formula [10], the mean-square noise voltage for a given bandwidth Δf of the inductor can be expressed as

$$\overline{V_n{}^2} = S_n(f)\Delta f = 4k_B T R_s \Delta f \tag{10}$$

where Δf is the sampling bandwidth in Hz, $S_n(f)$ is the noise voltage spectral density, k_B is the Boltzmann's constant, and T is the absolute temperature in K. Thus, the signal-to-noise ratio (SNR) of the inductor in is given by

$$\text{SNR} = \frac{\sqrt{\overline{V_s{}^2}}}{\sqrt{\overline{V_n{}^2}}} = \frac{k_s B_0 f_0}{\sqrt{8k_B T R_s \Delta f}}. \tag{11}$$

In standard applications, Q-factor is a very important characteristic of the inductor because it reflects the resonating ability of the inductor. In the EM-sensing application, an inductor is operating at very low frequencies (10–100 kHz) and captures the EM field by Faraday's law of electromagnetic induction and does not employ resonance. Therefore, Q-factor of the inductor is not considered in this work.

B. Lumped Physical Model of a Planar Inductor

A planar inductor is a complex structure with multiple physical parameters distributed over the device. However, a planar inductor can be replaced by the equivalent lumped model, such as that proposed in [12] and shown in Fig. 4.

This model requires the value of the resistance of the trace R_s, the resistance of the substrate R_{Si}, inductance L_s, underpass capacitance C_s, oxide capacitance C_{ox}, and substrate capacitance C_{Si}. For a rectangular planar coil inductance (in μH) can be calculated by the formula [13]

$$L_s = k_1 A_0 (A_1 - A_2 - A_3) + k_3 A_0 \left(2\frac{g}{s_1+s_2} - 0.5\right) + k_4 \frac{t+w}{s_1+s_2}\Bigg] \tag{12}$$

$$A_0 = (s_1+s_2)N^2 \tag{13}$$

$$A_1 = \log_{10}\frac{2s_1 s_2}{k_2(t+w)} \tag{14}$$

$$A_2 = \frac{s_2}{s_1+s_2}\log_{10}\left(\frac{s_1+g}{k_2}\right) \tag{15}$$

$$A_3 = \frac{s_2}{s_1+s_2}\log_{10}\left(\frac{s_2+g}{k_2}\right) \tag{16}$$

$$s_1 = a - Nw - (N-1)s \tag{17}$$

$$s_2 = b - Nw - (N-1)s \tag{18}$$

$$g = \sqrt{s_1^2 + s_2^2} \tag{19}$$

where s_1 and s_2 are the geometric parameters of the coil in μm, a and b are the width and length of the coil, respectively, in μm, w is the width of the trace in μm, s is the spacing between traces in μm, N is the number of turns, g is the average diagonal of the coil, and t is the thickness of the trace in μm (see Fig. 3). Coefficient values are $k_1 = 9.21 \cdot 10^{-7}$, $k_2 = 2.54 \cdot 10^4$, $k_3 = 0.01016$, and $k_4 = 0.447$ [13]. The resistance of the coil can be calculated from the sheet resistance of the metal

$$R_s = R_{\text{sheet}}\frac{l}{w} \tag{20}$$

where R_{sheet} is the on-silicon sheet resistance of the metal in ohm per square ($\Omega/\square$), and l and w are the length and width of the trace in μm, respectively. Oxide and substrate capacitances can be calculated from well-known formulae, where ϵ_{ox} is the absolute permittivity of the oxide, t_{ox} is the oxide thickness, and C_{sub} is the substrate capacitance per square unit

$$C_{\text{ox}} = \frac{1}{2} l w \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} \tag{21}$$

$$C_{\text{Si}} = \frac{1}{2} l w C_{\text{sub}}. \tag{22}$$

The series feedforward capacitance C_s which accounts for the capacitance due to the overlap between the inductor spiral and the underpass layer, is given by

$$C_s = \frac{1}{2}\frac{w_{\text{up}} w N \epsilon_{\text{ox}}}{t_{\text{ox}}} \tag{23}$$

where w_{up} is the width of the underpass layer in μm and t_{ox} is the oxide thickness between the inductor spiral and underpass layer in μm. As follows from [14], the combined impedance of C_{ox}, C_{Si}, and R_{Si} can be combined in C_p and R_p

$$R_p = \frac{1}{\omega^2 C_{\text{ox}}^2 R_{\text{Si}}} + \frac{R_{\text{Si}}(C_{\text{ox}}+C_{\text{Si}})^2}{C_{\text{ox}}^2} \tag{24}$$

$$C_p = C_{\text{ox}}\frac{1+\omega^2(C_{\text{ox}}+C_{\text{Si}})C_{\text{Si}}R_{\text{Si}}^2}{1+\omega^2(C_{\text{ox}}+C_{\text{Si}})^2 R_{\text{Si}}^2} \tag{25}$$

$$R_{\text{Si}} = \frac{t_{\text{sub}}}{0.5\left(l + \frac{D_{\text{out}}-D_{\text{in}}}{2}\right) w G_{\text{sub}}} \tag{26}$$

where $G_{\text{sub}} = 1/R_{\text{sub}}$ is the conductivity of the silicon substrate. This capacitance is in parallel with the feedforward capacitance C_s. The total equivalent capacitance of the inductor can thus be calculated as

$$C_{\text{tot}} = C_p + C_s. \tag{27}$$

The given formulae allow us to simplify the equivalent model of the inductor as shown in Fig. 5 [14].

III. Inductor Optimization

On-chip magnetic sensor design requires a particular optimization approach for coil design which looks to optimize SNR and differs significantly from typical power applications, where inductance or power dissipation are the key performance

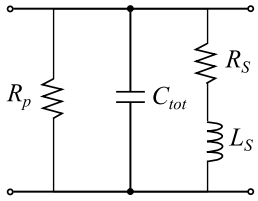

Fig. 5. Simplified lumped physical model of a planar inductor at low frequencies.

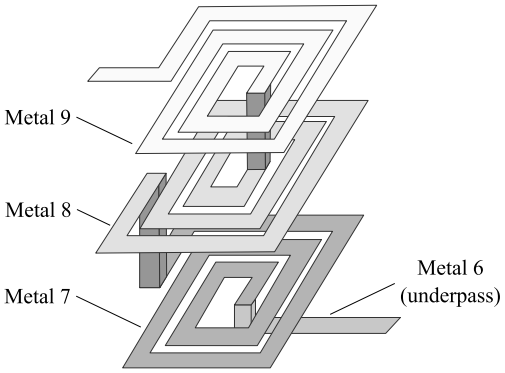

Fig. 6. Multilayer stacked inductor structure [15].

indicators [11]. In this work, by considering amplifier gain in conjunction with the sensitivity of commercially available sensors [8], a target SNR can be identified. As follows from Section II, the performance of the sensor is a tradeoff between two parameters: sensitivity and noise. The SNR combines both parameters and is an important figure of merit for this work. Typical values for the sensitivities of commercial sensors, such as the Aurora discrete coil sensors (Northern Digital Inc., Waterloo, ON, Canada) are 0.1–0.2 V/T/Hz [8]. Since our solution contains a built-in amplifier, this sensitivity specification can be achieved by amplifier gain. Thus, during the optimization process, we seek the best SNR considering the sensitivity specifications of existing discrete coil solutions.

A. Sensitivity Improvement Techniques

One of the most popular techniques for improving the sensitivity of a planar coil is a multilayer stacked design (see Fig. 6).

This method allows increasing flux linkage by increasing the effective cross-sectional area without increasing the area of the inductor on a die [15], [16]. Upper metal layers (which are intended for power supply and top-level routing) in CMOS technology have less resistance than lower layers. Thus, using lower metal layers may lead to a decrease in SNR. Another technique, a tapering design, described in [17], is shown in Fig. 7.

In the tapering design technique, width/spacing gradually increases/decreases while the trace traverses from the edge to the center of the coil. This allows for an increase in the number of turns and sensitivity of the coil according to (8) without a significant increase in the resistance.

B. MATLAB Optimization

Numerical optimization of the sensitivity techniques discussed in Section III-A was undertaken in MATLAB

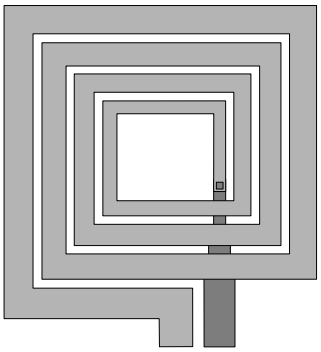

Fig. 7. Inductor design with tapering [18].

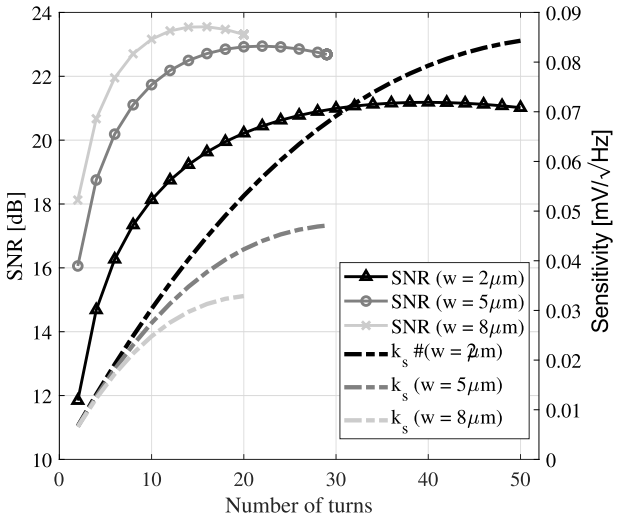

Fig. 8. Single-layer inductor optimization for M9 on Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm technology.

(The Mathworks, Natick, MA, USA). As SNR is the figure of merit of our design, Fig. 8 represents the optimization process for the SNR of the M9 ultrathick metal coil 450 × 1200-μm size for increasing numbers of turns.

Spacing between the turns is minimized (2 μm). Solid lines represent SNR and dashed lines represent sensitivity for each width of the trace. Considering achievable amplifier gain of 60 dB, once design optimization is complete, a target ON-chip inductor sensitivity of 0.06 mV/T/Hz was determined to achieve comparable accuracy to existing discrete sensor coils. An optimal configuration that meets this sensitivity requirement with 21.2-dB SNR can be achieved with 40 turns, 2-μm width of trace, and 2-μm spacing.

Fig. 9 represents the effect of tapering for different initial widths of the trace and tapering coefficient k_w defined as follows:

$$k_w = \frac{w_{i+1}}{w_i} \tag{28}$$

where w_i is the width of the ith turn in μm. From Fig. 9, we can observe that reducing the width of the trace does not give a significant increase in sensitivity, but negatively affects resistance, which leads to decreasing SNR. Tapering was not pursued further in this application.

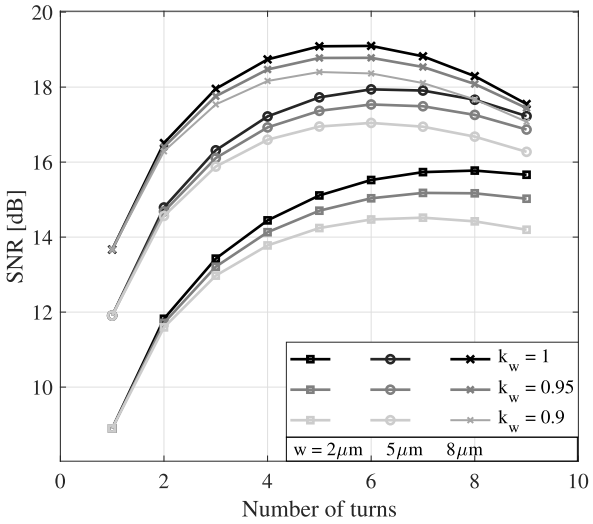

Fig. 9. Single-layer inductor design configurations for M9 with tapering design.

TABLE I
OPTIMAL INDUCTOR CONFIGURATIONS FOR TSMC 65-nm PROCESS

Coil geometry	Optimal Inductor Configurations				
	Number of turns	Width, μm	Spacing, μm	SNR[a], dB	Sensitivity, $\mu V/T/Hz$
M9	38	2	2	21.1	77
M9/M8	38/28	2/5	2/0.4	22.2	133
M10/M9/M8	15/38/28	7/2/5	3/2/0.4	23.6	202.31

[a] At f=20kHz and B=150nT

Based on the design procedure mentioned above, three inductor configurations have been obtained. The optimization has been performed based on the magnetic flux density of 150 nT and operating frequency 20 kHz to match the Anser EMT system requirements [2]. Optimized inductor configurations are shown in Table I.

It can be seen that the best SNR and sensitivity can be achieved by the three-layer stacked inductor implementation. This configuration has been selected as a final solution for our design.

IV. INDUCTOR PCELL DESIGN

A. PCELL Design in Cadence Virtuoso

Following the preliminary numerical analysis described in Section III-B, the planar inductor was specified in the Cadence[1] (Cadence Design Systems, Inc., San Jose, CA, USA) environment. A parameterized cell, or PCELL, is a programmable design entity that allows users to create a parametric instance in the integrated circuits (IC) design environment each time it is placed. PCELLs provide the following advantages.

1) Speed up layout data entry by eliminating the need to create duplicate versions of the same functional part.
2) Eliminate errors that can result in maintaining multiple versions of the same cell.
3) Manufacturing process independence.

[1]Registered trademark.

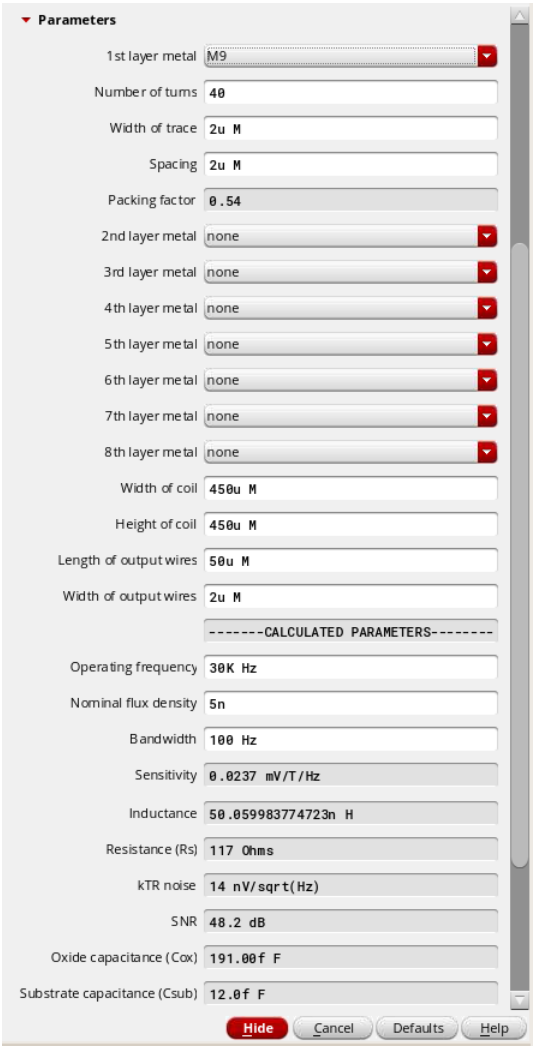

Fig. 10. Graphical user interface of the inductor PCELL.

4) Easier creation of complex designs.

This PCELL can be written by using the interactive programming language, SKILL (Cadence Design Systems, Inc.). As this work used many different input parameters to achieve an optimal solution, creating a PCELL was an attractive opportunity to speed up the design process.

B. Structure and Features of the Inductor PCELL

The graphical user interface of the new inductor PCELL is shown in Fig. 10. This PCELL supports the following features.

1) Multilayer design (up to eight layers in the stack).
2) A different width, spacing, and number of turns for each layer.
3) Custom via placement.
4) Physical parameter estimation (R, L, C, etc.).

In a multilayer planar coil design, the resistance of the via (which is used to connect metal layers) may become a significant bottleneck.

In order to eliminate this problem, a custom via tuning option was added to PCELL. This option allowed the user to adjust the size of the via to minimize via resistance.

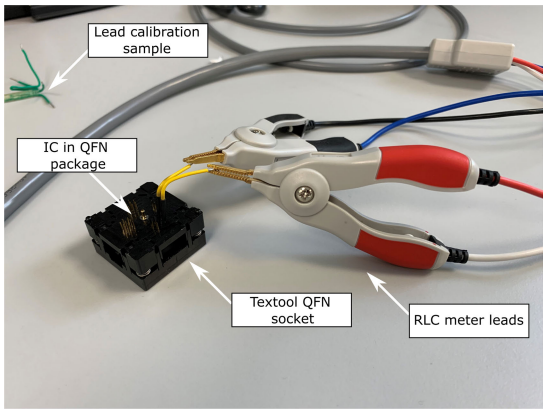

Fig. 11. Test setup for impedance measurements.

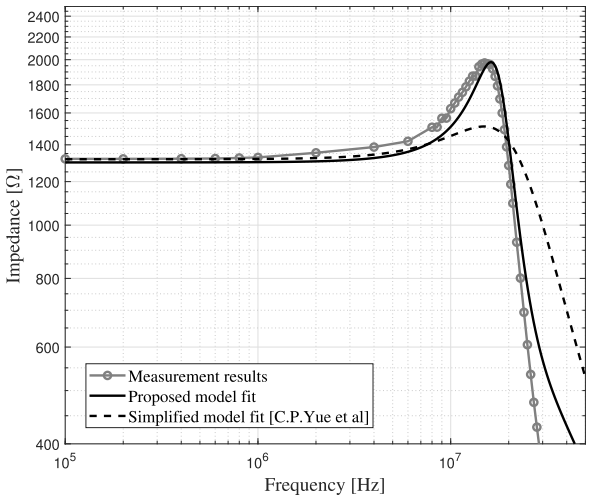

Fig. 12. Inductor impedance measurements.

The PCELL provides estimates of SNR, sensitivity, and physical parameters of the coil (like resistance, inductance, and capacitance). In order to increase possible design features, the PCELL contains stitching and paralleling functions. Like other PCELLs, this inductor PCELL satisfies all the limitations of the process design kit (PDK) rules of the 65-nm manufacturing process.

V. Implementation

The optimized design described in Section II was implemented on the TSMC 65-nm process within the overall sensor IC and the chip was mounted in a QFN package [19].

A. Impedance Measurements

Impedance measurements were performed using an HP4285A precision LCR meter. Open and short corrections have been used to account for test lead effects, as well as the result averaging over four iterations (see Fig. 11).

Fig. 12 shows the comparison between measured and simulated impedance using the simplified inductor model. As expected, it can be seen that the inductor exhibits completely resistive behavior up to 1 MHz.

As can also be seen from Fig. 12, the simplified model does not predict the impedance behavior well, due to some

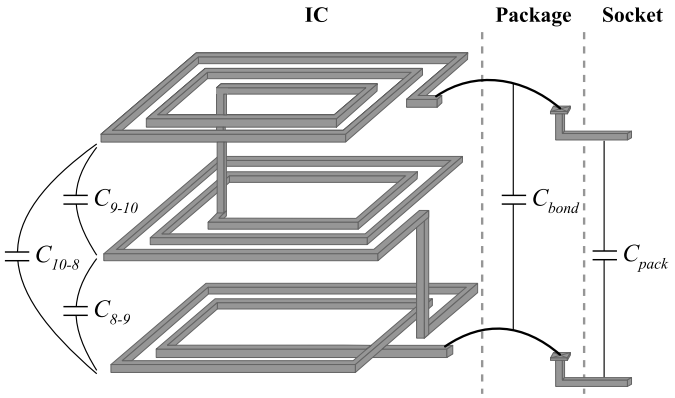

Fig. 13. Updated model for the multilayer stacked inductor.

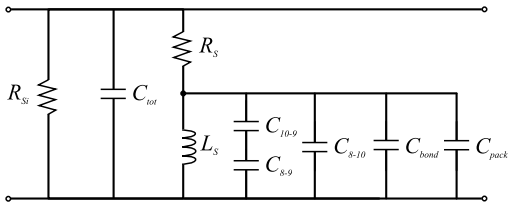

Fig. 14. Full updated model for the multilayer stacked inductor.

important parasitics, which are not taken into account in the model. These parasitics include the layer-to-layer capacitance as well as the capacitance of the bond wires and socket leads (see Fig. 13).

In order to fit the measured impedance, a modified model has been introduced (see Fig. 14). Capacitors C_{9-10}, C_{8-9}, and C_{10-8} represent the corresponding layer-to-layer capacitances which can be approximately calculated using the packing factor of each layer

$$C_{ij} = \frac{k_i + k_{i+1}}{2} A_{\text{plate}} \tag{29}$$

where A_{plate} is the area of the inductor and k is the packing factor of the layer of the inductor which can be calculated as follows:

$$k_i = \frac{w_i}{w_i + s_i} \tag{30}$$

where w_i and s_i are the width and spacing (in μm) between the traces, respectively. The terms C_{bond} and C_{pack}, which represent the capacitance of the bond wires and packaging, respectively, can be calculated as parallel capacitances. The updated model which includes all parasitic capacitances is depicted in Fig. 14. It is worth emphasizing that C_{9-10}, C_{8-9}, and C_{10-8} represent process-specific capacitances which may be analytically calculated while C_{bond} and C_{pack} will depend on the measurement setup for testing. For simplicity, the described capacitors which couple across L_s can be combined in a single term C_m

$$C_m = \frac{C_{10-9}C_{8-9}}{C_{10-9} + C_{8-9}} + C_{8-10} + C_{\text{bond}} + C_{\text{pack}}. \tag{31}$$

Therefore, the simplified inductor model for multilayer stacked inductor takes the form (see Fig. 15).

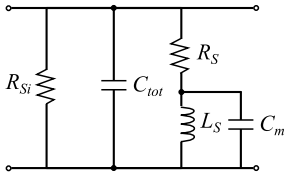

Fig. 15. Updated low-frequency model for the multilayer stacked inductor.

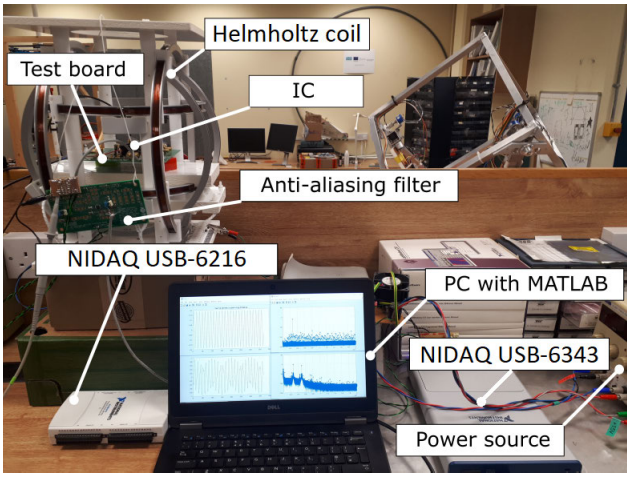

Fig. 16. Test setup for SNR measurements.

B. SNR and Sensitivity Measurements

The key metric for this design was SNR, as it represents both the noise and sensitivity of the inductor. SNR has been measured in conjunction with the analog ON-chip front-end and an OFF-chip second order Butterworth filter to prevent aliasing. The data acquisition has been performed using a NIDAQ USB-6343 (National Instruments, Austin, TX, USA). The signal was fed into the inductor by a 3-D Ferronato BH300HF-3-B Helmholtz coil, which is optimized for generating fields with frequencies from dc up to 300 kHz and field strengths up to 150 μT (see Fig. 16).

A Helmholtz coil is a co-axial pair of identical coils, wired in series to produce a uniform field in a small cylindrical volume between the two coils. The radius of the coils is equal to the intercoil spacing, and the field is effectively uniform (within 1%) in a cylindrical volume, co-axial with the coils.

The coil is controlled by a National Instruments USB-6343 data acquisition unit with DAC and ADC both running at 400 kS/s, driving a sine wave into an LT1210 power amplifier. The driver circuit also includes a bank of relay-switched capacitors in series with the coil, creating a tunable resonant series LC circuit, whose performance is controlled through a current sensing resistor.

For a desired field frequency and strength, the software controls the appropriate relays to select the nearest available capacitance value to drive the coil near resonance, outputs the frequency of interest to the amplifier at an initial default amplitude, and adjusts this amplitude according to the sensed current to generate a field at the desired strength. The total harmonic distortion (THD) of the coil current with reference to the desired frequency is also monitored through the software.

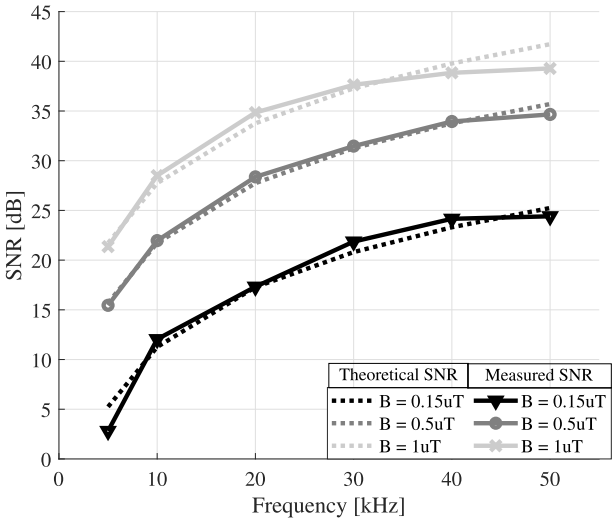

Fig. 17. SNR of the system.

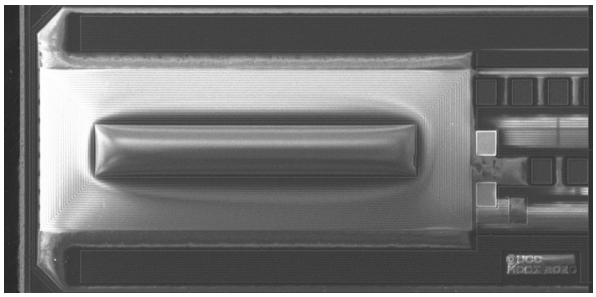

Fig. 18. Die photograph of the inductor structure.

The results of the measurements are depicted in Fig. 17. Since the analog front end contributes to the noise voltage, it is worth taking it into account. The measured input-referred noise of the analog front-end $[(S_{n(\mathrm{AFE})}(f))^{1/2}]$ is equal to 1.25 nV/$\sqrt{\mathrm{Hz}}$. Hence, the rms input-referred noise voltage of the analog front end for a given bandwidth Δf is

$$\sqrt{\overline{V_{n(\mathrm{AFE}),\mathrm{in}}{}^2}} = \sqrt{S_{n(\mathrm{AFE})}(f)\Delta f} \tag{32}$$

where $S_{n(\mathrm{AFE})}(f)$ is the voltage noise density of the analog front-end. Thus, the SNR takes the form

$$\mathrm{SNR} = \frac{\sqrt{\overline{V_s{}^2}}}{\sqrt{\overline{V_n{}^2} + \sqrt{\overline{V_{n(\mathrm{AFE}),\mathrm{in}}{}^2}}}}. \tag{33}$$

Using (11), we can obtain

$$\mathrm{SNR} = \frac{k_s B_0 f_0}{\sqrt{2\Delta f}(\sqrt{4k_B T R_s} + \overline{V_{n(\mathrm{AFE}),\mathrm{in}}{}^2})}. \tag{34}$$

It is worth noting that the SNR calculations are obtained for the bandwidth of 100 Hz which corresponds to the refresh rate of the system (see Fig. 17).

As can be seen from Fig. 17, the SNR of the inductor provides good matching with the theoretical predictions.

The manufactured chip containing the proposed inductor structure is depicted in Fig. 18.

TABLE II
MEASURED INDUCTOR PERFORMANCE

Coil parameters estimation		
Coil parameter	**Calculation result**	**Measurement result**
Sensitivity, $\mu V/T/Hz$	202.3	197.9
SNR$^{(a)}$, dB	23.6	22.1
Inductance, μH	7.7	8.07
Resistance, Ω	1276	1317

[a] At *f=20kHz* and *B=150nT*

VI. CONCLUSION

In this article, the design and optimization process for a planar inductor for time-varying magnetic field sensing in magnetic tracking applications has been presented. Optimal multilayer inductor configurations for the TSMC 65-nm process are represented in Table I. Table II shows the overall comparison between the calculated and measured parameters of the inductor. It can be seen that the calculations are closely matching with the experimental results. A modified planar inductor lumped-element model has been proposed to account for multilayer stacked designs and real-world instrumentation effects.

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