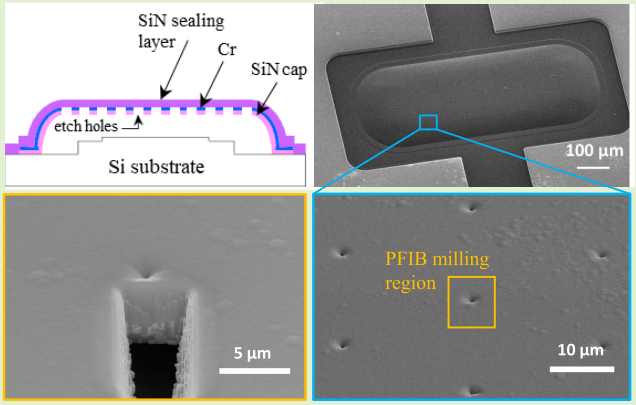
Low-Temperature Thin Film Encapsulation for MEMS With Silicon Nitride/Chromium Cap

Anna Persano, Alvise Bagolini, Jacopo Iannacci, *Senior Member, IEEE*, David Novel, Adriana Campa, and Fabio Quaranta

***Abstract*—In this work, a low-temperature fabrication process of thin-film encapsulation (TFE) with silicon nitride/chromium cap is proposed for large-size (750 × 300 μm) packaging of microelectromechanical systems (MEMS). A finite element method (FEM) model was developed to evaluate the shape of TFE as a function of the residual stress and the thickness of the sealing layer, providing useful guidelines for the fabrication process. The low temperature of 200 °C, which was used in the plasma-enhanced chemical vapor deposition (PECVD) of the silicon nitride capping layer, allowed an organic sacrificial material to be employed for the definition of the encapsulation area. Silicon nitride/chromium (1 μm/20 nm) bilayer was demonstrated to be successful to overcome the technological limitations that affect the creation of cap holes with size of ∼2 μm on high-topography substrates, as in the case of MEMS. Plasma focused ion beam (PFIB) and scanning electron microscopy (SEM) techniques were used in combination to gain deeper insight into the sealing process of cap holes. Specifically, a PFIB–SEM serial section procedure was developed, resulting to be a powerful tool to directly observe the sealing profile above cap holes. Hence, the presented results greatly contribute to overcome the main technological/reliability issues of TFE, paving the way for the widespread application of the proposed encapsulation methodology to the most used MEMS devices, such as radio frequency (RF) switches, transducers, actuators, sensors, and resonators.**



***Index Terms*—Microelectromechanical systems (MEMS), residual stress, silicon nitride, thin-film encapsulation (TFE).**

I. Introduction

MICROELECTROMECHANICAL systems (MEMS)-based sensors, -actuators, and -transducers have been pioneering various market applications and sectors for more than three decades. Starting from the first successful exploitation of inertial sensors for airbags in the automotive industry in the 1990s, MEMS-based devices have known successive waves in mass-market applications, like game consoles and smartphones and, more recently, wearables [1]. In terms of numbers, MEMS technology has been employed in all the main sectors, such as consumer, automotive, industrial, and telecom, reached a market volume of about U.S. $12 B in 2020 with important growing rates forecast in the next years [1]. Given this scenario, the future paradigms of 6G, super Internet of Things (Super-IoT), and tactile Internet (TI), will increasingly rely on smart, highly integrated, and power autonomous sensors and devices based on MEMS and nanoelectromechanical systems (NEMS) [2]. From a technology-related perspective, the mentioned applications pose nontrivial challenges in terms of manufacturing, integration, sensors fusions, and interfacing of heterogenous technologies, along with reliability and performance stability of MEMS/NEMS devices. To this end, a pivotal role can be played by packaging solutions since they ensure proper encapsulation and protection of micromechanical devices from harmful environmental factors, while easing integration of such components within subsystems and systems [3], [4].

Thin-film encapsulation (TFE) is an alternative and attractive technique to wafer bonding for packaging of MEMS, as it helps in the reduction of the overall device thickness,

Manuscript received 31 May 2023; accepted 19 June 2023. Date of publication 30 June 2023; date of current version 1 August 2023. This work was supported by the Italian Space Agency (ASI) under Project F36C18000400005 titled “Wafer-level micropackaging of RF MEMS switches for spatial applications” in the call “Nuove idee per la componentistica spaziale del futuro. The work of David Novel was supported by the Caritro Foundation under Project FLEXBOND.” The associate editor coordinating the review of this article and approving it for publication was Dr. Mert Torunbalci. *(Corresponding author: Anna Persano.)*

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This article has supplementary downloadable material available at https://doi.org/10.1109/JSEN.2023.3289594, provided by the authors.

Digital Object Identifier 10.1109/JSEN.2023.3289594

seal ring area, and cost due to the elimination of the cap wafer [5], [6].

Fabrication of TFE mainly implies the following technological steps: 1) deposition of a sacrificial layer on the wafer with unreleased MEMS devices; 2) patterning of the sacrificial layer to define the encapsulation area; 3) deposition of the cap layer in a metal, dielectric or semiconductor material with a thickness in the range of 1–10 μm; 4) patterning of the cap layer to create the matrix of etch holes; 5) removal of the sacrificial material through the etch holes; and 6) sealing.

A drawback of TFE method is the difficulty to encapsulate large-size MEMS devices, due to the low spring constant of the large and thin cap layer. To improve the robustness of TFE caps, periodic columns to support the capping structure [7] or thicker layers for capping and/or sealing [8], [9], [10] have been proposed in literature, but they generally imply difficulties in the fabrication, introduce an unnecessary increase in topography or cannot be used for all MEMS devices. A robust Ni/aluminum nitride (AlN) bilayer cap has been also presented [11] for TFE of MEMS, but this solution cannot be used in situations, where nickel is a contamination.

The residual stress of capping and sealing layers in TFE is an important concern to assure robustness and reliability to TFE. In fact, a thin film is desirable for sealing to reduce processing cost and time, but it might cause faulty sealing or excessive downward bending due to the low-cavity internal pressure and film residual stress. Generally, a low ($<$100 MPa) tensile stress is beneficial for capping layer since voids and buckling may form in the thin film if tensile or compressive stress exceeds a critical level, either during deposition of the thin film or during use [12]. Otherwise, an overall compressive residual stress is desirable for the sealing layer to counter structure downward bending that might be generated by a tensile state and/or the difference of pressure inside and outside the encapsulation MEMS cavity.

In the fabrication of TFE, a particular attention has been also devoted to the choice of the sacrificial material. The sacrificial material has to satisfy the following requirements: 1) good selectivity during the release with respect to the cap and the other structural materials, which are used in the fabrication of MEMS devices and 2) easy deposition and patterning with a good uniformity of thickness on large areas. Inorganic materials, like silicon oxide and amorphous silicon, are generally used as sacrificial materials [7], [10], [11], [13], but their etching requires F-based vapors that could be a serious challenge in combination with micromachining technologies for structures containing aluminum or silicon oxide. Organic sacrificial materials can be removed with an oxygen plasma etching [14], [15], leaving more freedom for the choice of the capping layer material that can suit the application (optically transparent and metal capping layer). Organic materials are also suitable for process flows at low temperature ($<$100 °C), which are mandatory for applications when a lower thermal budget is required [16], [17]. On the other hand, a high-temperature process is suitable for encapsulating MEMS devices made out of materials that can withstand high temperatures, such as silicon, poly-silicon, silicon dioxide, silicon nitride, and AlN, but it may affect metal contacts and/or induce out-of-plane deformations in the suspended beams of MEMS [18].

Another critical issue of TFE fabrication is the release time for the removal of the sacrificial material. A long release time may limit choices of cap and sacrificial layer materials because it might increase the chance that the release etch attacks the cap layer or MEMS device during the release process. Consequently, the release time should be as fast as possible to reduce this attack and to improve the throughput of the TFE process. A distribution of etch holes of $\sim$2 μm in diameter is generally created in the cap layer to allow the release process [15], [19]. In particular, the cap hole size has to be large enough to allow the complete removal of the sacrificial material in a reasonably short etching time, but the hole size has to be as small as possible to facilitate the sealing. From the technological point of view, the creation of cap holes of $\sim$2 μm in diameter is not trivial, due to the need to perform a high-resolution lithographic process on a nonplanar substrate, as in the case of MEMS.

Hence, it can be concluded that a deep investigation of materials and processes to be used for the fabrication of TFE is mandatory to solve the technological/reliability issues that still limit the widespread application of TFE to MEMS, such as the moderate thermal budget of the fabrication process, a properly tailored residual stress in the capping and sealing layers, the encapsulation of large area devices, and the creation of cap holes with size suitable to achieve a fast release and a safe sealing. In particular, the trade-off between the use of a thin sealing film and the need for a perfectly sealed and sufficiently high encapsulation cavity is paramount.

In this work, a fabrication process of TFE for MEMS is developed. Section II presents the finite element method (FEM) model that is formulated and used prior fabrication to predict the effects on the TFE shape of the residual stress in the sealing layer made out of silicon nitride with thickness in the range of 1.5–4 μm. As described in Section III, the design and the process flow are conceived to address the technological issues that still affect TFE fabrication. Experimental results are presented and discussed in Section IV, especially those concerning the creation of cap holes, the release, and the sealing. Finally, the conclusions derived from the presented work are presented in Section V.

II. Finite-Element Model

A finite-element model was developed, using Ansys1 software, to predict the shape of TFE as a function of sealing layer residual stress and thickness. The modeled encapsulation cavity is of 750 $\times$ 300 μm with a height of 20 μm, as required for the packaging of most MEMS devices. The packaging model is made of two layers with a different thickness and residual stress to reproduce TFE capping and sealing layers. Silicon nitride was chosen as material for both layers since it satisfies some essential requirements in the perspective to make the packaging process suitable for industrial production, such as a good structural integrity and selectivity with respect to the sacrificial material during the chemical etching, an excellent

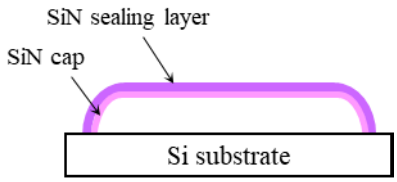

Fig. 1. Schematic of the TFE model.

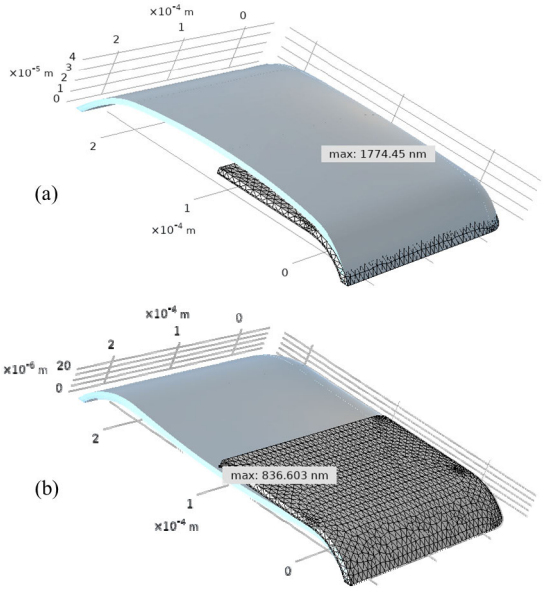

Fig. 2. Bending of TFE generated by (a) residual compressive stress of −690 MPa and (b) tensile stress of 200 MPa in the sealing layer, having this last a thickness of 4 μm. The TFE shapes without and with residual stresses are shown in dark and blue color, respectively. The displacement values of the TFE center are also reported.

insulation during device operation, and an optimized deposition rate in relation to the thickness to achieve. Moreover, plasma-enhanced chemical vapor deposition (PECVD) offers the possibility to obtain silicon nitride films with controlled residual stress by changing the plasma generator frequency and gas flows [20], [21]. The silicon nitride capping layer is supposed to have a thickness of 1 μm and an ultralow (<10 MPa) residual tensile stress, as already reported for mixed-frequency (MF) PECVD silicon nitride films [22]. The modeled sealing material is a PECVD silicon nitride deposited at a pressure of 550 mtorr, which sets the sealed cavity's final internal pressure. A Young's modulus of 200 GPa is supposed for silicon nitride of both layers [23]. The thin chromium layer, which was used in the fabrication of the device as a hard mask, was excluded from this model, after initial simulation showed that its contribution is largely negligible due to the very limited thickness. A schematic of TFE model is reported in Fig. 1.

The model of one quarter of the cap was created, and meshing was performed with triangle shapes, obtaining 19 318 elements. Linear structural static analysis was used to obtain the height of the TFE as a function of sealing layer residual stress and thickness. A set of simulations was performed varying the sealing film thickness in the range of 1.5–4 μm and

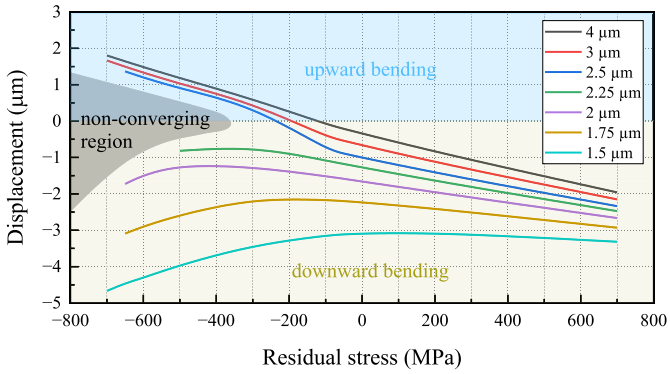

Fig. 3. Displacement of the TFE center as a function of residual stress and thickness of the sealing film.

the residual stress from a highly tensile (700 MPa) to a highly compressive value (−700 MPa). Fig. 2(a) and (b) shows the effect on the TFE shape of a residual compressive stress of −690 MPa and tensile stress of 200 MPa, respectively, in the sealing layer, having this last a thickness of 4 μm. An upward and a downward bending of TFE are visibly observed in the first and second cases, respectively.

Fig. 3 shows the displacement of TFE center as a function of the residual stress in the sealing layer, whose thickness varies in the range of 1.5–4 μm. As expected, a tensile stress causes a downward displacement, which shows an increase linearly proportional to the stress value. In the case of compressive stress, a downward bending is also observed for thicknesses up to 2.25 μm. For thicknesses greater than 2.5 μm, an inversion of bending, from downward to upward, is observed. In particular, a turning point is obtained for a sealing thickness between 2.25 and 2.5 μm and a compressive stress greater than ∼350 MPa: thicknesses greater than 2.5 μm are affected by an increase of the upward bending, whereas thicknesses lower than 2.25 μm exhibit an increase of downward displacement, which is caused by a negative buckling of the cap. This buckling is more pronounced at higher compressive stress values, as expected in buckling phenomena. A region of instability, where the FEM analysis does not converge, is also reported in Fig. 3. In this region, the combined effect of pressure gradient and residual stress generates an unstable equilibrium in the model.

Simulation results were used as guidelines to identify thickness and residual stress values in the sealing layer that are suitable to avoid significant deformations of the encapsulation structure and/or buckling phenomena. In particular, simulations show that for a sealing thickness greater than 2.5 μm, as generally required for the complete sealing of cap holes, a compressive stress between 100–200 and 700 MPa is predicted to obtain a slight (<1.8 μm) upward bending of TFE, which could be beneficial to counter the downward bending of TFE due to the tensile stress in the capping layer and/or to the different pressure between the inside and outside of the encapsulation cavity.

III. Design and Process Flow

The fabrication process of TFE for MEMS is significantly influenced by the high topography of the substrate, due to

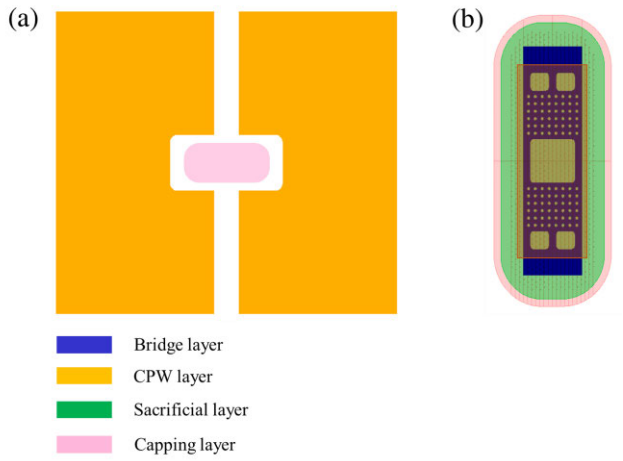

Fig. 4. (a) Design of TFE, beam, and CPW. (b) Details of TFE and encapsulated beam.

the presence of devices to be encapsulated. Moreover, other components are generally required for the operation of MEMS, such as the coplanar waveguides (CPWs) in the case of radio frequency (RF) MEMS switches. These elements do not need encapsulation, but they contribute to substrate topography. In order to consider this aspect, TFE structures are designed in the central part of a CPW [Fig. 4(a)], and a beam with the same shape as those typically used in MEMS is placed inside TFE structures [Fig. 4(b)]. To exactly replicate the topography of MEMS, a uniform distribution of holes with a diameter and pitch of 10 μm is situated in the beam. The encapsulation area, which is defined by the sacrificial material [see green area in Fig. 4(b)], is of 750 $\times$ 300 μm with a curvature of 120 μm at the corners. The cap covering the encapsulation area has a 20-μm-wide sealing ring [see pink area in Fig. 4(b)] and contains a uniform distribution of holes with different densities and diameters. Hole diameter (D) varies in the range of 2–3 μm and the percentage ratio between the hole total area and the encapsulating area ranges from 1% to 4%, resulting in a minimal distance between holes (pitch) varying from 10 to 17 μm.

The high topography of substrate due to the presence of MEMS and CPWs was created by carrying out a Bosch silicon deep reactive-ion etching (DRIE) in two steps [Fig. 5(a)]. First, an etching of 2.5 μm was performed to create the beam [see blue area in Fig. 4(b)]; then, a second etching of 10.5 μm was carried out to create the CPW and a rectangular shape on the beam [see orange areas in Fig. 4(a) and (b)]. The substrate profile in the directions longitudinal and transverse to the beam is sketched in Fig. 5(b) and (c), respectively.

A surface micromachining approach was used to fabricate TFE structures [Fig. 6(a)–(h)]. The positive resist AZ12XT was used as a sacrificial material to define the encapsulating area with a height of ~18 μm. To this scope, the following processes were performed: spin coating at 3000 r/min, exposure to UV radiation, development, and hard bake of 200 °C for 10 min to harden the sacrificial structure. A 1-μm-thick silicon nitride film was deposited on the sacrificial structure to form the capping layer. This layer was deposited in an

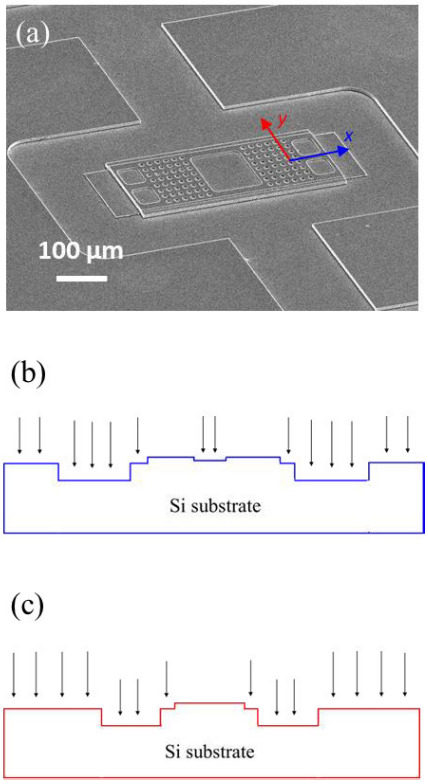

Fig. 5. (a) SEM plan view of the substrate topography after Bosch etchings. (b) and (c) Sketches of vertical profiles of micromachined substrate along the directions longitudinal (x) and transverse (y) to the beam, respectively. The profile directions are also shown in (a).

MF single process, using a coupled planar parallel electrode Multiplex Series PECVD (Surface Technology Systems Ltd.) with an electrode diameter of 24 cm. The system is equipped with a high-frequency (HF) generator at 13.56 MHz and a low-frequency (LF) generator at 380 kHz. The MF procedure consists in varying the modulation of HF and LF of RF power supply during the deposition, without changing the flows of reaction gases. For PECVD silicon nitride, it has been demonstrated [20], [21] that at HF (13.56 MHz), the stress is compressive, whereas at LFs (50 kHz), the stress is tensile. Therefore, low-stress dielectric layers can be deposited by stacking a tailored sequence of tensile and compressive layers deposited by HF and LF plasma, respectively. The stress of various layers compensates, providing a low-stress material that is stable, also if processed at high temperatures. Here, the intervals at HF and LF plasma excitation of one cycle during the deposition process are 8 and 3 s, respectively. Due to the presence of the organic sacrificial material, a PECVD process was developed at a temperature lower than 300 °C, which is the temperature generally used for PECVD silicon nitride [19], [22], [24]. The operating temperature of the shower head (coil) of the machine is 250 °C, while the temperature of the chuck (platen) where the wafer is placed during the deposition process is 200 °C. The other parameters for silicon nitride deposition are 40 sccm of NH_3, 40 sccm of SiH_4, 1960 sccm of N_2, chamber pressure of 900 mtorr, HF generator power of 30 W, and LF generator power of 20 W.

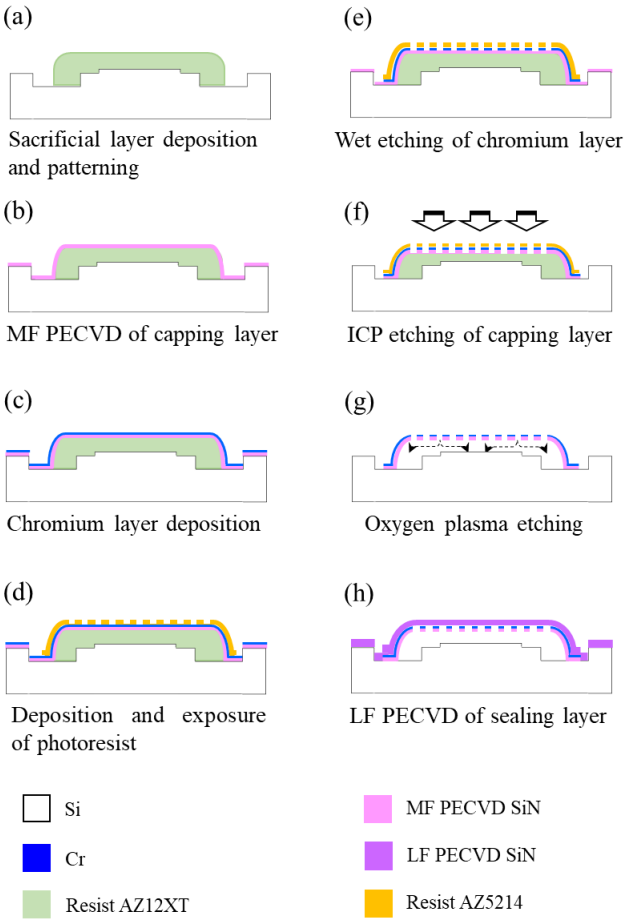

Fig. 6. Process flow for the fabrication of TFE structures with silicon nitride/chromium bilayer cap. In the case of cap made of sole silicon nitride, the steps (c) and (e) were not performed. (a) Sacrificial layer deposition and patterning. (b) MF PECVD of capping layer. (c) Chromium layer deposition. (d) Deposition and exposure of photoresist. (e) Wet etching of chromium layer. (f) ICP etching of capping layer. (g) Oxygen plasma etching. (h) LF PECVD of sealing layer.

Measurements of residual stress were performed on full wafers with the wafer curvature method, using the Stoney model [25]. Measurements were carried out with a Kla-Tencor mechanical profilometer, and equipped with a 2-μm diamond stylus tip. Three profiles were measured for each sample along its diameter, separated by an offset of 5 mm; the resulting stress data showed a standard deviation better than 3%. This standard deviation is valid for all stress data reported. A low tensile stress value of 2.2 MPa was measured for the silicon nitride deposited at MF, in agreement with the value reported in the literature [24]. Linear profiles along TFE structures were performed under the application of stylus forces in the range of 4.9–490 μN.

Silicon nitride/chromium (1 μm/20 nm) bilayer caps were also deposited. Both typologies of the capping layer, made of the sole silicon nitride layer and the silicon nitride/chromium bilayer, were patterned by optical lithography to define etch holes with diameters of 2–3 μm. For this purpose, positive photoresist AZ5214 with a thickness of 1.4 μm was deposited on the cap. After spin coating and exposure of the photoresist, a wet etching of 1 min in the solution TechniEtch Cr n:1 was performed to remove the chromium inside the holes in the bilayer cap, being this process selective with respect to the used photoresist. The chromium thickness was chosen as a compromise between the needs to provide a sufficient hard masking and to avoid the widening of holes during wet etching. An inductively coupled plasma (ICP) etching was performed to open the access holes in the capping layer. The ICP etching parameters are pressure of 5 mtorr, 10 sccm of O_2, 100 sccm of SF_6, coil power of 300 W, platen power of 10 W, time of 210 s, and rate of 312 nm/min. An oxygen plasma etching was performed for 100 min in a barrel etcher to remove the sacrificial organic material inside TFE. The other parameters of barrel etching are pressure of 600 mtorr, 300 sccm of O_2 with a small percentage ($<$1%) of SF_6, and pressure of 200 W. Adding a small amount of SF_6 can significantly increase the photoresist etching rate because highly reactive fluorine atoms can boost the rate of extracting hydrogen from the photoresist polymer.

A 4-μm-thick silicon nitride layer, which was obtained at 300 °C by the LF PECVD process, was used to seal TFE caps. Low-frequency PECVD silicon nitride deposited at 300 °C has been already used for this purpose [19], due to its thermal expansion compatibility with common cap materials and moisture barrier properties [26]. Here, other deposition parameters used for LF PECVD of silicon nitride are chamber pressure of 550 mtorr; 1960 sccm of N_2, 40 sccm of SiH_4, 20 sccm of NH_3, LF generator power of 60 W, and rate of 45.5 nm/min. The residual stress measured for the sealing silicon nitride is -690 MPa. Thickness and residual stress of the sealing layer were chosen, according to previous simulations that predict a negligible (1–2 μm) upward bending of TFE for a sealing thickness and residual stress of 4 μm and -700 MPa, respectively (see Fig. 3).

IV. Results and Discussion

A. Creation of Cap Holes

Fig. 7(a) shows a silicon nitride TFE cap after the deposition and the exposure of the photoresist for the definition of etch holes with a size of 2 μm. The cap hole pattern with the underlying sacrificial material is clearly visible in Fig. 7(b).

Fig. 7(c) shows the profilometry scans recorded along the TFE covered by the photoresist with stylus forces of 4.9 and 490 μN. The cap shows a quite flat profile with a height of 19 μm in the center. A downward bending of the central region of TFE cap is observed with respect to the edges, which is generated by reflow effects in the underlying photoresist during hard bake. Due to this hardening process of the sacrificial material, no variation is observed in profiles with increased stylus force.

Here, a fluorine-based ICP etching was used to create the etch holes in the TFE cap. A trade-off between photoresist thickness and minimum feature size has to be found, given the limitations of optical photolithography and the selectivity of the plasma etching process. Moreover, the uniformity of the photoresist across the wafer is inevitably compromised by the high topography of the substrate, due to the presence

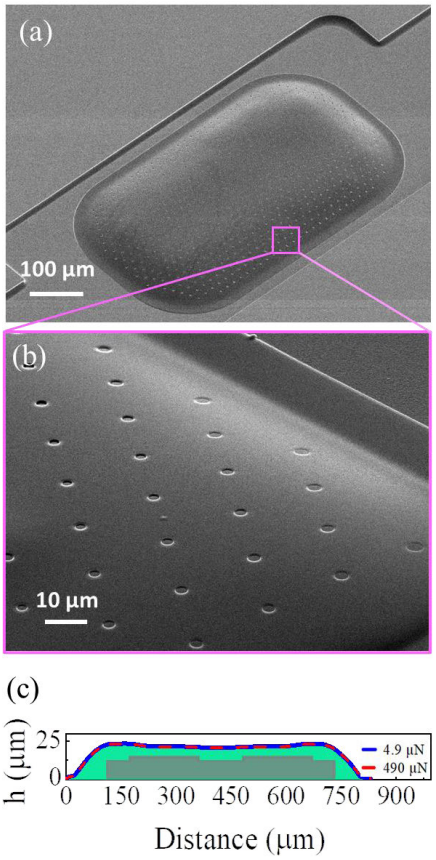

Fig. 7. SEM images of (a) whole silicon nitride TFE cap and (b) region of the TFE cap, after the deposition and the exposure of the photoresist for the definition of holes with a size of 2 μm. (c) Profiles along the TFE structure after the lithographic patterning. The substrate profile is also sketched in (c).

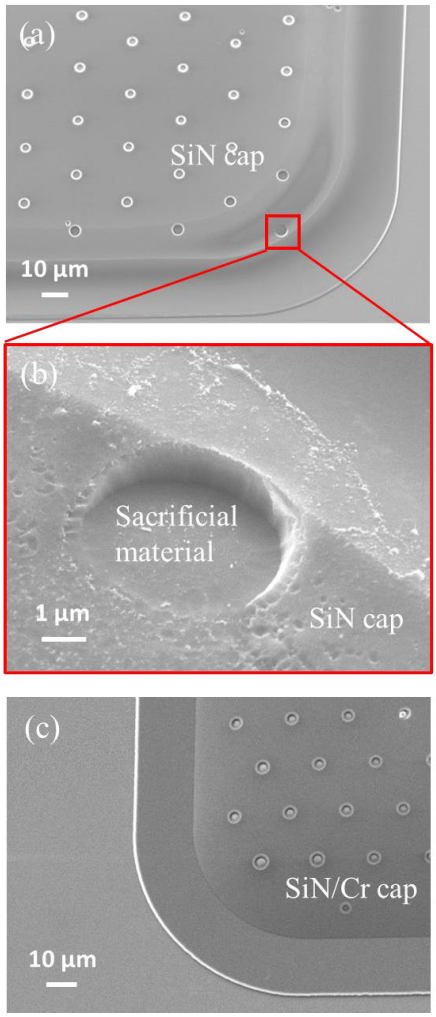

Fig. 8. (a) SEM top view of the border and corner regions of a silicon nitride cap after ICP etching. (b) High-magnification SEM image of a hole in the silicon nitride TFE cap at the corner region. (c) SEM top view of the border and corner regions of a silicon nitride/chromium bilayer cap after ICP etching.

of CPWs and sacrificial structures to be encapsulated. From several performed tests, it was found that the positive resist AZ5214 with the thickness of 1.4 μm is the best trade-off solution to pattern TFE cap with holes of 2–3 μm, considering the inevitable photoresist thinning in the regions of high-topographical variation, which are the cap borders and corners.

Significantly different results were obtained after ICP etching for caps made of the sole silicon nitride layer and of the silicon nitride/chromium bilayer. In the first case, a ring along the cap edge, especially at the corner, is clearly visible, which indicates an unwanted etching of silicon nitride in the regions where the photoresist is thinner [Fig. 8(a)]. In agreement with this interpretation, Fig. 8(b) shows a significant reduction of silicon nitride thickness along the edge of a hole situated at the corner of the cap. It is worth noting that the hole in Fig. 8(b) also shows a widening effect because at the corners of the encapsulation, the lithographic mask is not in contact with the cap. To avoid this effect, in successive samples, etch holes have not been placed at the cap corners.

Fig. 8(c) shows the border and corner regions of a silicon nitride/chromium bilayer cap after the ICP etching. No ring is observed along the border and at the corner, denoting that the chromium layer effectively prevents the etching of silicon nitride in the regions, where the photoresist is thinner.

B. Release

An oxygen plasma etching was performed in a barrel etcher to remove the sacrificial material through the etch holes of the TFE cap. Fig. 9(a) and (b) shows the corner and border regions of a silicon nitride cap after the release process. Perforation of the TFE cap is visible at the corner and along the border, which is caused by an unwanted ICP etching of the silicon nitride in the regions where the photoresist is thinner. Instead, no damage is observed at the corners and along the border of the silicon nitride/chromium bilayer cap, as observed from Fig. 9(c) and (d), respectively. This result confirms the success of the thin chromium film in protecting the silicon nitride cap from damage during the ICP etching.

The complete removal of the sacrificial material below the TFE cap depends on the interplay between the properties of the barrel etching and the geometric parameters of cap hole distribution. Due to its pure chemical nature, the barrel etching is an isotropic process. The spherical shape of the etching front below a hole in the TFE cap can be observed from Fig. 10(a). Fig. 10(b) and (c) shows the volume below the cap in the case of incomplete and complete removal of the sacrificial

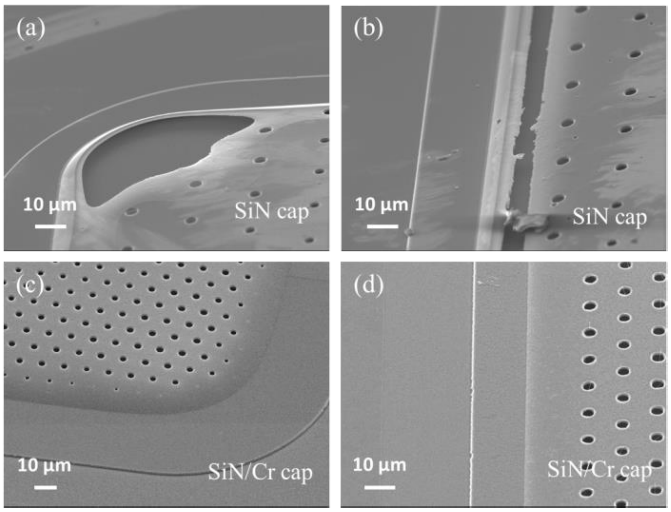

Fig. 9. SEM view of (a) corner and (b) border regions of a silicon nitride cap after release. SEM view of (c) corner and (d) border regions of a silicon nitride/chromium bilayer cap after release.

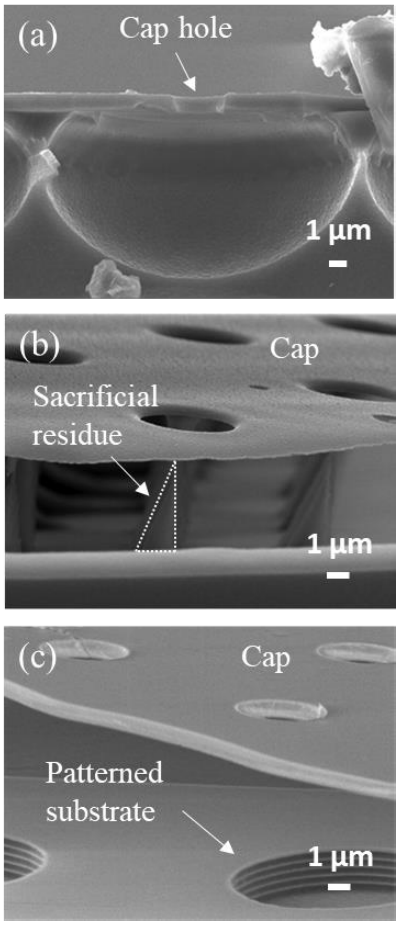

Fig. 10. SEM images of silicon nitride/chromium bilayer caps that have been intentionally broken after the oxygen plasma etching. (a) Isotropic etching front below a cap hole. (b) Residual sacrificial material between cap holes in the case of incomplete release. (c) Volume below the cap in the case of complete release.

material, respectively. As expected, the regions more critical for the removal of the sacrificial material are those between holes. Consequently, the size and the pitch of etch holes are determinant for the release time, which is required for the complete removal of the sacrificial material. Etch holes with a larger size are preferred for release, but these holes will hinder the efficient sealing of the TFE cap. The etching is also limited by the diffusion of etching species through the holes and to the etch front, and of the etch product from the etch front to the etch holes. In conclusion, the release time (t_{RE}) is expected to satisfy the following formula [13]:

$$t_{RE} \geq \frac{P - D}{2X} \tag{1}$$

where P is the pitch between holes, D is the hole size, and X is the etch rate of the sacrificial material. However, this formula can only provide a lower estimate of the expected release time. The performed etching tests started with the release of caps with larger ($D = 3\ \mu$m) and denser ($P = 10\ \mu$m) etch holes, before focusing on the release of caps with the smallest ($D = 2\ \mu$m) and less dense ($P = 17\ \mu$m) holes that is the most beneficial pattern for TFE sealing. Given the sacrificial material used here, it was found that the etching rate is 206 nm/min, and the release time is 100 min for the distribution of holes with $P = 17\ \mu$m and $D = 2\ \mu$m. The obtained release time satisfies the condition $t_{RE} > 36$ min that is given by (1).

Fig. 11(a) shows the scanning electron microscopy (SEM) image of a silicon nitride/chromium bilayer cap after the release process with $t_{RE} = 100$ min, $P = 17\ \mu$m, and $D = 2\ \mu$m. Optical inspection was also performed on the same cap to check the complete removal of the sacrificial material, as silicon nitride is a transparent material [Fig. 11(b)]. Optical images show that the TFE cap was properly released, without any sacrificial residues. Fig. 11(c) shows the mechanical profiles recorded for the TFE cap of Fig. 11(a) and (b) under the application of the stylus forces of 4.9–490 μN. Increasing the force, the cap bends due to the absence of the sacrificial material. Under the application of the highest force value, the cap results to be collapsed above the encapsulated beam, as pointed out by the cap height of 14.5 μm that is very close to the sum of the height of the beam (13 μm) and the bilayer cap thickness (1.02 μm). Consistently, the profile central concavity, having a width and depth of 100 and 2.5 μm, respectively, is perfectly conformal with the hole created in the beam with the first Bosch process step. Fig. 11(d) shows the increase of the cap deflection as a function of the applied force in six different points of the top surface [see green dotted lines in Fig. 11(c)] of five caps. Deflection is observed to increase with the applied force, until a saturation to the value of $4.6 \pm 0.4\ \mu$m.

C. Sealing

The last step in TFE fabrication is the sealing process, which was obtained by LF PECVD of a 4-μm-thick silicon nitride layer [Fig. 12(a)]. A high-resolution SEM image of a sealed 2-μm-sized hole is shown in Fig. 12(b). The granular morphology of the silicon nitride as well as some line features, which can be ascribed to the process of hole sealing, are observed. In order to gain more insight into the sealing process, a focused ion beam (FIB)–SEM analysis was

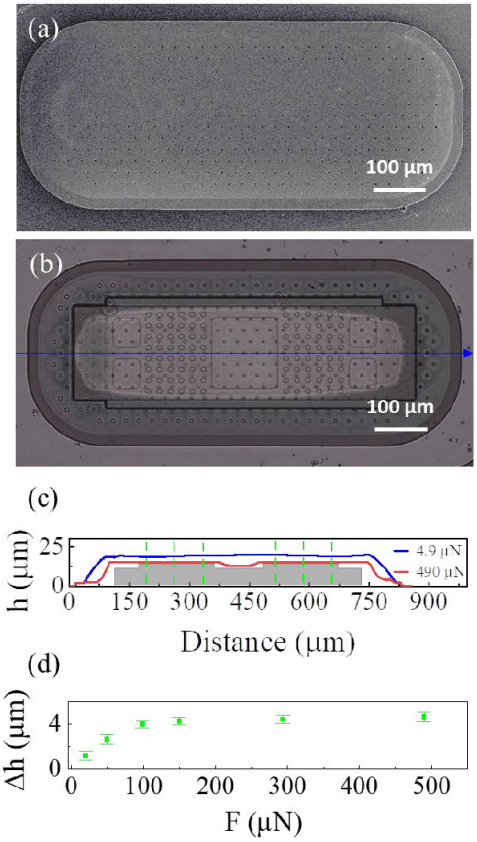

Fig. 11. (a) SEM plan-view and (b) optical microscope image of a released silicon nitride/chromium cap with holes of 2 μm. (c) Profiles along the blue line drown in (b) under the application of the stylus forces of 4.9 and 490 μN. (d) Deflection of the TFE cap as a function of the applied stylus force, starting from the profile recorded for the lowest force of 4.9 μN. The beam inside encapsulation is visible in (b) and different colors in the central part of the optical image is due to different focuses for the highest central region of cap compared to border regions. The substrate profile is also sketched in (c). Deflection values in (d) are calculated in the cap points indicated by the green dotted lines in (c).

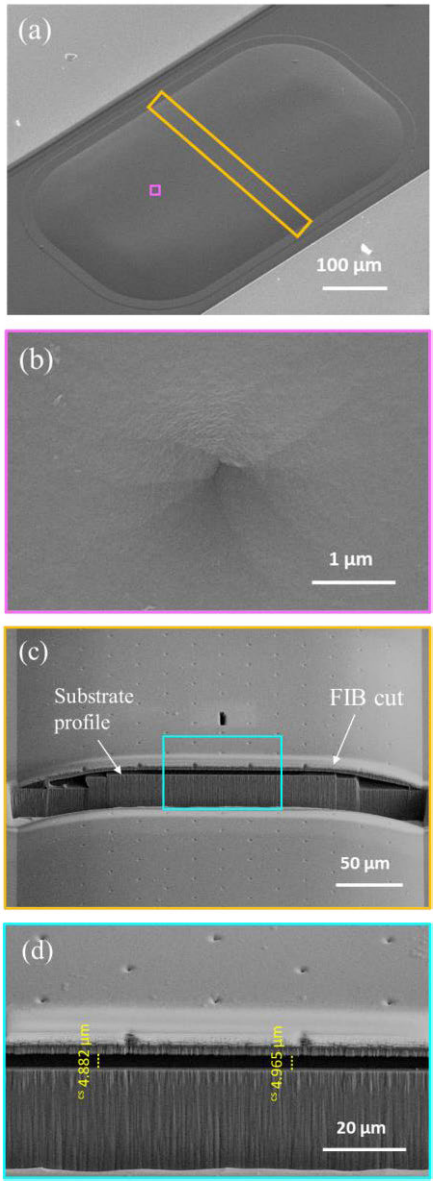

Fig. 12. (a) SEM image of a sealed TFE. (b) High-magnification SEM image of a sealed hole with size of 2 μm. (c) SEM cross-sectional view of an FIB cut through the sealed TFE. (d) Zoomed-in view of the air gap between the cap and the substrate. Frames of different colors are drawn in (a) and (c) to indicate the regions magnified in (b)–(d). Two measurements of the air gap inside encapsulation are also reported in (d).

performed with a Thermo Scientific Helios 5 Plasma FIB (PFIB) Dual Beam. FIB milling was carried out at 30 kV, with a large cut at a high current close to the area of interest. This cut was made through the TFE and exposes its layered structure. The FIB milling continues with a serial sectioning at a lower current in a process that resembles thinning of TEM lamellas. Fig. 12(c) shows the inside of TFE, which is observable from a typical FIB cut of the cap. The substrate profile, which was obtained with the performed Bosch etching of the silicon substrate [Fig. 5(c)], is visible. Complete removal of the sacrificial material is observed in the central region of the encapsulation cavity, which would be the region of interest for device operation. Specifically, the air gap between the encapsulated beam and the cap was extrapolated by SEM analysis [Fig. 12(d)], resulting to be 4.94 ± 0.05 μm, in agreement with profilometry measurements [Fig. 11(d)].

Similar results have been obtained for TFE with an area until 900×900 μm. For larger areas, a proper TFE scheme is probably needed to assure the robustness of the encapsulation.

The configuration of the electronic and ionic columns of the Helios PFIB–SEM allows to perform SEM microscopy, while the ion column is milling. This process can be automated with the intermittent switching between patterning and imaging features (iSPI), after having optimized the two beam scanning parameters to minimize image shift between consecutive cross sections. Multiple analyses were performed, with low amorphization depth because of Xe+ plasma [27], [28]. The sequence of SEM images was later converted with the FIJI platform [29] into a .gif file for visualization purposes (available in the Supporting Information). The obtained PFIB–SEM serial section procedure provides a valuable analytical tool to investigate the sealing process since, compared to the analysis of a single cross section, it allows to directly observe the sealing profile from the border to the center of the hole. Fig. 13(a)] and 13(b)] shows the SEM images recorded when

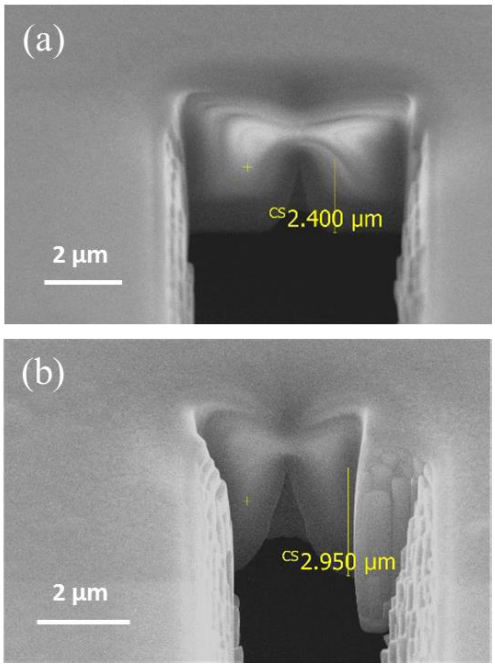

Fig. 13. SEM images recorded during a FIB cut through the diameter of 2 μm (a) and 2.5 μm (b) of a sealed hole cap. The measurements of the cusp height, which is visible on top of the sealed hole, are also reported in (a) and (b).

the FIB beam is cutting the hole along its maximum size, that is along its diameter of 2 and 2.5 μm, respectively. Under this condition, a cusp is visible in the profile of the sealing layer on top of the hole. The cusp height minus the cap thickness provides the direct measurement of the minimum material thickness required for the complete sealing of the cap hole. Cusp height measurements result to be 2.4 + 0.2 and 2.95 + 0.15 μm for holes with sizes of 2 and 2.5 μm, respectively. Hence, the minimal thicknesses of LF PECVD silicon nitride of ∼1.4- and ∼1.95-μm result are required for the complete sealing of cap holes with sizes of 2 and 2.5 μm, respectively. However, based on finite-element simulations (see Fig. 3), buckling phenomena could occur if the silicon nitride sealing layer is thinner than 2 μm and is affected by a high compressive stress. All these aspects have to be considered in the TFE design and fabrication.

The height increase of a TFE before and after FIB cut was measured, resulting to be of ∼390 nm. A simulation was performed to predict the height difference of fabricated TFE due to the increase of the internal pressure from low pressure (550 mtorr) to ambient pressure, as occurs before and after FIB perforation. The height increase is predicted to be 354 nm, pointing out that the performed FEM analysis is in good agreement with experimental results. It is worth noting that the pressure difference between the inside and the outside of the encapsulation cavity does not play a dominant role in setting the final cap height, its contribution being almost an order of magnitude less than that of residual stress. The residual deposition of silicon nitride inside encapsulation during the sealing process was investigated by SEM and atomic force microscopy (AFM). In the encapsulated area, traces of silicon nitride with a diameter of a few micrometers and a height of ∼100 nm were observed, only in correspondence to sealed etch holes. The presence of this residual silicon nitride has to be taken into account in the design of encapsulated devices, in order to optimize their performance.

V. Conclusion

A fabrication process for TFE of MEMS was developed, which overcomes the most critical technological issues arising from the need to obtain a thin, large-size, suspended, and sealed cap.

Prior to fabrication, an FEM analysis was carried out to assess the effect of sealing layer thickness and residual stress on the shape of the encapsulation. Such predictions were followed in the fabrication process to prevent significant TFE deformations.

The silicon nitride capping layer was deposited by an MF PECVD process at the temperature of 200 °C, allowing to use an organic sacrificial material that was easily removed by an oxygen plasma etching. Compared to the commonly used etching of sacrificial layers with aggressive and metal-corrosive vapors, the proposed technological solution leaves more flexibility with respect to materials of capping layer and device, thus widening the scope of application of the presented TFE. Caps made of the sole silicon nitride layer and the silicon nitride/chromium bilayer were compared, demonstrating the success of the chromium film to prevent the damage of silicon nitride at the corner and border regions during the etching for the creation of cap holes.

The volume inside sealed TFE was observed by the combined use of SEM and FIB techniques. Furthermore, a PFIB serial section procedure was developed to record SEM cross-sectional images of the sealed cap hole during the FIB cut. A cusp-like sealing profile is observed above the hole, inferring that the minimal thicknesses of LF PECVD silicon nitride, which is required for the complete sealing of cap holes with diameters of 2 and 2.5 μm, are ∼1.4 and 1.95 μm, respectively.

Acknowledgment

The authors would like to thank P. Cretì and M. C. Martucci for the technical support in the device fabrication process.

References

[1] (2021). *Status of the MEMS Industry*. [Online]. Available: https://www.i-micronews.com/products/status-of-the-mems-industry-2021/

[2] J. Iannacci and H. V. Poor, "Review and perspectives of micro/nano technologies as key-enablers of 6G," *IEEE Access*, vol. 10, pp. 55428–55458, 2022.

[3] S. Li, *SiP-System in Package Design and Simulation*, 1st ed. Hoboken, NJ, USA: Wiley, 2017.

[4] J. H. Lau, C. K. Lee, C. S. Premachandran, and Y. Aibin, *Advanced MEMS Packaging*, 1st ed. New York, NY, USA: McGraw-Hill Education, 2010.

[5] H. A. C. Tilmans et al., "MEMS packaging and reliability: An undividable couple," *Microelectron. Rel.*, vol. 52, nos. 9–10, pp. 2228–2234, Sep. 2012.

[6] A. Persano, F. Quaranta, A. Taurino, P. A. Siciliano, and J. Iannacci, "Thin film encapsulation for RF MEMS in 5G and modern telecommunication systems," *Sensors*, vol. 20, no. 7, p. 2133, Apr. 2020.

[7] F. Santagata, J. J. M. Zaal, V. G. Huerta, L. Mele, J. F. Creemer, and P. M. Sarro, "Mechanical design and characterization for MEMS thin-film packaging," *J. Microelectromech. Syst.*, vol. 21, no. 1, pp. 100–109, Feb. 2012.

[8] Y. Shimooka et al., "Robust hermetic wafer level thin-film encapsulation technology for stacked MEMS/IC package," in *Proc. 58th Electron. Compon. Technol. Conf.*, May 2008, pp. 824–828.
[9] K. Chen, S. Wang, J. C. Salvia, R. Melamud, R. T. Howe, and T. W. Kenny, "Wafer-level epitaxial silicon packaging for out-of-plane RF MEMS resonators with integrated actuation electrodes," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 1, no. 3, pp. 310–317, Mar. 2011.
[10] A. B. Graham et al., "A method for wafer-scale encapsulation of large lateral deflection MEMS devices," *J. Microelectromech. Syst.*, vol. 19, no. 1, pp. 28–37, Feb. 2010.
[11] J. Sharma, J. Lee, S. Merugu, and N. Singh, "A robust bilayer cap in thin film encapsulation for MEMS device application," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 5, no. 7, pp. 930–937, Jul. 2015.
[12] S. K. Lahiri, "Mechanical stress induced void and hillock formations in thin films," in *Proc. IEEE Int. Workshop Memory Technol., Design, Test*, Aug. 1994, pp. 22–25.
[13] J.-W. Lee, J. Sharma, M. S. Narducci, S. Merugu, Z. X. Lin, and N. Singh, "Cavity-enhanced sacrificial layer micromachining for faster release of thin film encapsulated MEMS," *J. Micromech. Microeng.*, vol. 25, May 2015, Art. no. 065010.
[14] C. O'Mahony, M. Hill, Z. Olszewski, and A. Blake, "Wafer-level thin-film encapsulation for MEMS," *Microelectron. Eng.*, vol. 86, nos. 4–6, pp. 1311–1313, Apr. 2009.
[15] D. Reuter, A. Bertz, M. Nowack, and T. Gessner, "Thin film encapsulation technology for harms using sacrificial CF-polymer," *Sens. Actuators A, Phys.*, vols. 145–146, pp. 316–322, Nov. 2007.
[16] Y. Li et al., "Composite encapsulation films with ultrahigh barrier performance for improving the reliability of blue organic light-emitting diodes," *Adv. Mater. Interfaces*, vol. 7, no. 13, May 2020, Art. no. 2000237.
[17] J. Kim et al., "Hydrogen-assisted low-temperature plasma-enhanced chemical vapor deposition of thin film encapsulation layers for top-emission organic light-emitting diodes," *Organ. Electron.*, vol. 97, Oct. 2021, Art. no. 106261.
[18] A. Persano, J. Iannacci, P. Siciliano, and F. Quaranta, "Out-of-plane deformation and pull-in voltage of cantilevers with residual stress gradient: Experiment and modelling," *Microsyst. Technol.*, vol. 25, no. 9, pp. 3581–3588, Dec. 2018.
[19] K. D. Leedy, R. E. Strawser, R. Cortez, and J. L. Ebel, "Thin-film encapsulated RF MEMS switches," *J. Microelectromech. Syst.*, vol. 16, no. 2, pp. 304–309, Apr. 2007.
[20] D. W. Hess, "Plasma-enhanced CVD: Oxides, nitrides, transition metals, and transition metal silicides," *J. Vac. Sci. Technol. A, Vac., Surf., Films*, vol. 2, no. 2, pp. 244–252, Apr. 1984.
[21] A. Bagolini et al., "Development of MEMS MOS gas sensors with CMOS compatible PECVD inter-metal passivation," *Sens. Actuators B, Chem.*, vol. 292, pp. 225–232, Aug. 2019.
[22] A. Picciotto, A. Bagolini, P. Bellutti, and M. Boscardin, "Influence of interfaces density and thermal processes on mechanical stress of PECVD silicon nitride," *Appl. Surf. Sci.*, vol. 256, no. 1, pp. 251–255, Oct. 2009.
[23] C. A. Zorman, R. C. Roberts, and L. Chen, *MEMS Materials and Processes Handbook*. Boston, MA, USA: Springer, 2011.
[24] A. Tarraf, J. Daleiden, S. Irmer, D. Prasai, and H. Hillmer, "Stress investigation of PECVD dielectric layers for advanced optical MEMS," *J. Micromech. Microeng.*, vol. 14, no. 3, pp. 317–323, Nov. 2003.
[25] G. G. Stoney, "The tension of metallic films deposited by electrolysis," *Proc. Roy. Soc. London A*, vol. 82, no. 553, pp. 172–175, May 1909.
[26] K. Najafi, "Micropackaging technologies for integrated microsystems: Applications to MEMS and MOEMS," in *Proc. SPIE*, Jan. 2003, pp. 1–19.
[27] T. L. Burnett et al., "Large volume serial section tomography by Xe plasma FIB dual beam microscopy," *Ultramicroscopy*, vol. 161, pp. 119–129, Feb. 2016.
[28] J. Liu, R. Niu, J. Gu, M. Cabral, M. Song, and X. Liao, "Effect of ion irradiation introduced by focused ion-beam milling on the mechanical behaviour of sub-micron-sized samples," *Sci. Rep.*, vol. 10, no. 1, p. 10324, Jun. 2020.
[29] J. Schindelin et al., "Fiji: An open-source platform for biological-image analysis," *Nature Methods*, vol. 9, no. 7, pp. 676–682, Jul. 2012.

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Open Access funding provided by 'Consiglio Nazionale delle Ricerche-CARI-CARE-ITALY'
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