A Self-Powered Asynchronous Image Sensor With TFS Operation

Ruben Gomez-Merchan, Juan Antonio Leñero-Bardallo, *Member, IEEE*, and Ángel Rodríguez-Vázquez, *Life Fellow, IEEE*

Abstract—This article presents a self-powered image sensor with a novel pixel architecture with energy harvesting capabilities. Pixels are autonomous entities that can harvest or sense illumination independently. Pixels have a fully asynchronous operation and do not require to be scanned to read out their asynchronous output. The sensor was manufactured in UMC 180-nm technology and tested. Their specifications are competitive against the art, offering fast operation, a good balance between the energy consumed and harvested, and high-dynamic range operation. The article describes the sensor and pixel architectures in detail and provides experimental results. Sensor specifications are benchmarked against the art.

Index Terms— Asynchronous operation, diode efficiency, energy harvesting, image sensor, integrated photovoltaic cells, self-powered, stacked diodes, time-to-first-spike (TFS).
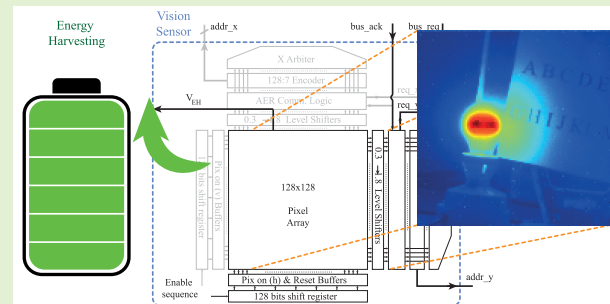
I. INTRODUCTION

ENERGY-EFICIENT sensors are the fuel to implement the Internet-of-Things (IoT) paradigm and, ultimately, critical enablers of the cyber-universe of fully interconnected analog sensors and digital processors [1]. The International Roadmap for Devices and Semiconductors [2] identifies the reduction of the size, weight, and power of sensor nodes as major challenges for deploying distributed sensor networks in an ever-increasing number of applications involving interaction with the environment and hence analog signal sensing. Because optical images and the visual sense have a large

quota among the different sensing modalities, it is arguable that energy-efficient vision sensors will play a relevant role in future IoT systems and intelligent electronic systems, in general [1], [2]. Indeed, different strategic agendas identify the deployment of visual intelligence as one primary driver for disruption in information technologies and microsystem design [3].

The quest for energy-efficient vision sensors encompasses diverse challenges. On the one hand, vision chip concepts and architectures capable of capturing and analyzing images with a minimum power budget are required. On the other hand, opportunities to harvest energy from the luminous stimuli must be explored. Reducing the power budget guarantees long working cycles under battery supply for low-latency applications. A reduced power budget besides energy harvesting might allow battery-less operation or very long battery-replacement cycles for high-latency applications.

The power reduction challenge calls for either the incorporation, at the focal plane, of embedded feature extraction and parallel processing resources [4] or for the use of asynchronous event-driven vision sensor concepts [5], [6], [7], among other strategies. The harvesting challenge calls for reconfiguring photodiodes to acquire either information or energy. Different image sensors combining both acquisition modes have been reported during the last few years (see [8], [9], [10], [11], [12], [13], [14], [15], [16] as representative examples). The vision sensor chip reported in this article employs event-driven pixels operating in the time-to-first-spike (TFS) mode [17], [18]
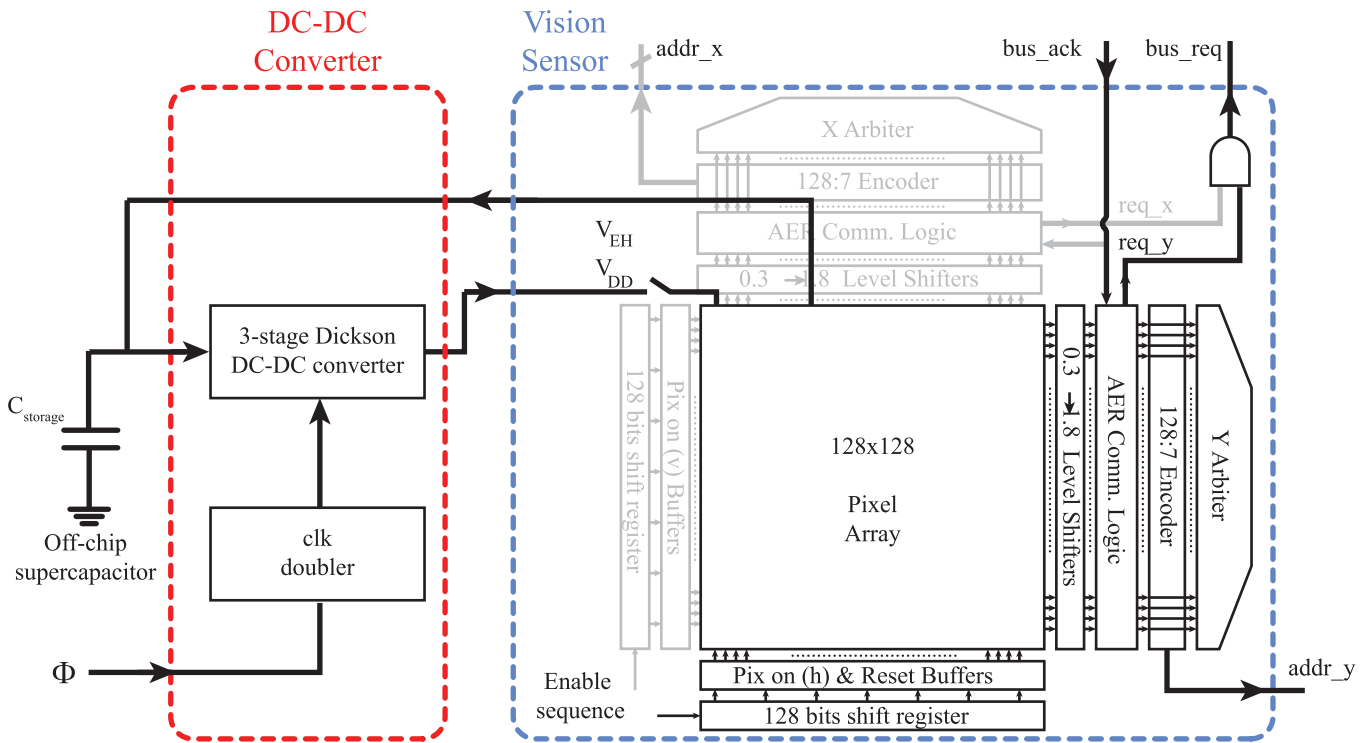
Fig. 1. Sensor architecture. The main constitutive blocks are: the pixel array, external buffers and control circuitry, external asynchronous arbitration logic to implement the AER communication protocol, and a Dickson dc–dc converter.

for information acquisition with reverse-biased photodiodes and the photovoltaic mode [19], [20], [21] for energy harvesting.

Asynchronous sensors are particularly well suited for power-budget reduction. Unlike conventional frame-based image sensors, asynchronous ones do not aim at scanning and encoding the whole pixel array, despite the relevance of the local pixel information, but at locating and encoding only pixel data that convey information encoded in the form of events, for example, temporal or spatial contrast. Hence, no energy is employed to encode and read pixels that do not contain information from an application point of view, thus making a significant difference from conventional imagers. Precluding such useless data encoding saves significant energy because ADC conversion and readout define the largest part of the imagers power budget [4]. Since the pixel operates in the TFS mode in this implementation, the information corresponds to the local pixel illumination, and all pixels are read out. However, the asynchronous nature of the pixel prevents dark pixels from occupying column ADCs for extended time intervals, leading to increased speed and power efficiency as pixels can be turned off immediately after readout.

1) Pixels are autonomous entities, and hence they can start harvesting energy individually once they have sensed their local illumination.
2) Their intrinsic asynchronous operation mode fits very well with application scenarios where snapshots are taken when an event occurs. For instance, an auxiliary dynamic vision sensor could trigger the proposed sensor after the recognition of an intruder in surveillance

systems [22], motion detection at home [23], traffic monitoring [24], or external operator-triggered scene luminance measurements [25].

Although several authors have already anticipated the advantages of using pulsewidth modulation to information in self-powered pixels with shallow power consumption [11], [13], [26], there are very few self-powered asynchronous sensors reported so far. Shi et al. [12] advanced a concept of an isolated asynchronous self-powered pixel. However, to our knowledge, no contributions report self-powered asynchronous image sensors. In this article, we propose a novel, fully asynchronous sensor implementation. Its pixels are autonomous entities that can harvest energy once they have sensed their local illumination. Thus, pixels contribute to harvesting energy once their local illumination level is read out. The article provides experimental results and insights into the pixel and sensor architecture. The proposed pixel architecture is the first one that allows different pixels to harvest energy or sense illumination independently and has not been reported yet. The image sensor is benchmarked against the art showing the advantages of the proposed architecture.

II. SYSTEM ARCHITECTURE

The proposed system is composed of two different blocks, as shown in Fig. 1. The first of them is a low-power asynchronous vision sensor, which combines the tasks of sensing and energy harvesting. The harvested energy is stored in a 7.5-mF low leakage off-chip supercapacitor, C_{storage}, designed for energy harvesting applications [27]. During the energy harvesting phase, the photodiodes are connected in parallel, charging the supercapacitor, whose voltage, V_{EH}, is limited
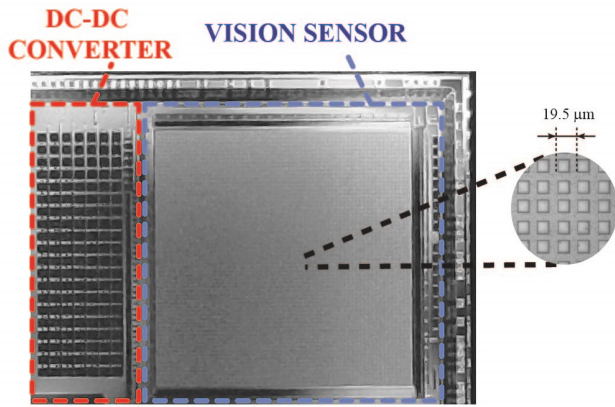
Fig. 2. Chip microphotograph. The yellow dotted line contains the image sensor. Pixel-level detail is shown. The red dotted line is the dc–dc converter. The image sensor dimensions are 2800 × 2800 mm². Pixel Dickson dc–dc converter dimensions, including the capacitor array, are 2430 × 1040 mm².

Fig. 3. I–V curve of a photodiode operating in the photovoltaic regime. The black arrow indicates how the curves vary with the illumination.

by the illumination conditions. This supercapacitor performs the function of a charge reservoir, with a reduced footprint of 3.2 × 2.5 mm. Although the pixels are designed to operate with a supply voltage as low as 250 mV, it is advisable to use larger supply voltages to decrease image artifacts caused by delays in the readout chain, thus reducing image degradation. These artifacts occur because the pixels encode the illumination level into the time it takes for the pixel to spike. Subsequently, any random delay (e.g., collisions in the readout channel) appears as random noise in the signal. Additionally, a lower supply voltage decreases the integration time, leading to a lower signal and thus decreasing the signal-to-noise ratio. This will be further addressed in Section III. Therefore, a dedicated dc–dc converter is included in the same die to step up the voltage at V_{EH}. Fig. 2 shows a microphotograph of the die containing both blocks.

The operation of the system is divided into two different phases. During the harvesting phase, the sensor is in an idle state, and all photodiodes operate in the photovoltaic mode. In this mode, a current I_{pv} flows from the cathode to the anode, and a voltage V_{pv} builds up at the junction, as depicted in Fig. 3. The collected charge is stored in the supercapacitor. Since power consumption is not continuous and the system does not have an external battery beyond the supercapacitor, no maximum power point tracking technique [28] was implemented. Therefore, the choice of a high capacitance allows storing a large amount of energy when the sensor is exposed to high illumination. When the system demands information from the scene, the sensing phase starts. During this phase, the photodiodes of the pixels are reverse-biased and operate in the TFS mode to measure the photocurrent. One major novelty of this sensor lies in how the pixels work after readout. The pixels stop consuming energy and start harvesting energy immediately after they send the information to the external receiver. In this way, the most illuminated pixels support the sensing operation. However, the supply voltage drops during the sensing operation, limiting the frame rate of the sensor by the time the dc–dc requires to regulate the supply voltage. This
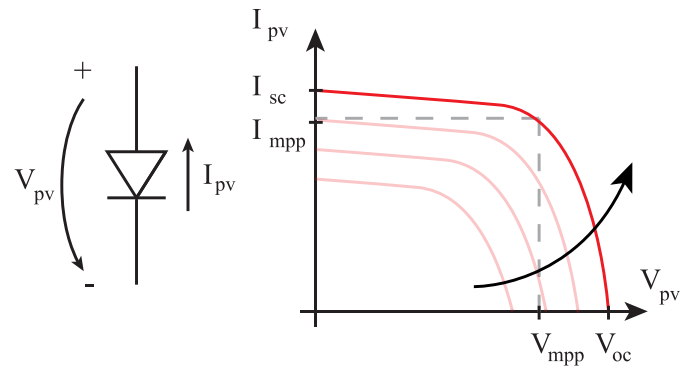
voltage drop depends on the time the pixels are consuming energy, and therefore on the scene.

A. Harvesting Subsystem

The core components of the harvesting subsystem are the photodiodes of the pixel. The cathode of the photodiode is connected to the ground when the pixel operates in the harvesting mode. Thus, the photocurrent leaving the anode (see Fig. 3) is used to charge the reservoir. Fig. 3 encloses four parameters. First, I_{sc} is the short-circuit current, that is, the current at 0 V. The voltage when no current flows through the junction is called the open-circuit voltage, V_{oc}, and it is the maximum voltage that can be generated while keeping the diode reverse-biased. If the junction voltage is greater than V_{oc}, it is forward-biased and consumes energy. Finally, there is a maximum power point, defined by I_{mpp} and V_{mpp}.

Photodiodes are usually connected in series to increase the effective value of V_{oc}. These branches of photodiodes are then connected in parallel to increase the available power; however, standard CMOS processes do not allow series association of photodiodes without penalty [20], [29]. Although other authors proposed a series connection of two diodes with different active areas to reduce parasitic current leakage [30], this approach is process-dependent and difficult to predict analytically. Thus, an only-parallel photodiode array is usually preferred, at the cost of a maximum V_{oc} close to 500 mV [19]. Photodiode stacking can also be employed to slightly increase V_{oc} [19], but still dc–dc conversion might be necessary to power a real system [21].

Fig. 4(a) shows the schematic of the dc–dc converter core. The dc–dc converter steps up the V_{EH} voltage to 700 mV, since the open-circuit voltage of a silicon photodiode is measured to be in the range of 250–450 mV at a luminance of 10–10 000 lx [19], [20], [31], [32]. The core is composed of a classic three-stage Dickson dc–dc converter. In this implementation, the well of the pMOS transistors is connected to the drain to reduce the reverse current [33]. Furthermore, connecting the bulk to the drain reduces the transistors' threshold voltage, allowing for operation at lower voltages. Indeed, the operation benefits from the current flowing through the source-to-bulk diode.
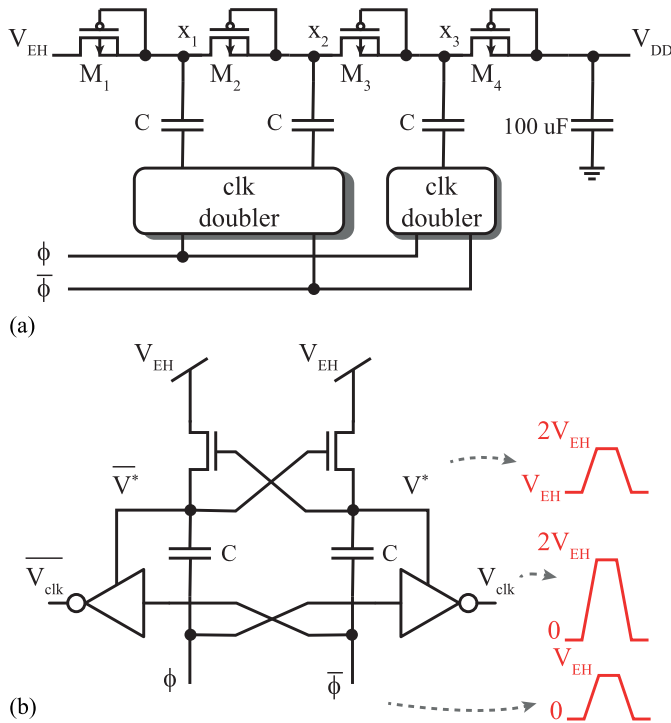
Fig. 4. (a) Three-stage pMOS Dickson charge pump. (b) Clk voltage doubler. All transistor dimensions are $[W\,(\mu\mathrm{m})]/[L\,(\mu\mathrm{m})] = 100/0.2$ and $C = 200$ pF.

The circuit in Fig. 4(a) operates as a conventional Dickson dc–dc converter but is designed to precharge the output voltage before operation (i.e., with no load) and then halt during operation. Initially, when Φ is low, the capacitor in x_1 is charged to $V_{\mathrm{EH}} - V_{\mathrm{drop}}$, where V_{drop} is the voltage drop across M_1. Since the output power when the converter is enabled is nearly zero, V_{drop} will tend to a value lower than the threshold voltage, as the subthreshold current of M_1 charges x_1; however, this implies that the dc–dc converter will have a slow startup. In this particular implementation, V_{drop} is close to 70 mV. On the other hand, when Φ is high, the voltage at x_1 increases by the voltage swing of the clock, V_{clk}. Thus, considering that the converter has three stages, the maximum output voltage of the dc–dc converter, V_{DD}, is determined as

$$V_{\mathrm{DD,max}} = V_{\mathrm{EH}} + 3 \cdot V_{\mathrm{clk}} - 4 \cdot V_{\mathrm{drop}}. \qquad (1)$$

Since the input voltage can be as low as 250 mV, the converter also includes a clock voltage doubler to ensure that the converter works under low-illumination conditions. Fig. 4(b) shows the schematic of the voltage doubler, where Φ and $\overline{\Phi}$ are the clock and inverted clock phases, respectively. This circuit functions as follows: suppose that $V^\star$ is close to V_{EH}. When $\overline{\Phi}$ goes from 0 to V_{EH}, $V^\star$ increases to $2V_{\mathrm{EH}}$, causing the output to go from 0 to $2V_{\mathrm{EH}}$.

The output of the dc–dc converter is connected to an off-chip 100 μF capacitor to reduce the voltage drop during operation. The frequency of the clock is controlled off-chip, since the voltage regulation of this converter was not included in this implementation. Thus, energy management still needs to be optimized in future implementations, including more complex circuits to enhance power management [21], [34].
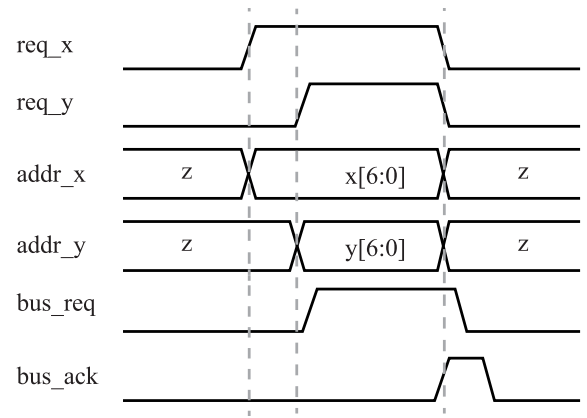

Fig. 5. Waveforms of the AER communication protocol, where a single event (pixel) is depicted in this example. x [6:0] and y [6:0] represent the coordinates of the pixel that generated the event, while z represents high-impedance.

B. Vision Sensor

The vision sensor employs a standard address event representation (AER) protocol [35], [36], [37], [38] to support asynchronous readout. Fig. 1 shows the block diagram of the vision sensor. In addition to the pixel array, the sensor is composed of column and row buffers followed by 0.3–1.8-V level shifters (in case the peripheral circuitry is biased at a voltage higher than the pixel array), AER communication logic blocks, 7-bit encoders, and row and column arbiter trees [38].

Fig. 5 summarizes the waveforms of the AER communication protocol. When a pixel generates an event, the X and Y arbiter trees decide which pixel accesses the address bus, while the AER communication logic blocks generate two global signals, req_y and req_x. The AND operation of both signals, bus_req indicates to the receiver that the pixel corresponding to the address bus coordinates has generated an event. This bus is composed of the output of the encoders, addr_x and addr_y. Finally, when the external peripheral has read and stored the pixel address, the external receiver activates bus_ack and the AER communication logic blocks generate the signals that reset the pixel.

Furthermore, two 128-bit shift registers store the enable sequence in such a way that the pix_on and reset signals are only enabled in certain rows and columns. This allows a region of interest (ROI) to sense the lighting level and keep the rest of the pixels harvesting energy.

III. PROPOSED PIXEL

Fig. 6 shows the schematic of the pixel, where V_{EH} is the global storage node shared among pixels. The pixel has been designed at the electrical level to operate with 250-mV supply voltage so that its operation is directly compatible with the voltage levels generated by the pixel array. Pixels are autonomous entities that can harvest energy from the environment while not sensing the illumination level. This is controlled by the signal stored in the per-pixel SR latch. Depending on the output of the latch, transistors M_{p1-2} and M_{n1-2} commute the terminals of the photodiode [39]. When the photodiode is reverse-biased, a comparator and
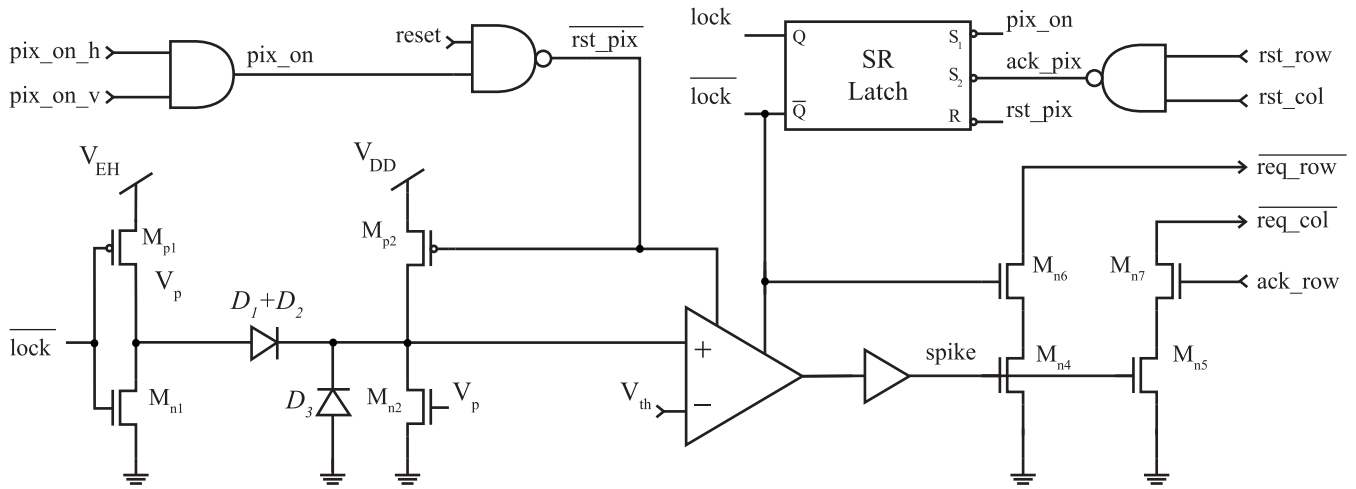
Fig. 6. Pixel schematics. It is composed of a photodiode and two pairs of switches, a comparator, pull-down transistors, a memory cell, and reset and enable logic. $D_1 + D_2$ is the parallel connection of the diodes labeled D_1 and D_2 in Fig. 7. Transistor dimensions [W (μm)]/[L (μm)] are: $M_{n1-2} = 0.44/0.4$, $M_{p1-2} = 0.5/0.4$, $M_{n4-7} = 5.7/0.18$.

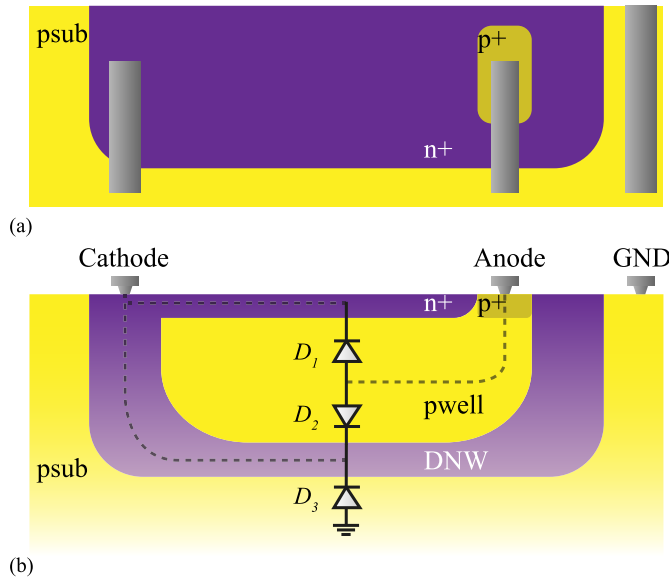Fig. 7. (a) Photodiode top view. (b) Photodiode cross section including the three p-n junctions: n^+/p-well (D_1), p-well/dnw (D_2), and dnw/psub (D_3).

pull-down transistors implement the TFS operation of an AER communication.

A. Photodiode Layout and Configurations

A description of diode implementation was advanced in a preliminary conference contribution [39]. As already mentioned, diodes toggle between two operation regimes: Photovoltaic and reverse-biased regime. The top view and the cross section of the photodiode are shown in Fig. 7, where three different diodes are connected in parallel, namely the n^+/p-well junction, D_1, the p-well/Deep n-well junction, D_2, and the Deep n-well/p-sub junction, D_3. The three diodes share the same cathode. The anodes of D_1 and D_2 are also shared, and the anode of D_3 is grounded; therefore,

D_3 cannot contribute to energy harvesting. It has previously been demonstrated that the architecture including D_1 and D_2 in parallel presents a higher open-circuit voltage than nonstacked diodes [19]. An interesting aspect introduced in this implementation is that the cathodes of D_1 and D_2 are connected extending the n^+ diffusion of D_1. This allows increasing the active area of D_1 and the pixel fill factor. While offering certain benefits, note that the utilization of these diodes and the integration scheme present some drawbacks in terms of noise performance. Compared to pinned photodiodes, where the charge-collecting layer is buried within the silicon crystal, surface traps result in a higher noise level in these devices. Furthermore, the integration scheme precludes the implementation of a floating diffusion, resulting in a high kTC noise due to the reset operation, which cannot be mitigated. Apart from these general considerations, we did not observe a significant improvement in noise performance between stacked and conventional junction configurations.

The configuration of the photodiode depends on the state of the pixel, which is defined by the local lock signal. When lock is deactivated (and, therefore, $\overline{lock}$ activated), the photodiode is reverse biased and a current can flow from the power supply node, V_{DD}, to ground through the photodiode, as depicted in Fig. 8(a). In contrast, when lock is logic high, the cathode is grounded, and the photodiode enters the photovoltaic regime to harvest energy immediately after readout. In this configuration, the photocurrent flows to the V_{EH} node, thus contributing to the power supply, as shown in Fig. 8(b).

The proper electrical design of M_{n3} and M_{p4} is crucial. To operate at supply voltages close to 250 mV, thin-gate-oxide transistors were selected. These two transistors must be strong enough to drive a current larger than the photocurrent, I_{ph}, when the pixel is under high-illumination conditions; however, the leakage current, I_{leak}, increases with the strength of the switch, leading to a random offset and therefore, pixel-to-pixel nonuniformities. Although I_{leak} can reduce the dynamic range, its effect can be alleviated by an off-chip calibration process.
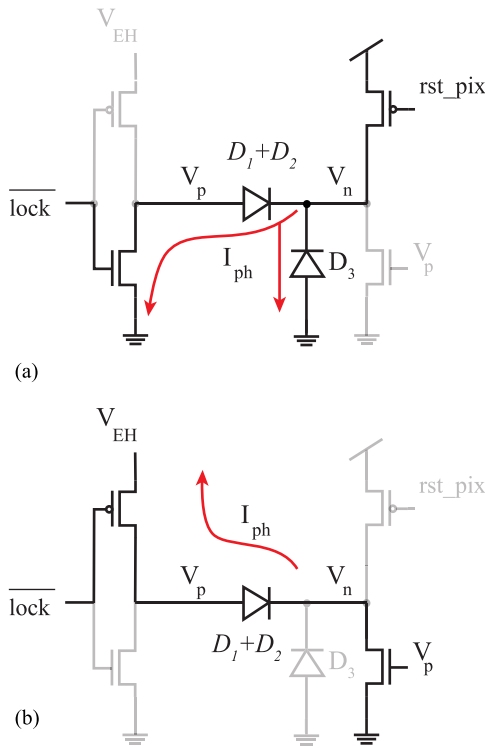
Fig. 8. Photodiode configuration when it is (a) sensing (b) harvesting. $D_1 + D_2$ is the parallel connection of the diodes labeled D_1 and D_2 in Fig. 7.

B. Pixel Operation

The pixels rely on the TFS concept to sense the illumination level of the scene. TFS operation is particularly interesting as the brightest pixels are read out first. Therefore, they instantly contribute to energy harvesting, while the less-illuminated ones consume energy. The operation is governed by pix_on, which is defined as the AND operation of two signals pix_on_h and pix_on_v. These signals are shared per row and per column, respectively, and are the output of the AND operation of the global pix_on signal and the sequence stored in the shift registers from Fig. 1. This allows the system to enable only an ROI, while the rest of the pixels are harvesting energy.

The different signals involved in the operation of the pixels are represented in Fig. 9. Before starting the sensing operation, pix_on is logic-low and $\overline{\text{rst\_pix}}$ is logic-high. Thus, lock is activated at the beginning of the operation. At this point, the operation can be divided into three phases.

1) Reset: To sense the pixel illuminance, the charge is integrated into the photodiode capacitance, C_{ph}. Therefore, the photodiode must be reset at the beginning of the operation. This is accomplished by the active-low $\overline{\text{rst\_pix}}$ signal and transistor M_{p4}. Note that this signal also unlocks the pixel. To prevent M_{p4} from driving a current in pixels outside the ROI, $\overline{\text{rst\_pix}}$ is implemented as the NAND function of pix_on and a global reset signal:

$$\overline{\text{rst\_pix}} = \overline{\text{pix\_on} \cdot \text{reset}}. \tag{2}$$

In this way, when the pix_on signal is logic high, $\overline{\text{rst\_pix}}$ is the negated value of reset. The reset time, t_{rst}, must be minimized to reduce power consumption, though this time must be long enough to reset high-illuminated photodiodes.
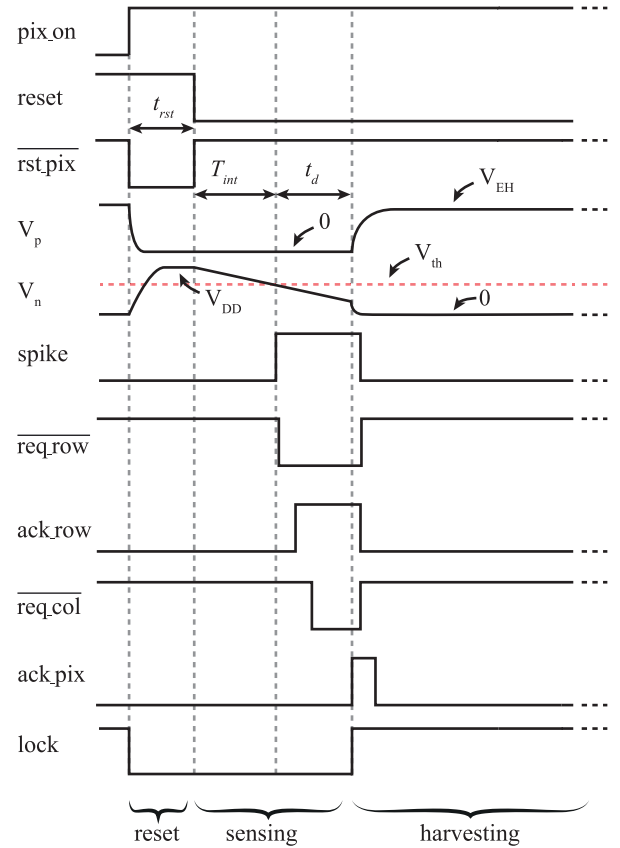

Fig. 9. Chronogram of the signals involved in the pixel's operation.

2) Integration: When reset is released, the voltage at node V_n decreases linearly depending on the photocurrent value. Defining T_{int} as the time it takes the photodiode to reach the voltage threshold of the comparator, V_{th}, the photocurrent can be computed as

$$I_{\text{ph,TFS}} = C_{\text{ph}} \cdot \frac{(V_{\text{DD}} - V_{\text{th}})}{T_{\text{int}}}. \tag{3}$$

It is important to note that the measurement depends on the value of V_{DD}. This value is the same for all pixels, but may vary from frame to frame. Thus, if the application requires computing information among different measurements, this voltage must be properly regulated. Furthermore, as shown in (3), IR drops in the V_{DD} line inside the pixel array during the reset phase can cause a systematic error in the signal, that is, patterns. However, the power consumption of the pixel array is low enough that the IR drop is insignificant. In contrast, IR drops during the integration phase can lead to a jitter at the comparator, resulting in random noise in the signal.

3) Readout: When V_n reaches V_{th}, the output of the comparator, spike, indicates that the pixel must be read out. To do so, the pixel uses transistors M_{n4-7}. First, the series combination of M_{n4} and M_{n6} pulls down $\overline{\text{req\_row}}$. This signal is shared by the entire row, implementing a wired OR gate. An arbiter circuit decides which row must be read and activates the ack_row signal, so pixels in that row can pull down $\overline{\text{req\_col}}$ signal and repeat the process at the column level. After granting access to the pixel, the AER communication logic
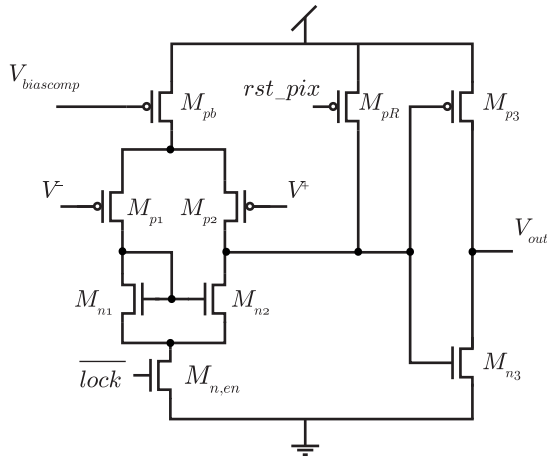
Fig. 10. Schematic of the pixel comparator. Transistor dimensions $[W(\mu m)]/[L(\mu m)]$ are: $M_{p,b} = 7.04/0.4$, $M_{p1} = M_{p2} = 3.52/0.18$, $M_{n1} = M_{n2} = 0.88/2$, $M_{n,en} = M_{p,en} = 0.88/0.3$, and $M_{p3} = M_{p4} = M_{n3} = M_{n4} = 0.44/0.3$.

Fig. 11. Measured short-circuit current and open-circuit voltage of photodiodes versus illuminance at $T = 30\ °C$.

block activates bus_req to indicate that valid data is set on the output address bus. Finally, the receiver stores the coordinates of the pixel and activates bus_ack. This signal triggers rst_col and rst_row, so that the local ack_pix signal locks the pixel.

C. Comparator

Fig. 10 shows the schematic of the in-pixel comparator. It is the only analog block and the dominant source of power consumption. Thus, a careful design of this component is crucial for proper performance. The comparator is composed of a 5T-OTA followed by a CMOS inverter, as depicted in Fig. 10. The comparator is designed to work at supply voltages as low as 250 mV and all transistors work in weak inversion to reduce the power consumption of the entire array, at the expense of a reduced speed. When the pixel is harvesting energy, $M_{n,en}$ switches off the bias current of the comparator using the $\overline{lock}$ control signal.

The comparator plays a crucial role in fixed-pattern noise (FPN) and temporal noise; as (3) shows, any variation in T_{int} or V_{th} modifies signal. Because the mismatch of pull-down transistors and other digital components entails negligible time variations concerning the signal, FPN has two primary sources, according to our study: the comparator's offset and the deviation of the leakage current of M_{p2} and M_{n2}. The latter can be minimized using thick-oxide devices. The comparator's offset has an impact on the effective value of V_{th}, resulting in a random pattern in the pixel array. Also, the transient noise of the comparator is translated into pixel signal transient noise. Offset-cancellation techniques can be employed to mitigate the effect of the comparator's offset in FPN. However, their implementation at the pixel level incurs a high cost in terms of area and increases the complexity of the operation. As such, the implementation of these techniques falls outside the scope of this study and merits further investigation in future research.

Additionally, the architecture depicted in Fig. 10 exhibits a systematic offset due to its asymmetrical topology. However, it would not affect the operation, as it is a systematic error
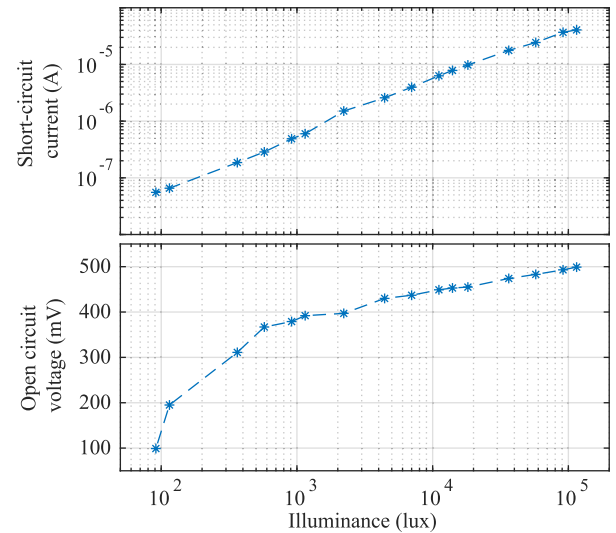
present in all pixels and can be compensated by adjusting the value of V_{th}.

Finally, the value of V_{th} is not trivial. It can be adjusted to alter T_{int} and, therefore, the sensitivity of the pixel to light, as depicted in (3). On the one hand, a low T_{int} value (high V_{th}) reduces the period of time the sensor consumes energy; however, the signal-to-noise ratio decreases, as delays in the readout chain (primarily due to collisions in the arbitration circuitry) are significant compared to T_{int}. The signal power is defined either by T_{int} or $(V_{DD} - V_{th})$ in the time or voltage domain, respectively. Thus, a low value of V_{th} enhances the signal power, minimizing the impact of the comparator's offset and noise, at the cost of reduced speed and increased energy consumption.

IV. EXPERIMENTAL RESULTS

A. Open-Circuit Voltage

Fig. 11 shows the dependence between the short-circuit current and the open-circuit voltage with illumination. Both parameters determine the sensor's capability to harvest energy since the maximum power generated by the array of photodiodes is related to these parameters. Empirical studies [40] have represented this correlation as

$$V_{mpp} \simeq k_1 V_{oc} \qquad (4)$$
$$I_{mpp} \simeq k_2 I_{sc} \qquad (5)$$

where k_1 and k_2 are constants. The range of k_1 has been found to be 0.71–0.78, while k_2 is in the range of 0.78–0.92 [40]. Given an illumination value, V_{EH} tends to reach V_{oc}, which has a logarithmic dependence on illumination and decreases linearly with temperature [19]. On the other hand, as the value of k_2 is approaching unity, the short-circuit current is found to be a determinant of the rate at which energy can be harvested, that is, the steepness at which the voltage of the supercapacitor increases when $V_{EH} < V_{oc}$. Consequently, the frame rate of the sensor is constrained by these two parameters and thus by the illumination. This is because the sensor must recover the
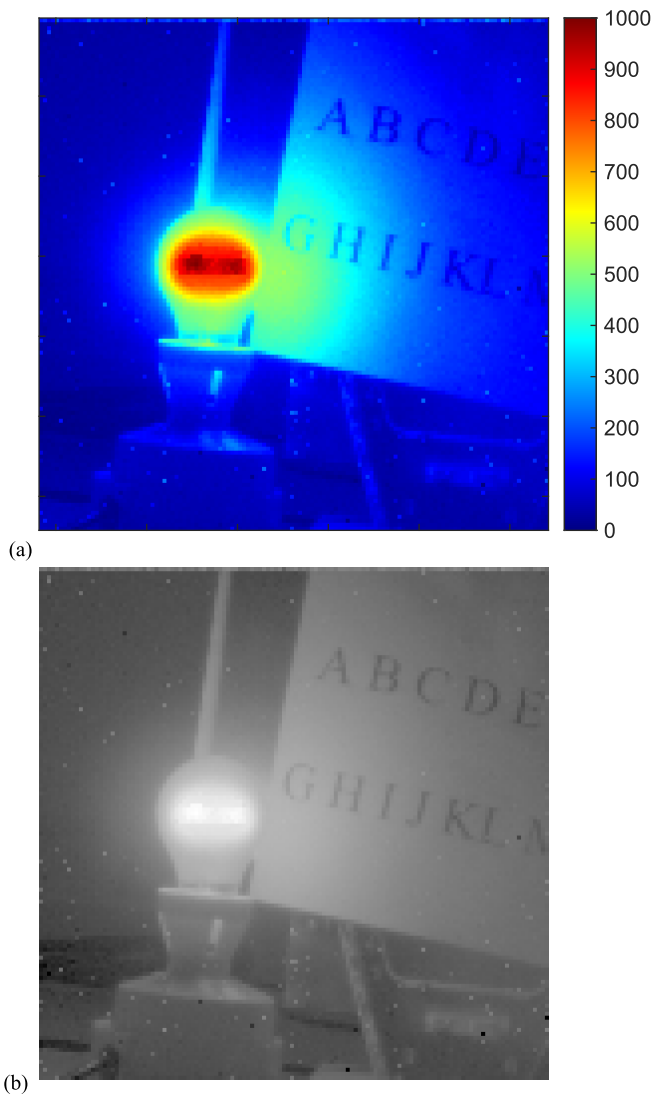
(a)

(b)

Fig. 12.   Sample image rendered with the sensor of a scene. (a) Colormap image. (b) 8-bit grayscale image.

energy expended during the image capture process to maintain a continuous operation.

B. Dynamic Power Consumption and Energy Harvesting

Fig. 12 shows an image captured with the sensor, wherein both a color map and an 8-bit grayscale representation of the illumination values have been employed. The image was acquired in 14 ms. Fig. 13 depicts experimental data showing the amount of energy consumed and harvested by the sensor during the previous image acquisition. Fig. 13 (top panel) shows the percentage of pixels operating in sensing and harvesting mode during the image acquisition. Initially, all pixels start in the sensing mode. At this instant, all pixels consume energy, and the sensor experiences its maximum power consumption, 1.14 μW. Then, the most illuminated pixels start to toggle to the harvesting mode. As a result, the overall power consumption of the sensor decreases with time. Consequently, acquiring a low-light scene requires greater energy consumption and, therefore, a longer harvesting period
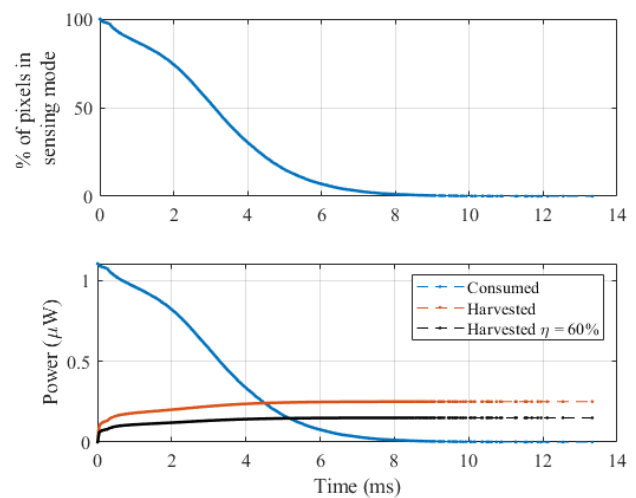

Fig. 13.   (Top) Number of pixels operating in sensing mode during the acquisition of the image shown in Fig. 12. (Bottom) Balance between the sensor power consumption and the power harvested by the pixels operating in harvesting mode during the image acquisition.

to recover from it, as pixels operate in the sensing mode for longer. In Fig. 13 (bottom panel), the measured energy consumed and the estimated energy harvested are plotted. Two situations have been considered to estimate the harvested energy: operating with an ideal Dickson dc–dc converter and with the implemented converter with an efficiency of $\eta = 60\%$. The sensor harvests the energy required to acquire the image in 17 ms. Analyzing the plots, we can conclude that the maximum energy that the sensor consumes when all pixels operate in sensing mode is higher than the maximum amount of energy collected when all pixels harvest energy simultaneously. Thus, the sensor cannot operate continuously and needs to harvest energy between acquisitions. In the example, an effective frame rate of 58 frames/s was achieved with the self-powering operation.

C. Acquisition Time Versus Illumination

The experimental results of Fig. 13 show that during the acquisition time, the consumed power and energy are higher than the harvested ones. Hence, if the sensor is intended to acquire images continuously, the frame rate will be restricted by the time required for the sensor to recover the energy used during one acquisition, as discussed in Sections IV-A and IV-B. The experimental results determined that the maximum continuous frame rate for the sensor was 51.5 frames/s at an illumination level of 500 lx, and 19.9 frames/s at an illumination level of 100 lx.

When a reduced latency between frames is required, the sensor can operate in the burst mode, allowing for the capture of multiple frames before recovering the energy expended during the process. In this scenario, assuming that the dc–dc converter is fast enough, the frame rate will be limited by the readout time, specifically the value of T_{int} of the darkest pixel. Fig. 14 depicts experimental data showing the maximum possible frame rate versus the illuminance. All pixels were exposed to the same illumination level. Given
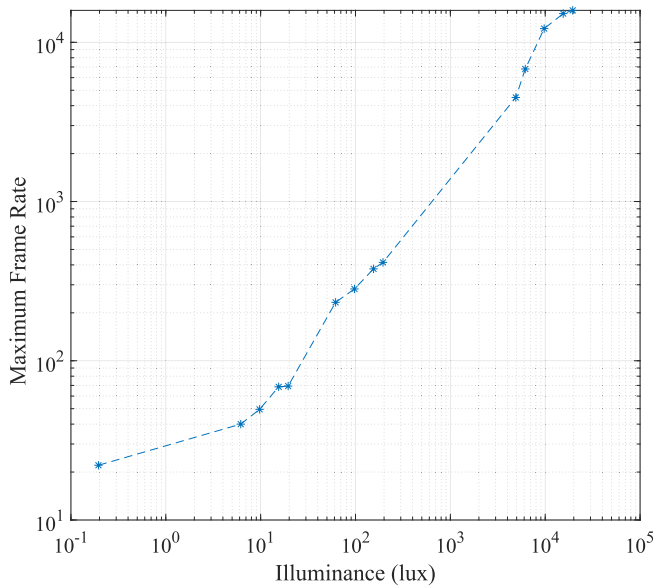
Fig. 14. Measured maximum frame rate versus illumination. All pixels were illuminated uniformly. The maximum frame rate is determined by the sum of the image acquisition and readout time.
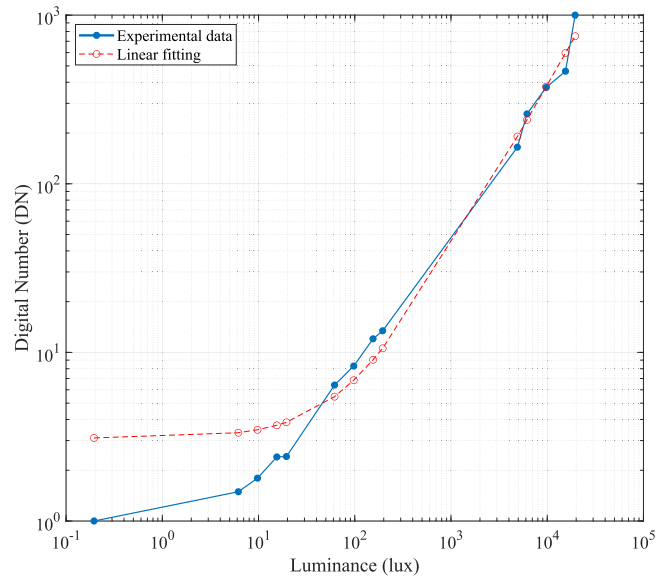

Fig. 15. Measured sensor outputs (DN) versus illumination over six decades. The red line indicates the linear data fitting. The coefficient of determination is $r^2 = 0.9370$.

that the external supercapacitor is precharged and it stores enough energy, the sensor could acquire images at 50 frames/s with a chip illumination of only 10 lx. It must be remarked that the energy balance is quite complex for visual scenes with a large intrascene dynamic range, with high- and low-illuminated pixels. When a high-speed acquisition is necessary, a defined acquisition time can be established for reading out the image. However, this comes at the cost of losing the information from pixels whose T_{int} exceeds the defined acquisition time (low-illuminated pixels), resulting in a trade-off between image quality and acquisition speed, which will vary depending on the specific scenario and the application requirements.

D. Pixel Response to Illumination and FPN

Fig. 15 shows the measured sensor output versus the chip illuminance. The digital number is normalized and ranges from 0 to 1000. All pixels were illuminated uniformly with a white Lambertian light source. In this experiment, the luminance was varied while maintaining the same electrical conditions, allowing for the determination of the intrascene dynamic range, which was found to be 100 dB. The red trace corresponds with the linear data fitting. The coefficient of determination is $r^2 = 0.9370$. The sensor response to illumination is linear within an illumination range of four decades. Below 10 lx, the sensor output linearity is limited by the current leakage introduced by the transistors connected to the anode and cathode of the photodiode in Fig. 6. This leakage is comparable to the photocurrent with low illumination and is responsible for the sensor nonlinearity in such circumstances. The current leakage also impacts the FPN of the pixels with low illumination because the leakage current has a large variability from pixel to pixel. The measured FPN was 5.34% with a sensor illuminance of 1 klx. This limitation could be amended by using transistors with a thicker gate

oxide. Therefore, the lower limit of the dynamic range is determined by the leakage current of M_{p2} and M_{n2}, while the bandwidth of the comparator determines the upper limit, that is, the digital number is limited when T_{int} is shorter than the response time of the comparator.

Sensor calibration is also possible to improve image quality. The procedure can be performed off-chip by subtracting the illumination values measured without illumination from each frame.

V. BENCHMARKING

In order to evaluate the performance of the proposed sensor compared to existing solutions, the image figure of merit (iFoM) was calculated and compared. The energy required to capture a single frame was determined by integrating the blue trace in Fig. 13. However, for a fair comparison, the iFoM was calculated using the assumption of a dark frame, in which the power consumption is approximately equal to the peak power consumption (1.14 μW) for the majority of the time, and a frame rate of 19.9 frames/s under 100-lx ambient lighting conditions. The resulting iFoM was found to be 3.41 fJ/pixel·code.

Table I compares the specifications of the implemented sensor against other relevant and recent self-powered ones. Although different architectures for low-power imaging have been reported in the past [41], [42], [43], we only compare the proposed sensor to different image sensors implementing energy harvesting capabilities. Among the reported solutions in the literature, the selected ones were chosen for their outstanding balance between power consumption and frame rate (i.e., iFoM) or their unique functionalities. The work presented in [11] reports a PWM sensor that operates at 0.32 V, being compatible with the native open-circuit voltages of silicon photodiodes. This work was continued in further publications [13], obtaining a better image quality and linearity

TABLE I
STATE-OF-THE-ART COMPARISON

Features Work	This work	Tang 2011 [31]	Park 2018 [10]	Chiou 2016 [11]	Cevik 2015 [8]	H.Wang 2015 [16]
Pixel Architecture	Asynchronous pixel with TFS readout	APS pixel with synchronous readout	APS pixel with synchronous readout	Synchronous pixel with PWM readout	APS pixel with synchronous readout	Synchronous pixel with ADC readout
Technology	UMC 0.18 μm	0.35 μm	0.18 μm	0.18 μm	0.35 μm	0.5 μm
Pixel complexity	54 Transistors	4 Transistors	3 Transistors	5 Transistors	4 Transistors	14 transistors
Pixel Count	128 × 128	128 × 96	100 × 90	256 × 192	64 × 45	32 × 32
Fill factor (%)	30.65	39	46 / 94 ^{a}	30.8	65	36
Pixel Pitch	19.5 μm	21 μm	5 μm	7.5 μm	18 μm	54 μm × 48 μm
Supply Voltage	0.7 V	1.35 V	0.6 V	0.32 V	1 V	ND
Pixel Power Consumption	70 pW	30.7 pW	ND	ND	ND	ND
Sensor Power Consumption	1.14 μW	10 μW	3.9-57.8 μW	10.6 μW	9.06 μW	ND
Frame rate for the reported sensor power consumption (fps)	51.5fps@500lux, 19.9fps@100lux	9.6	7.5-10	6.5	21.2	ND
Dynamic Range	100 dB	ND	ND	137 dB	60.6 dB	ND
FPN (%)	5.34	>1	9.2	0.189	0.33	ND
iFoM (fJ/pixel·code)	3.41	164.06	225.8	8.6	578	3304.7
Independent Energy harvesting and light sensing operation	Yes (at pixel level)	No	No	No	No	Yes (configurable)

^{a}The pixel has two stacked photodiodes. Results are reported for the photodiode used to sense light and the one used to harvest energy, respectively.

but worse iFoM. The work in [10] demonstrates an APS solution that features two stacked diodes (one for harvesting, and the other for sensing) that operates at 0.6 V, while the work presented in [8] describes an APS architecture in which the same photodiode can work as a harvester or sensing unit. Also, Wang and Leon-Salas [16] reported an APS sensor in which the photodiodes can independently switch terminals, enabling each pixel to function in sensing or harvesting mode. However, during image acquisition, the pixels cannot operate in both modes, and iFoM is worse than that of other reported sensors due to the lower resolution of the implemented ADCs. In summary, the proposed sensor exhibits the most favorable value of iFoM, followed by PWM sensors, and then by APS sensors.

The proposed architecture is the only one compatible with simultaneous harvesting and image acquisition at the pixel level. This possibility optimizes the amount of energy harvested because the most illuminated pixels have an earlier and higher contribution to the sensor's self-powered operation. Moreover, the proposed asynchronous readout allows dynamically deciding the amount of time dedicated to acquiring one image. It is possible to render one image after receiving a certain number of events or update the image representation dynamically. Therefore, there is room for further research work to investigate the optimal balance between integration time, image quality, and power consumption.

The proposed architecture outperforms the art, offering a very low image acquisition and readout time, exploiting the advantages of the fast asynchronous readout circuitry. Frames can be acquired within a short time interval. Therefore, the ratio between the amount of time the sensor is harvesting and sensing is higher than in previous implementations. Even if we consider a continuous sensor operation, powering the sensor externally, the pixel energy consumption is competitive over the art. The sensor also offers high intrascene dynamic range operation. The main limitation of the proposed architecture is the FPN level, which is higher than the art. This can be amended in further implementations by performing a careful study to reduce the current leakage of the transistors that alters the photocurrent measurement. At this point, there is room for improvement by selecting different types of transistors or simplifying the number of transistors connected to the photodiode.

Furthermore, the functionalities of the sensor can be extended to implement a Free Running mode. In this mode, pixels are reset after readout, and events are generated continuously. Therefore, the temporal error caused by the collisions is averaged. However, pixels are continuously consuming energy during this mode, limiting its use to periods when the average illumination is high enough. To implement this function, switches must be added to V_p to keep the photodiode reverse-biased regardless of lock and a reset

logic must be implemented to reset the pixel when lock is activated.

VI. Conclusion

A new self-powered asynchronous image sensor has been presented. The proposed architecture amends some of the limitations of classic synchronous pixel architectures to harvest energy. On the one hand, pixels are autonomous entities that can harvest energy or sense illumination independently, not necessary to divide the sensor operation into two phases associated with energy harvesting and sensing. On the other hand, the proposed asynchronous readout scheme proves to be very competitive to harvest energy because there is no requirement for an A/D conversion or to read out all the pixels to render one image. With the proposed sensor architecture, the system can trade between image quality, frame rate, and power consumption. All of these capabilities open the possibility for further research work to optimize sensor operation and the amount of energy harvested depending on the illumination conditions and image rendering requirements.

References

[1] M. M. Sandhu, S. Khalifa, R. Jurdak, and M. Portmann, "Task scheduling for energy-harvesting-based IoT: A survey and critical analysis," *IEEE Internet Things J.*, vol. 8, no. 18, pp. 13825–13848, Sep. 2021.

[2] International Roadmap for Devices and Systems 2021 Edition. (2021). *Systems and Architectures*. [Online]. Available: https://irds.ieee.org/images/files/pdf/2021/2021IRDS_SA.pdf

[3] *Emerging Vision Technologies: Enabling a New Era of Intelligent Devices*. San Diego, CA, USA: Qualcomm, 2016.

[4] A. Rodríguez-Vázquez, J. Fernández-Berni, J. A. Leñero-Bardallo, I. Vornicu, and R. Carmona-Galán, "CMOS vision sensors: Embedding computer vision at imaging front-ends," *IEEE Circuits Syst. Mag.*, vol. 18, no. 2, pp. 90–107, 2nd Quart., 2018.

[5] C. Posch, T. Serrano-Gotarredona, B. Linares-Barranco, and T. Delbruck, "Retinomorphic event-based vision sensors: Bioinspired cameras with spiking output," *Proc. IEEE*, vol. 102, no. 10, pp. 1470–1484, Oct. 2014.

[6] T. Delbrück, B. Linares-Barranco, E. Culurciello, and C. Posch, "Activity-driven, event-based vision sensors," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Jun. 2010, pp. 2426–2429.

[7] J. A. Leñero-Bardallo, R. Carmona-Galán, and A. Rodríguez-Vázquez, "Applications of event-based image sensors—Review and analysis," *Int. J. Circuit Theory Appl.*, vol. 46, pp. 1620–1630, Aug. 2018.

[8] I. Cevik and S. U. Ay, "An ultra-low power energy harvesting and imaging (EHI) type CMOS APS imager with self-power capability," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2177–2186, Sep. 2015.

[9] A. Fish, S. Hamami, and O. Yadid-Pecht, "CMOS image sensors with self-powered generation capability," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1210–1214, Nov. 2006.

[10] S.-Y. Park, K. Lee, H. Song, and E. Yoon, "Simultaneous imaging and energy harvesting in CMOS image sensor pixels," *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 532–535, Apr. 2018.

[11] A. Y.-C. Chiou and C.-C. Hsieh, "A 137 dB dynamic range and 0.32 V self-powered CMOS imager with energy harvesting pixels," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2769–2776, Nov. 2016.

[12] C. Shi, M. K. Law, and A. Bermak, "A novel asynchronous pixel for an energy harvesting CMOS image sensor," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 1, pp. 118–129, Jan. 2011.

[13] A. Y. Chiou and C. Hsieh, "An ULV PWM CMOS imager with adaptive-multiple-sampling linear response, HDR imaging, and energy harvesting," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 298–306, Jan. 2019.

[14] S. U. Ay, "A CMOS energy harvesting and imaging (EHI) active pixel sensor (APS) imager for retinal prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 535–545, Dec. 2011.

[15] H.-T. Wang and W. D. Leon-Salas, "A hybrid CMOS imager with sensing and energy harvesting capabilities," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2013, pp. 2634–2637.

[16] H.-T. Wang and W. D. Leon-Salas, "An image sensor with joint sensing and energy harvesting functions," *IEEE Sensors J.*, vol. 15, no. 2, pp. 902–916, Feb. 2015.

[17] C. Shoushun and A. Bermak, "A low power CMOS imager based on time-to-first-spike encoding and fair AER," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 5, May 2005, pp. 5306–5309.

[18] C. Shoushun and A. Bermak, "Arbitrated time-to-first spike CMOS image sensor with on-chip histogram equalization," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 3, pp. 346–357, Mar. 2007.

[19] R. Gómez-Merchán, D. Palomeque-Mangut, J. A. Leñero-Bardallo, M. Delgado-Restituto, and A. Rodríguez-Vázquez, "A comparative study of stacked-diode configurations operating in the photovoltaic region," *IEEE Sensors J.*, vol. 20, no. 16, pp. 9105–9113, Aug. 2020.

[20] U. Çilingiroglu, B. Tar, and Ç. Özmen, "On-chip photovoltaic energy conversion in bulk-CMOS for indoor applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 8, pp. 2491–2504, Aug. 2014.

[21] E. Ferro, P. López, V. M. Brea, and D. Cabello, "Micro-energy harvesting system including a PMU and a solar cell on the same substrate with cold startup from 2.38 nW and input power range up to 10 μW using continuous MPPT," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5105–5116, Jun. 2019.

[22] J. A. Leñero-Bardallo, P. Häfliger, R. Carmona-Galán, and A. Rodríguez-Vázquez, "A bio-inspired vision sensor with dual operation and readout modes," *IEEE Sensors J.*, vol. 16, no. 2, pp. 317–330, Jan. 2016.

[23] Z. Fu, T. Delbrück, P. Lichtsteiner, and E. Culurciello, "An address-event fall detector for assisted living applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 2, pp. 88–96, Jun. 2008.

[24] M. Litzenberger et al., "Vehicle counting with an embedded traffic data system using an optical transient sensor," in *Proc. IEEE Intell. Transp. Syst. Conf.*, Seattle, WA, USA, Sep. 2007, pp. 36–40.

[25] C. Posch, D. Matolin, and R. Wohlgenannt, "A QVGA 143 dB dynamic range asynchronous address-event PWM dynamic image sensor with lossless pixel-level video compression," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2010, vol. 46, no. 1, pp. 259–275.

[26] M.-T. Chung, C.-L. Lee, and C.-C. Hsieh, "A 0.5 V PWM CMOS imager with 82 dB dynamic range and 0.055% fixed-pattern-noise," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2522–2530, Oct. 2013.

[27] *Electric Double Layer Capacitor*, Seiko Instrum., Chiba, Japan, Aug. 2018. [Online]. Available: https://www.seiko-instruments.de/fileadmin/Editors/COMP/PDF/MicroBattery_catalogue_E_2018A_forWeb.pdf

[28] C. Lu, V. Raghunathan, and K. Roy, "Maximum power point considerations in micro-scale solar energy harvesting systems," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 273–276.

[29] F. Horiguchi, "Integration of series-connected on-chip solar battery in a triple-well CMOS LSI," *IEEE Trans. Electron Devices*, vol. 59, no. 6, pp. 1580–1584, Jun. 2012.

[30] M. K. Law and A. Bermak, "High-voltage generation with stacked photodiodes in standard CMOS process," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1425–1427, Dec. 2010.

[31] F. Tang and A. Bermak, "An 84 pW/frame per pixel current-mode CMOS image sensor with energy harvesting capability," *IEEE Sensors J.*, vol. 12, no. 4, pp. 720–726, Apr. 2012.

[32] R. Gomez-Merchan, M. Lopez-Carmona, J. A. Lenero-Bardallo, and A. Rodriguez-Vazquez, "A high-speed low-power sun sensor with solar cells and continuous operation," in *Proc. IEEE 47th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2021, pp. 147–150.

[33] A. Ballo, A. D. Grasso, and G. Palumbo, "A review of charge pump topologies for the power management of IoT nodes," *Electronics*, vol. 8, no. 5, p. 480, 2019.

[34] S. Ghosh, H.-T. Wang, and W. D. Leon-Salas, "A circuit for energy harvesting using on-chip solar cells," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4658–4671, Sep. 2014.

[35] M. Silviotti, "Wiring considerations in analog VLSI systems with application to field-programmable networks," Ph.D. dissertation, California Inst. Technol., Pasadena, CA, USA, 1991.

[36] M. Mahowald, *An Analog VLSI System for Stereoscopic Vision*. Norwell, MA, USA: Kluwer, 1994.

[37] A. Mortara, E. A. Vittoz, and P. Venier, "A communication scheme for analog VLSI perceptive systems," *IEEE J. Solid-State Circuits*, vol. 30, no. 6, pp. 660–669, Jun. 1995.

[38] K. A. Boahen, "Point-to-point connectivity between neuromorphic chips using address events," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 5, pp. 416–434, May 2000.

[39] R. Gomez-Merchan, R. De La Rosa-Vidal, J. A. Leñero-Bardallo, and Á. Rodríguez-Vázquez, "On the implementation of in-pixel controlled diodes with sensing and energy harvesting capabilities," in *Proc. 17th Conf. Ph. D Res. Microelectron. Electron. (PRIME)*, Jun. 2022, pp. 105–108.

[40] T. Esram and P. L. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 439–449, Jun. 2007.

[41] J. Choi, J. Shin, D. Kang, and D.-S. Park, "Always-on CMOS image sensor for mobile and wearable devices," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 130–140, Jan. 2016.

[42] N. Couniot, G. D. Streel, F. Botman, A. K. Lusala, D. Flandre, and D. Bol, "A 65 nm 0.5 V DPS CMOS image sensor with 17 pJ/frame.pixel and 42 dB dynamic range for ultra-low-power SoCs," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2419–2430, Oct. 2015.

[43] C. Yin, C. F. Chiu, and C. C. Hsieh, "A 0.5 V, 14.28-kframes/s, 96.7-dB smart image sensor with array-level image signal processing for IoT applications," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1134–1140, Mar. 2016.

Juan Antonio Leñero-Bardallo (Member, IEEE) received the M.Sc. degree in telecommunications engineering and the Ph.D. degree in microelectronics from the University of Seville, Seville, Spain, in 2005 and 2010, respectively.

After the completion of his Ph.D. degree, he has served in several academic institutions and worked for the semiconductor industry at Chronocam Inc., Paris, France. From September 2010 to March 2010, he has worked as a Postdoctoral Associate with Yale University, New Haven, CT, USA. From March 2010 to August 2013, he was a Postdoctoral Associate with the University of Oslo, Oslo, Norway. Since February 2018, he has been an Associate Professor with the University of Seville. His main research interests include addressing event representation (AER) vision systems, frame-based vision sensors, smart sensors, and biomedical systems.

Dr. Leñero-Bardallo has been a member of the IEEE Sensory Systems Technical Committee since 2012. He was the IEEE International Symposium on Circutis and Systems (ISCAS) 2020 Financial Chair.

Ángel Rodríguez-Vázquez (Life Fellow, IEEE) received the Ph.D. degree in physics-electronics from the Universidad de Sevilla, Seville, Spain, in 1982, with several awards, including the IEEE Rogelio Segovia Torres Award in 1981.

After staying at the University of California at Berkeley, Berkeley, CA, USA, and Texas A&M University, College Station, TX, USA, he became a Full Professor of Electronics at the University of Sevilla in 1995. He co-founded the Instituto de Microelectrónica de Sevilla and started a Research Laboratory on Analog and Mixed-Signal Circuits for Sensors and Communications. He has always been looking for a balance between long-term research and industrial innovation. In 2001, he was the Main Promotor of AnaFocus Ltd., Seville, where he has served as the CEO until June 2009, when the company reached maturity as a worldwide provider of smart CMOS imagers. He has also participated in the foundation of the Hungarian startup AnaLogic Ltd., Budapest, Hungary. He has filed ten patents; AnaFocus started based on his patents on vision chip architectures. His research interests include smart imagers, vision chips, and biomedical circuits, always with an emphasis on system integration. His laboratory designed many high-performance mixed-signal chips in the framework of Spanish, European, and USA research and development programs. These included three generations of vision chips, analog front-ends for XDSL MoDems, ADCs for wireless communications, ADCs for automotive sensors, chaotic signals generators, and complete MoDems for power-line communications.

Dr. Rodríguez-Vázquez's publications have some 9900 citations and several awards: the IEEE Guillemin-Cauer Best Paper Award, two Wiley's *International Journal of Circuit Theory and Applications* (IJCTA) Best Paper Awards, two IEEE European Conference on Circuit Theory and Design (ECCTD) Best Paper Awards, one IEEE-International Symposium on Circutis and Systems (ISCAS) Best Paper Award, one Society of Photo-Optical Instrumentation Engineers, Information Society Technologies (SPIE-IST) Electronic Imaging Best Paper Award, the IEEE ISCAS Best Demo-Paper Award, and the IEEE International Conference on Electronics, Circuits and Systems (ICECS) Best Demo-Paper Award. He received the Ph.D. degree with several awards, including the IEEE Rogelio Segovia Torres Award in 1981. He chaired several international IEEE (Nonlinear Dynamics of Electronic Systems (NDES) 1996, Cellular Neural Networks Automata (CNNA) 1996, ECCTD 2007, European Solid State Circuits Conference (ESSCIRC) 2010, ICECS 2013) and SPIE conferences. He has served as the VP of Region 8 of IEEE Circuits and Systems Society (CASS) (2009–2012) and the Chair of the IEEE CASS Fellow Evaluation Committee (2010 and 2012–2015). He was the General Co-Chair of IEEE ISCAS 2020. He has served as an editor for IEEE and non-IEEE journals and is on the committee of several international journals and conferences.

Ruben Gomez-Merchan was born in Cáceres, Spain, in 1997. He received the bachelor's (Hons.) degree in electronics, robotics, and mechatronics engineering and the master's (Hons.) degree in microelectronics from the University of Seville (US), Seville, Spain, in 2019 and 2020, respectively, where he is currently pursuing the Ph.D. degree in physics-electronics.

His work was supported by the Spanish Government through the Formación del Profesorado Universitario (FPU) Program under Grant FPU19/03410. From 2018 to 2019, he was with the Department of Electronic Engineering, US. In 2019, he was granted by the Spanish National Research Council (CSIC), starting his activity at the Instituto de Microelectronica de Sevilla (IMSE), USA. From September 2022 to December 2022, he was a Visiting Researcher with Sony Europe Design Center, Oslo, Norway. His main research interests include dc/dc converters and PV systems. His main research interests also include smart complementary metal oxide semiconductor (CMOS) sensors and address event representation (AER) vision systems.

Dr. Gomez-Merchan was a recipient as a coauthor of the Best Paper Award of the Imaging Sensors and Systems Conference at Electronic Imaging 2023.